CHAPTER 4

Televisions and Monitors

Power Devices in TV & Monitor Applications

(including selection guides)

4.1.1 An Introduction to Horizontal Deflection

Introduction

This section starts with the operation of the power semiconductors in a simple deflection test circuit leading to a functional explanation of a typical TV horizontal deflection circuit. The operation of the common correction circuits are discussed and the secondary function of the horizontal deflection circuit described.

Deflection Test Circuit

The horizontal deflection test circuit used to assess Philips deflection transistors is shown in Fig. 1 below. Lc represents the horizontal deflection coils.

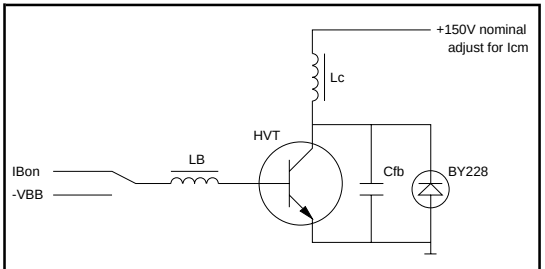


Fig. 1. Test Circuit for Deflection Transistors

This circuit is a simplification of a practical horizontal deflection circuit. It can be used to produce the voltage and current waveforms seen by both the transistor and the diode in a real horizontal deflection circuit. It is, therefore, very useful as a test circuit for switching times and power dissipation. The waveforms produced by the test circuit are shown in Fig. 2.

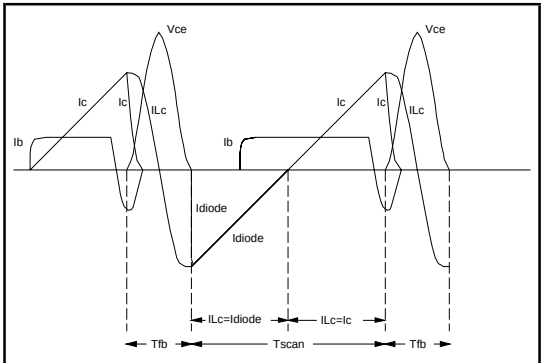


Fig. 2. Test Circuit Waveforms

Cycle of Operation

Briefly going through one cycle of operation, the sequence of events is as follows. (This can be followed through on the waveforms shown in detail in Fig. 3, by starting on the left and following the stages numbered 1 to 8).

1. Turn on the deflection transistor by applying a positive current drive to the base. The voltage on the collector is now approximately 0.5V because the device is fully on. This means that the voltage across the coil, Lc, is the full line voltage; in this case 150V.

2. According to the law, V = L • dI/dt, the current in the coil Lc will now start to rise with a gradient given by 150V/Lc. This portion of the coil current (ILc), is the sawtooth portion of the collector current in the transistor (Ic).

3. Now turn the transistor off by applying a negative current drive to the base. Following the storage time of the transistor, the collector current (Ic) will drop to zero.

4. The current in Lc (ILc) is still flowing! This current, typically 4.5A for testing the BU2508A, cannot flow through the transistor any more, nor can it flow through the reverse biased diode, BY228. It, therefore, flows into the flyback capacitor, Cfb, and so the capacitor voltage rises as ILc falls. Because Cfb is connected across the transistor, the rise in capacitor voltage is seen as a rise in Vce across the transistor.

Lc will transfer all its energy to Cfb. The capacitor voltage reaches its peak value, typically 1200V, at the point where ILc crosses zero.

5. Now we have a situation where there is zero energy in Lc but there is a very large voltage across it. So ILc will rise, and since this current is supplied by Cfb, the voltage across Cfb falls. This is, of course, a resonant LC circuit and essentially it is energy which is flowing, first from the inductor, Lc, to the capacitor, Cfb, and then from the capacitor, Cfb, to the inductor, Lc. Note that the current in Lc is now flowing in the opposite direction to what it was previously. It is, therefore, a negative current.

6. This resonance would continue, with the coil current and the capacitor voltage following sinusoidal paths, were it not for the diode, BY228. When the capacitor voltage starts to go negative the diode becomes forward biased and effectively clamps the capacitor voltage to approximately -1.5V, the diode VF drop. This also clamps the voltage across Lc to approximately the same value as it was when the transistor was conducting, ie the line voltage (150V). Note that the coil current is now being conducted by the diode, and hence ILc = Idiode.

7. So we have again a current ramp in Lc with a dI/dt equal to 150/Lc. This current starts with a value equal to the value it had at the end of the transistor on time (neglecting circuit losses). It is, however, flowing in the opposite (negative) direction and so the positive dI/dt will bring it back towards zero.

8. Before ILc actually reaches zero, the base drive is re-applied to the transistor. This means that when ILc does reach zero, we arrive back at the same conditions we had at the beginning of stage 1; ie the transistor is on, the current in Lc is zero and the voltage across Lc is the line voltage (150V).

TV Operating Principle

In a television set, or a computer monitor, the picture information is written onto the screen one line at a time. Each of these horizontal lines of picture information is written onto the screen by scanning the screen from left to right with an electron beam. This electron beam is produced by a gun situated at the back of the tube, and it is accelerated towards the screen by a high potential (typically 25kV). The beam is deflected from left to right magnetically, by varying the current in a set of horizontal deflection coils positioned between the gun and the screen.

The screen is phosphor coated, and when the high energy electron beam strikes the phosphor coating the phosphor gives off visible light. The density of electrons in the electron beam can be varied: phosphor brightness depends on beam density, and so the instantaneous brightness of the scanning spot can be varied at a fast rate as each line of picture information is written onto the screen. A set of vertical deflection coils deflect the beam vertically at the end of each horizontal scan and so lines of picture information can be built up, one after the other. The vertical deflection frequency (or *field rate*) for European sets is 50 Hz (alternate line scanning, giving 25 complete screens of information per second).

With no current in the horizontal deflection coils, the magnetic field between them is zero and so the electron beam hits the centre of the screen. With a negative current in the coils , the resultant magnetic field deflects the electron beam to the left side of the screen. With a positive coil current the deflection is to the right.

Now consider the characteristic deflection waveforms, Fig. 3. The current ILc represents the current in the horizontal deflection coils. During the period where the current in the deflection coils is ramping linearly from its peak negative value to its peak positive value, the electron beam is scanning the screen from left to right. This is the scan time, Tscan.

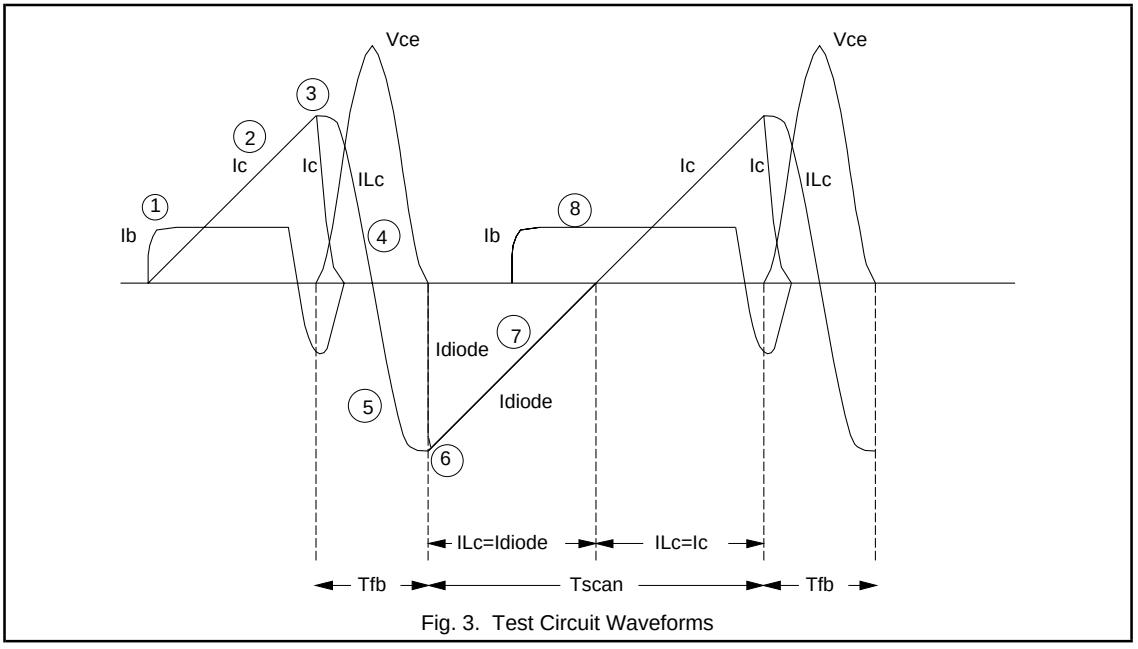


Fig. 3. Test Circuit Waveforms

During the period where the horizontal deflection coil current flows into the flyback capacitor, and then back into the coil (the half cosine curve at the end of the scan period), the electron beam is rapidly moving from the right side of the screen to the left. This is called the flyback period, Tfb, and no information is written onto the screen during this part of the cycle.

S-Correction

The actual TV horizontal deflection circuit differs from the test circuit in a number of ways that improve the picture quality. The simplified deflection circuit shown in Fig. 1 can be redrawn as shown in Fig. 4 where Lc is the horizontal deflection yoke and Cs is charged to the line voltage (150V).

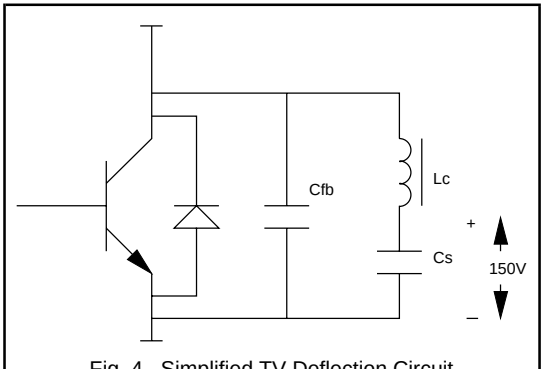


Fig. 4. Simplified TV Deflection Circuit

The advantage of this arrangement is that, by carefully selecting the value of Cs, one form of picture distortion is corrected for as follows.

The front of the TV tube is flat, rather than curved, and so during each horizontal scan the electron beam travels a greater distance to the edges of the screen than it does to the middle. A linear deflection coil current would tend to over deflect the beam as it travelled towards the edges of the screen. This would result in a set of 'equidistant' lines appearing on the screen as shown in Fig. 5 below.

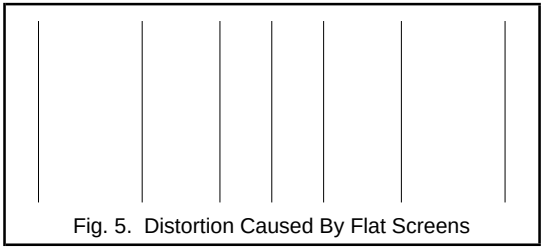


Fig. 5. Distortion Caused By Flat Screens

The voltage on the capacitor, Cs, will be modulated by the deflection coil current, ILc. When the diode is in forward conduction and the current in Lc is 'negative', the voltage on Cs will rise as Cs becomes more charged. When the transistor is conducting and the current in Lc is 'positive', the voltage on Cs will drop as Cs discharges. This is shown in Fig. 6 below.

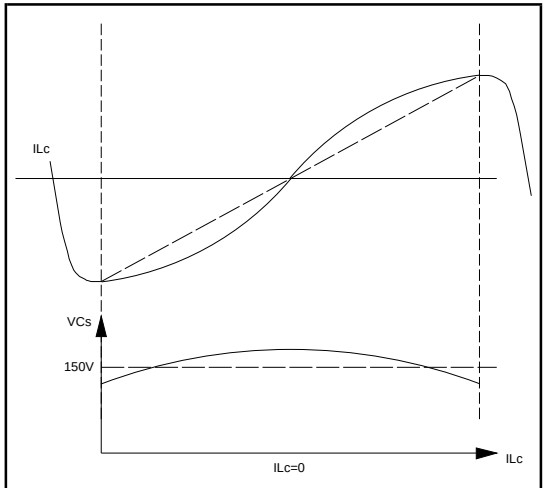


Fig. 6. S-Correction

This will give an 'S' shape to the current ramp in the deflection coils which corrects for the path difference between the centre and the edge of a flat screen tube. Hence the value of the capacitor, Cs, is quite critical. Cs is known as the S-correction capacitor.

Linearity Correction

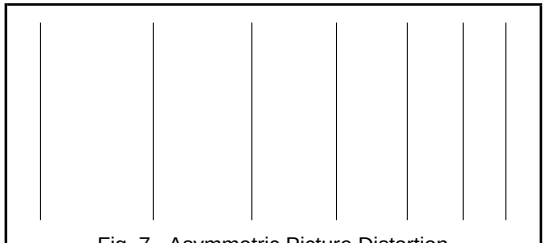


Fig. 7. Asymmetric Picture Distortion Caused by Coil Resistance

The voltage across the deflection coil is also modulated by the voltage drop across the series resistance of the coil. This parasitic resistance (RLc) causes an asymmetric picture distortion. A set of 'equidistant' vertical lines would appear on the screen as shown in Fig. 7. The voltage across the coils is falling as the beam scans the screen

from left to right. The beam, therefore, travels more slowly towards the right side of the screen and the lines are drawn closer together, see Fig. 8.

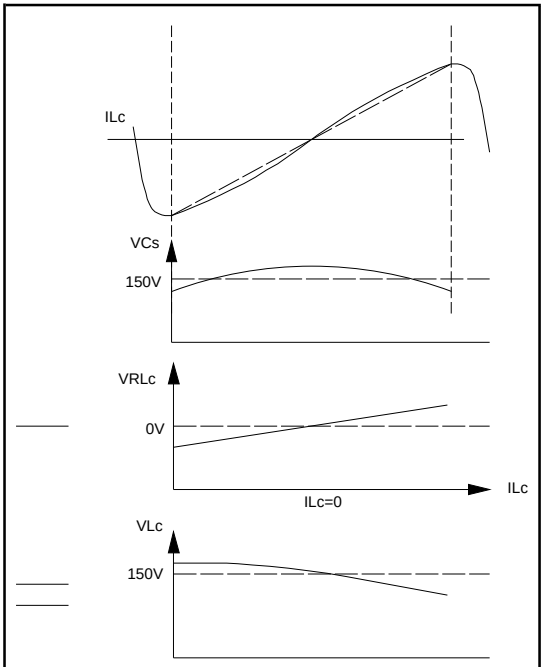


Fig. 8. Effect of Coil Resistance on Voltage Across Coil

VRLc is the voltage drop across the resistive component of Lc. Subtracting this from the voltage across Cs (VCs) gives the voltage across the inductive component on the deflection coils (VLc). To compensate for the voltage drop across the parasitic coil resistance we need a component with a negative resistance to place in series with the coil. This negative resistance effect is mimicked by using a saturable inductance, Lsat, in series with the deflection coils as shown in Fig. 9 below.

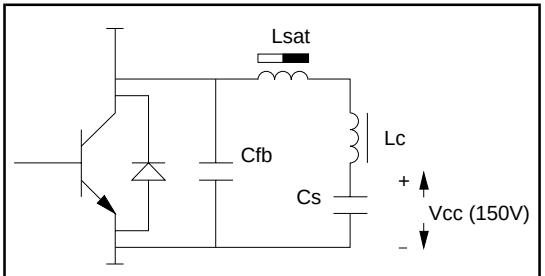


Fig. 9. Position of Saturable Inductor in Circuit

For an inductor with a low saturation current, the relationship between inductance and current is as shown in Fig. 10. As the current is increased much above zero, the core saturates and so the inductance drops. This happens if the current is conducted in either direction.

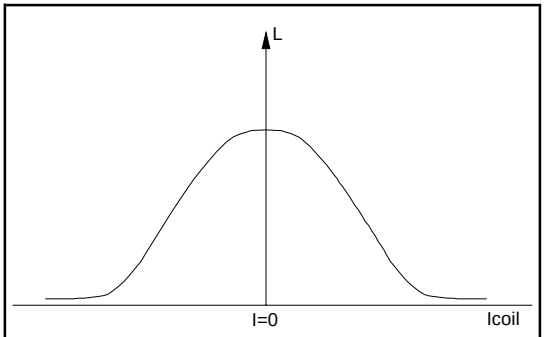


Fig. 10. L/I Characteristic of a Saturable Inductance

By taking a saturable inductance and premagnetising the core, we add a dc bias to this characteristic as shown in Fig. 11 below.

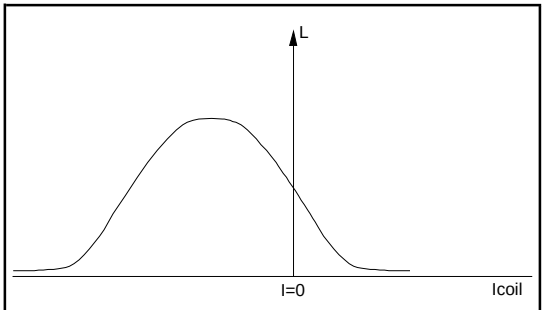


Fig. 11. DC Shift Produced by Premagnetised Core

Since Lsat has a much lower inductance than Lc, the dI/dt through Lsat is governed by the deflection coils, and is therefore dILc/dt. The voltage drop across Lsat is therefore given by V = Lsat•dILc/dt. During the scan time, Tscan, dILc/dt is approximately constant in value, and so the voltage/current characteristics of Lsat during the scan time are as shown in Fig. 12 below.

This is the characteristic required and so the voltage developed across Lsat, the linearity correction coil, compensates for the series resistance of the deflection coils.

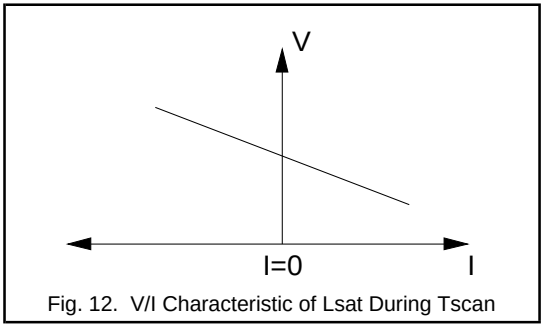


Fig. 12. V/I Characteristic of Lsat During Tscan

Cs Losses

So the circuit shown in Fig. 9 now gives the desired deflection waveforms. The electron beam scans the screen at a uniform rate on each horizontal scan. However, the circuit is not lossless and unless Cs is kept topped up the dc voltage on Cs, Vcc, will gradually decay. To prevent this from happening a voltage supply can be added across Cs but this introduces other problems.

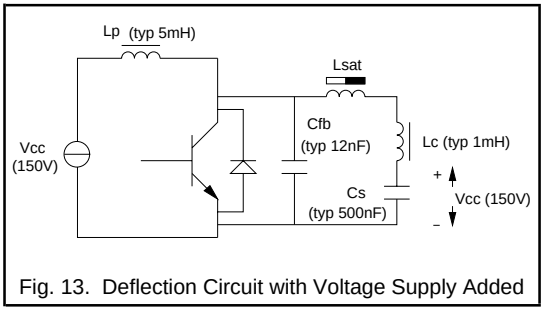


Fig. 13. Deflection Circuit with Voltage Supply Added

The average voltage across Lc *must* be zero. A dc voltage across Lc would generate a dc current which would produce a picture shift to the right. Applying Vcc directly to Cs would result in a dc current component through the deflection coils, so Cs must be charged to Vcc by some other way. Applying Vcc to Cs via the deflection coils overcomes this problem.

A large choke inductance, Lp, in series with the Vcc supply is necessary to prevent an enormous increase in the current through the power switch. Without it the Vcc supply would be shorted out every time the transistor was turned on. Typically the arrangement shown in Fig. 13 will result in a 20% increase in the current through the power switch and the power diode.

East-West Correction

So to recap on the circuit so far: the series resistance of the deflection coils is compensated for by the linearity correction coil, Lsat, and the varying length of the electron beam path, as the beam scans the screen from left to right, is compensated for by the S-correction capacitor, Cs. This capacitor modulates the voltage across the deflection coils during each horizontal scan, modulating the magnetic field ramp between them, and thus keeping the speed at which the electron beam scans the screen constant.

However, as the picture information is written onto the screen, by writing one line of information after another, a further variation in the length of the beam path is introduced as the beam scans the screen from top to bottom. The length of the beam path to the edge of the screen is shorter when the central lines of picture information are being written than it is when the lines at the top or the bottom of the screen are being written.

This means that a higher peak magnetic field is required to deflect the beam to the screen edges when the beam is writing the central lines of picture information, than that required to deflect the beam to the screen edges when the lines of picture information at the top and bottom of the screen are being written.

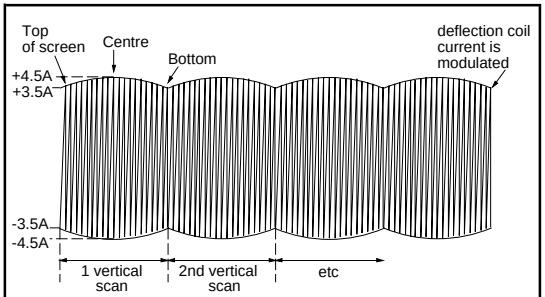


Fig. 14. Modulation of the Peak Deflection Coil Current

This requires increasing the peak deflection coil current gradually over the first half of each vertical scan, and then reducing it gradually over the later half of each vertical scan (see Fig. 14). This is done by modulating the voltage across the deflection coils. This process is known as east-west correction.

The line voltage, Vcc, is supplied by a winding on the SMPS transformer. This voltage is regulated by the SMPS and during the operation of the TV set it is constant.

In order to achieve the required modulation of the voltage across the deflection coils, a simple linear regulator could be added in series with Lp. One disadvantage of this solution is that it increases the circuit losses.

The Line Output Transformer (LOT)

The horizontal deflection transistor serves another purpose as well as deflecting the beam: driving the line output transformer (LOT). The LOT has a number of low voltage outputs but its primary function is to generate the EHT voltages to accelerate and focus the electron beam.

Fortunately, this function can be combined with a feature previously described as a cure for Cs losses; the inductive choke, Lp. The LOT has a large primary inductance that serves the purpose of Lp so a separate choke is not required, see Fig. 15 below.

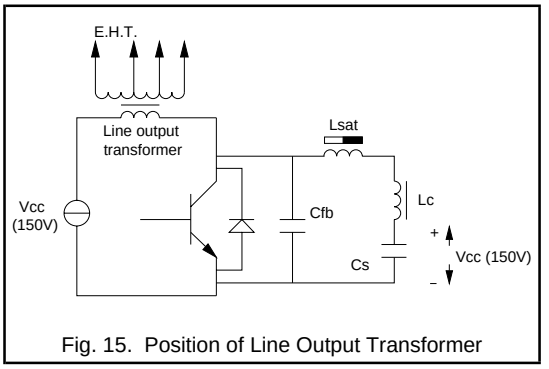


Fig. 15. Position of Line Output Transformer

A lot of power may be drawn from the LOT but the deflection must not be affected. In order to keep the secondary windings of the LOT at fixed voltages, we need to keep the voltage across the primary winding fixed. Therefore, the requirements for the LOT and a regulated supply to Lp are in conflict.

'Real' and 'Dummy' Deflection Circuits

As a way around this problem, consider a 'dummy' deflection circuit in series with the 'real' deflection circuit. This enables one circuit to meet the requirements for deflection, including east-west correction, and the dummy circuit meets the requirements for the LOT, see Fig. 16.

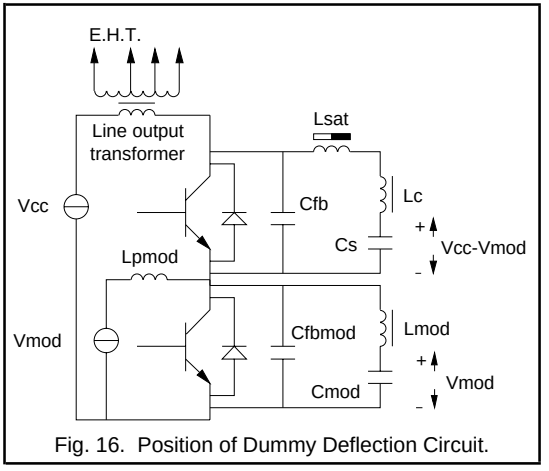


Fig. 16. Position of Dummy Deflection Circuit.

The two deflection circuits operate in direct synchronisation. Vmod is a voltage between zero and 30V that controls the east-west correction. Thus we can vary the voltage across the deflection coils in the 'real' deflection circuit without varying the voltage across the primary of the LOT in the 'dummy' circuit.

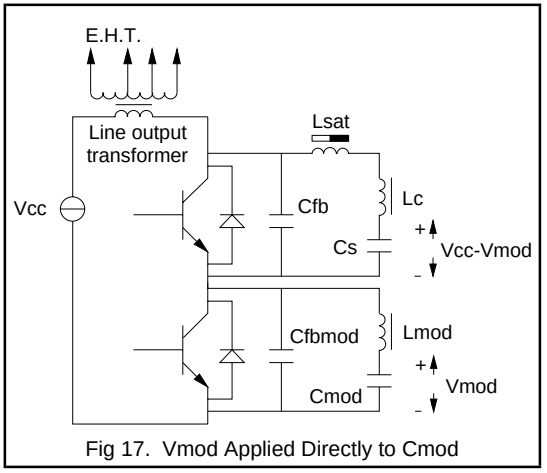


Fig 17. Vmod Applied Directly to Cmod

For proper flyback tuning, the 'real' and 'dummy' deflection circuits and the LOT must be tuned to the same flyback frequency. The two deflection circuits are tuned through careful selection of the flyback capacitors. In the case of the LOT the capacitance of the windings provides the necessary capacitance (typically 2nF) for correct tuning.

Since Lmod is only an inductor and not a real deflection component, a net dc current through it is not a problem. Therefore, we can apply Vmod directly to Cmod and this way reduce the component count by removing Lpmod, see Fig. 17.

Lmod is a quarter of the value of Lc. Cfbmod is four times as big as Cfb. Cmod is not critical as long as it is large enough to supply the required energy.

Suppose there is no voltage supplied externally to Cmod. The supply voltage, Vcc, will split according to the ratio of the impedances of the two circuits. In fact, the Vcc will split according to the ratio of the two flyback capacitors, Cfb and Cfbmod, as shown in Fig. 18.

The average voltage across Cfbmod will automatically be 30V (for Vcc = 150V), if no external voltages are applied to the 'dummy' circuit. Consequently, Cmod will become charged to 30V. The two deflection circuits are always operating in direct synchronisation. Under the condition where Vmod is 30V the currents in the two circuits would also be equal.

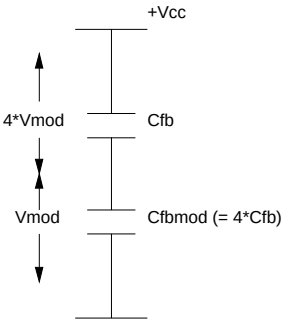


Fig. 18. Average Voltage Across the two Flyback Capacitors.

The range of Vmod required is 0 to 30V. Vmod is reduced below 30V as current is drawn from Cmod. An external supply to Cmod is never needed. This is the arrangement used in practice.

To draw current from Cmod a series linear regulator is added across Cmod as shown in Fig. 19.

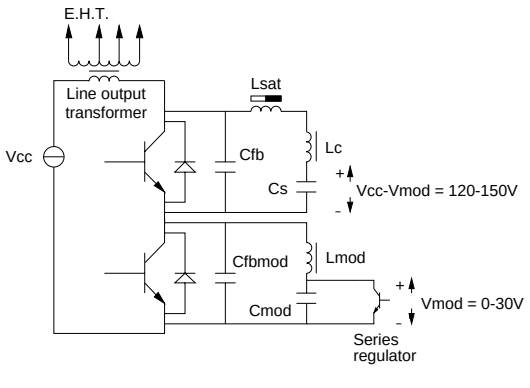


Fig. 19. Series Regulator Controlling Vmod

Diode Modulator Circuit

The circuit is now quite close to an actual TV horizontal deflection circuit. As the two transistors are switching in perfect synchronisation this circuit can be simplified further by removing one transistor, as shown in Fig. 20. This arrangement makes no difference to the operation of the circuit.

The circuit in Fig. 20 now shows all the features of the horizontal deflection diode modulator circuit. These features should be distinguishable when studying actual circuit diagrams.

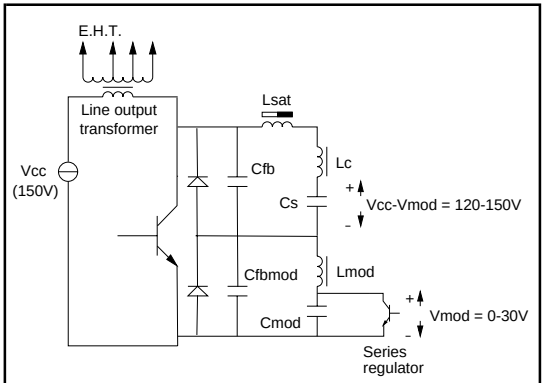


Fig. 20. The diode modulator circuit

Diode Modulator: Upper Diode

First consider the voltage requirements. In this respect, the worst case conditions for the upper diode are when Vmod = 0V. Under these conditions the upper diode must support the full flyback voltage. Therefore, the peak voltage limiting value on the upper diode must match the V_{CES} limit of the transistor.

Now consider the current requirements. With no circuit losses, the currents in the diode and the transistor are as shown in Fig. 21 where Ic is the transistor current and Idiode is the diode current. Of this current, 80% flows in the deflection coils and 20% flows in the LOT primary.

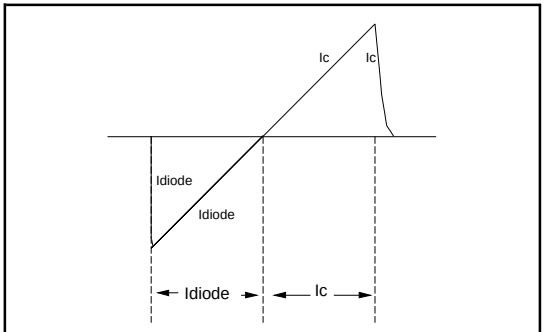


Fig. 21. With no load, Ic and Idiode are equal.

With circuit losses included, the transistor current will exceed the diode current. Circuit losses add a dc component to the waveform shown in Fig. 21. The loading on the LOT contributes a further dc component, increasing the transistor current and reducing the diode current still further, Fig. 22.

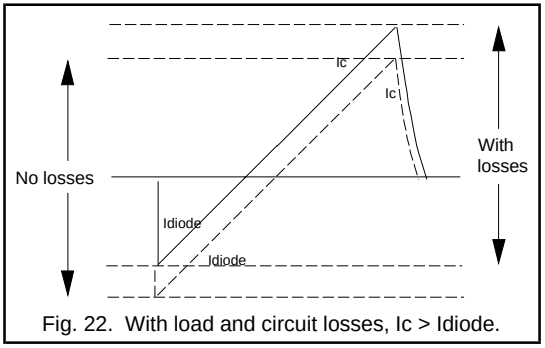


Fig. 22. With load and circuit losses, Ic > Idiode.

For example, for a current which is 12A peak to peak, 10A of this will be deflection current and 2A will be LOT current. With no load, the peak diode current would be equal to the peak transistor current, ie both would equal 6A. However, the LOT requires 1A dc in order to power the secondary windings. This makes the peak diode current 5A and the peak transistor current 7A. These are practical values for a 32 kHz black line S (ie EHT = 30kV) TV set.

The diode must conduct the full current immediately after the flyback period. Until the *forward* recovery voltage of the diode has been reached the diode cannot conduct. A high forward recovery voltage device would impede the start of the scan. If once the forward recovery voltage has been reached the device takes a long time before falling to its V_F level then the voltage across the deflection coils would be non-linear and, therefore, cause picture distortion. For a 32 kHz set the diode must recover to less than 5V in under 0.5µs.

Diode Modulator: Lower Diode

First consider the voltage requirements. At one extreme, all the flyback voltage is across the top diode and at the other extreme, the worst case condition for the lower diode is when the flyback voltage is split between the two diodes in the ratio 4:1 (ie when Vmod is at its maximum value of 30V). The voltage limiting value on the lower diode is, therefore, usually given as one quarter of the rating of the top diode. So, if the transistor is 1500V, the top diode is also 1500V and the bottom diode is 400V.

However, it is not uncommon for fault conditions to occur in TV circuits that cause large voltage spikes on the lower diode. To accommodate such occurrences, a 600V device is often used as the lower diode.

Now consider the current requirements. The lower diode must take the same current as the horizontal deflection coil, Fig. 23, and so its current requirement is the same as that of the top diode.

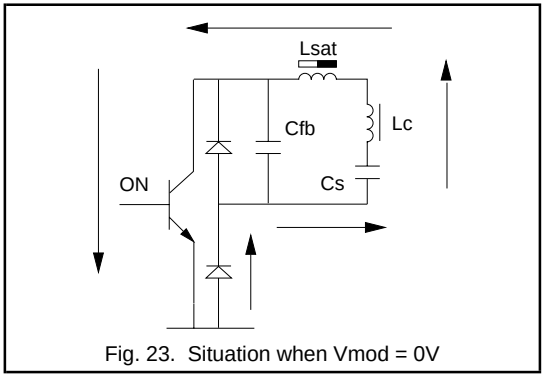


Fig. 23. Situation when Vmod = 0V

As shown in Fig. 23, the lower diode is conducting its peak current immediately before the flyback period and switches off as the transistor. Therefore, the *reverse* recovery of the lower diode must be very fast to minimise circuit losses.

Diode Modulator Circuit Example

Putting the above diode requirements into the circuit of Fig. 20 enable a typical 16 kHz TV horizontal deflection circuit to be constructed, see Fig. 24. This circuit is representative of a modern 25" TV design. The deflection transistor, BU2508A, will run with a peak I_C of 4.5A at 16 kHz. The combined inductance and capacitance will produce a flyback pulse of typically 1200V peak and 13µs width. The upper diode, BY228, has the same current and voltage capability as the deflection transistor. The lower diode, BYW95C, has the same current capability but a reduced voltage rating. More often than not, 600V devices are used as the lower diode with 1500V upper diodes.

The dc supply comes from the TV SMPS circuit. The SMPS will use a power switch also, typically BUT11AF in 16 kHz TV. A transformer will provide all the high power dc supplies required for the TV. For a 150V supply a high voltage diode will be used in the output stage, typically BY229-600. The LOT generates the EHT to accelerate the electron beam, typically a voltage of 25kV is produced.

In smaller TV's (14-21") this circuit could be much simplified. For smaller screen sizes EW correction is not essential and the diode modulator is not usually present. The circuit now uses a single diode and capacitor. The diode can be incorporated in the deflection transistor, for example, the BU2508D. Also for the smaller screen sizes it is common that the tube technology allows for lower flyback voltages. In these applications the 1000V BUT11A and BUT12A are often used.

In larger 16 kHz TV's (28" and above) and all 32 kHz TV's the axial diodes will not normally be capable in terms of current handling. These diodes are replaced by devices in TO220 type power outlines: BY359 for the upper diode and

BY229-600 or BYV29-500 for the lower diode. Also larger deflection transistors are available: BU2520A and BU2525A.

The same sort of scaling is also applicable to monitor deflection circuits. All monitors tend to use 1500V deflection transistors and upper diodes. The BU2508D (ie with diode) is often used so that the BY228 can be used as the upper diode. Using a D-type deflection transistor takes some current from the diode modulator but does not affect the operating principle. For the high frequency (up to 82 kHz), multi-sync monitors BU2522A and BU2527A deflection transistors are used. Above 64 kHz the BY459 is used as an upper diode.

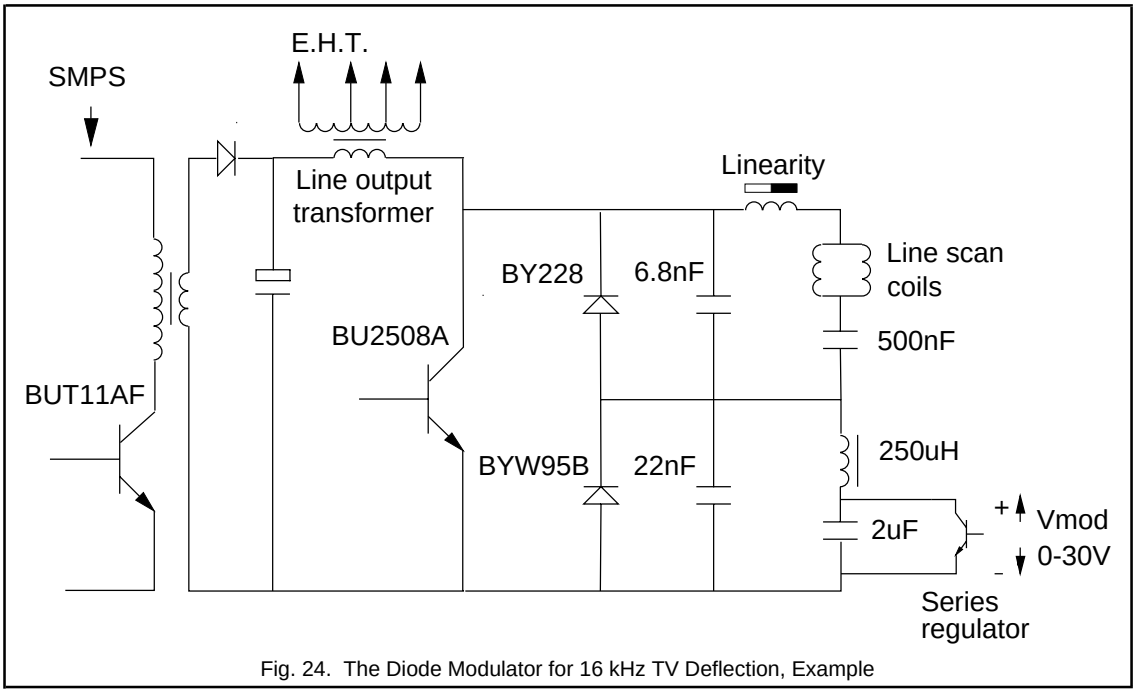


Fig. 24. The Diode Modulator for 16 kHz TV Deflection, Example

4.1.2 The BU25XXA/D Range of Deflection Transistors

Introduction

The BU25XXA range forms the heart of Philips Semiconductors 1500V power bipolar transistors. This technology offers world class dissipation in its target application of 16 kHz TV horizontal deflection circuits. The range has been extended for state-of-the-art large screen TV (8 A, 32 kHz) and all the volume monitor applications (up to 6 A, 64 kHz). The successful application of the BU25XXA range in all sectors of TV & monitor horizontal deflection has proved it to be a global technology.

As a further improvement, the BU25XXD range of devices have been introduced. Using BU25XXA technology, horizontal deflection transistors incorporating base-emitter resistive damping and a collector-emitter damper diode have been produced. The devices in this range are specifically aimed at the small-screen 16 kHz TV and 48 kHz monitor applications where the use of a D-type device can offer a significant cost-saving. The D-types offer the same performance as the A-type equivalent with only slightly increased dissipation, at a similar cost.

Specification Notes

The I_{Csat} value defines the peak current reached in a horizontal deflection circuit during normal operation for which optimum performance is obtained. Unlike other specification points, it is not necessary to inset this value in a real application. Operation either much above or below the specified I_{Csat} value will result in less than optimum performance. For higher frequencies the I_{Csat} should be lowered to keep the dissipation down.

The V_{CESM} value defines the peak voltage applied under any condition. The BU25XXA/D range could operate under continuous switching to 1500V in a deflection circuit without any degradation to performance but exceeding 1500V is neither recommended nor guaranteed. In normal running the peak flyback voltage is typically 1150V but a 1500V device is required for fault conditions.

The storage time, t_s, and fall time, t_f, limits are given for operation at the I_{Csat} value and the frequency of operation given by the application limit.

The BU25XXA Range Selection Guide

	Specification				Application	
Device	I_{Csat}	V_{CESM}	t_s	t_f	TV	Monitor
BU2508A/AF/AX	4.5 A 4.0 A	1500 V 1500 V	6.0 µs 5.5 µs	600 ns 400 ns	≤ 25", 16 kHz -	- 14", SVGA, 38 kHz
BU2520A/AF/AX	6.0 A	1500 V	5.5 µs 4.0 µs	500 ns 350 ns	≤ 29", 16 kHz ≤ 28", 32 kHz	15", SVGA, 48 kHz
BU2525A/AF/AX	8.0 A	1500 V	4.0 µs	350 ns	≤ 32", 32 kHz	(17", 64 kHz)
BU2522A/AF/AX	6.0 A	1500 V	2.0 µs	250 ns	-	15", 64 kHz
BU2527A/AF/AX	6.0 A	1500 V	2.0 µs	200 ns	-	17", 64 kHz

The BU25XXD Range Selection Guide

	Specification				Application	
Device	I_{Csat}	V_{CESM}	t_s	t_f	TV	Monitor
BU2506DF/DX	3.0 A	1500 V	6.0 µs	500 ns	≤ 23", 16 kHz	-
BU2508D/DF/DX	4.5 A	1500 V	6.0 µs	600 ns	≤ 25", 16 kHz	14", SVGA, 38 kHz
BU2520D/DF/DX	6.0 A	1500 V	5.5 µs	500 ns	≤ 29", 16 kHz	15", SVGA, 48 kHz

Application Notes

The applications given in the selection guide should be seen as an indication of the limits that successful designs have been achieved for that device type. This should help in the selection of a device for a given application at the design concept stage. For example, a 15" monitor requiring operation up to 6 A at 64 kHz could use either a BU2522A or BU2527A. If the design has specific constraints on switching and dissipation then the BU2527A is the best option, but if cost is also a prime consideration then the smaller chip BU2522A could be used with only slightly degraded performance. For an optimised design the BU2525A can be used in 17", 64 kHz applications but the BU2527A is the recommended choice.

Outlines

Philips Semiconductors recognise both the varying design criteria and the market availability of device outlines and this is reflected in the range of outlines offered for the BU25XXA/D range. Three different outlines are offered for the devices available, one non-isolated (SOT93) and two isolated/full-pack designs (SOT199, TOP3D). The outline is defined by the last letter in the type number, for example:

BU2508A	SOT93	non-isolated
BU2508AF	SOT199	isolated
BU2508AX	TOP3D	isolated

All three outlines are high quality packages manufactured to Philips Total Quality Management standards.

The Benefits of the D-type

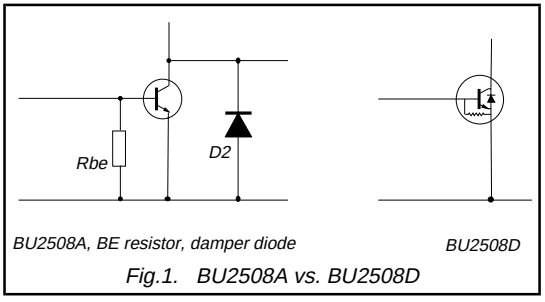


Fig.1. BU2508A vs. BU2508D

The BU2508D technology incorporates the damper diode and a base-emitter damping resistor, see Fig.1. In the target 16 kHz applications the damper diode is usually an axial type (eg. BY228), the D-type deflection transistor incorporates this device in a monolithic structure. This presents a significant cost-saving in the application. The base-emitter resistor eliminates the need for external damping at the transistor base-emitter. The only consideration for replacing an A-type with a D-type is that the base current required for optimised switching is slightly higher for the D-type.

For higher currents and frequencies where diode modulator circuits are used it appears at first that use of the D-types is not possible. However, this is not so; D-type transistors can be used WITH diode modulators in a beneficial way. For example, a 15", 48 kHz SVGA monitor utilising a diode modulator is at the borderline between an axial upper damper diode and a TO220 type. The dissipation is such that if an axial diode is used some sort of thermal management may be necessary. By using a D-type transistor some of the current is taken by the diode in the D-type relieving the discrete upper damper device. Use of a D-type in this way has allowed an axial diode to be used in place of a TO220 type making a significant cost saving.

Causes of Dissipation

In the cycle of operation there are four distinct phases: turn-on, on, turn-off, off. Each phase is a potential cause of dissipation. Of course, for enhanced circuit performance dissipation in the deflection transistor must be minimised.

a) Turn-on. The primary function of a deflection transistor is to assist in the sweep of the beam across the screen of the display, ie to horizontally deflect the beam. As the deflection transistor turns-on the beam is scanning from just less than half way across. At mid-screen the beam is un-deflected, ie the deflection current is zero. So, the deflection transistor turns on with a small negative collector current, I_C ramping up through zero. At turn-on there are no sudden severe load requirements that cause significant dissipation. In horizontal deflection turn-on dissipation is negligible.

b) On-state. As the beam is deflected from the centre of the screen to the right - hand side the I_C increases as determined by the voltage across the deflection coil. The resulting voltage drop across the deflection transistor, V_{CE} depends not only on this I_C but also on the base drive: for high I_B the V_{CE} will be low; for low I_B the V_{CE} will be high. For high I_B the transistor is said to be overdriven giving low on-state dissipation. For low I_B the transistor is said to be underdriven giving higher on-state dissipation.

c) Turn-off. Turn-off starts when the forward I_B is stopped. This is followed 2 - 6 µs later (depending on the device and application) by the I_C peaking. This delay is called the storage time, t_s of the device. During this time the V_{CE} rises as the current rises causing increased dissipation: the longer t_s the higher the dissipation. As the I_C peaks so scanning ends and the process of flyback begins. Now, as the I_C falls (in time t_f, the fall-time) the V_{CE} rises to the peak flyback voltage; this a phase of high dissipation.

Turn-off is the dominant loss phase for all deflection transistors. The device characteristics in this phase are of much interest to the TV & monitor design engineers.

d) Off-state. In an optimised drive circuit the device will be off for V_{CE} above 250V in flyback. For the rest of the flyback the collector-emitter is reverse biased while the base-emitter will also be reverse biased: between -1 to -4V. Any leakage through the device will be the cause of dissipation. For the BU25XXA/D range, low-contaminant processing ensures that the bulk leakage is very low. Also, the long-established Philips glass passivation has very low leakage. The device characteristics coupled with the low pulse width and duty cycle of the flyback mean that the losses in the off-state are negligible.

In a D-type deflection transistor there is an additional cause of dissipation:

e) Diode Conduction. At the end of flyback the next scan will start. As the flyback voltage goes negative so the diode conducts, this clamps the voltage on the flyback capacitor. The fixed voltage provides a fixed ramp in current through the deflection coil and through the diode; the beam sweeps from the left towards the centre of the screen. At, or near, the centre this current approaches zero ending the diode conduction phase. The dissipation here is dominated by two characteristics of the diode: the forward recovery and the on-state voltage drop. This can be a significant cause of dissipation in a D-type transistor.

The effect of both underdrive and overdrive on the device is increased device dissipation and hence increased junction temperature. In general, the higher the junction temperature the shorter the lifetime of the device in the application. Optimised drive circuit design and good thermal management can bring the device junction temperature down to well below the limit T_{jmax}. Such considerations enhance the reliability of the deflection transistor in the application. It is essential that care is taken at the design stage to optimise the base drive for the device product spread.

Dynamic Testing

The BU25XXA/D range is assessed in a deflection switching test circuit designed to simulate the most demanding running conditions of the application. The horizontal deflection coils, which form the major part of the collector load, are represented by a variable inductance Lc and the flyback and diode modulator circuits by a single diode, BY228 and variable capacitance, Cfb. For BU2508A/AF/AX TV applications the test circuit is shown in Fig.2 below.

This circuit generates the characteristic deflection waveforms, Fig.3, from which the storage time, fall time and energy loss at turn-off can be measured. These parameters define the device performance in the application.

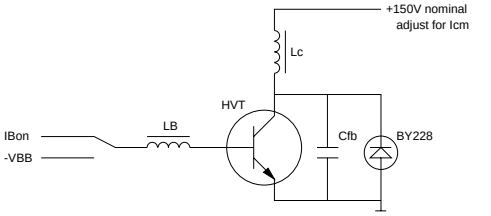


Fig.2. BU2508A/AF/AX 16 kHz Deflection Switching Test Circuit

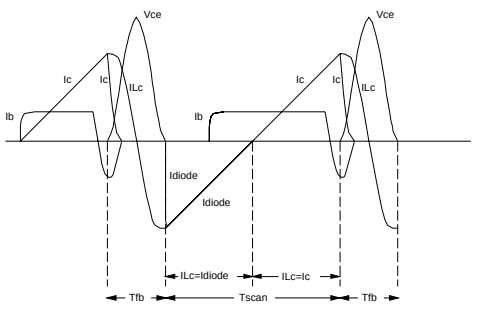


Fig.3. Deflection Switching Waveforms

It is not valid to do a single-shot test for the switching parameters as the characteristics of the nth pulse depend on the previous (n-1)th pulse. To achieve this the tester works in a double pulse mode.

'Bathtub' Curves

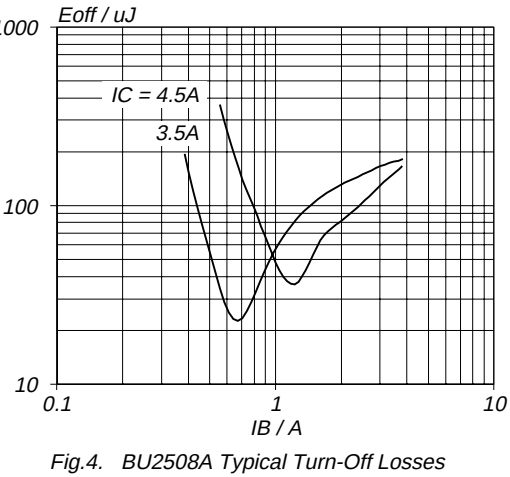


Fig.4. BU2508A Typical Turn-Off Losses - 'Bathtub' curve

A plot of base current, I_B, against turn off dissipation, Eoff, for one BU2508A measured in the switching test circuit at a peak collector current of 4.5A gives the characteristic 'bathtub' shape shown in Fig.4 above. From this curve the tolerance to base drive variations can be assessed and the optimum I_B determined for a given I_C.

The switching performance is also determined by the peak reverse base current at switch off. For a typical h_{FE} device, of all types in the BU25XXA/D range, a peak reverse base current, I_{Boff}, equal to one half the typical peak I_C is recommended for optimum dissipation. This is largely determined by the drive transformer and is usually difficult to be fine-tuned. In the typical non-simultaneous base drive circuit the level of forward base current, I_B, is easily controlled, hence, the presentation of the turn-off losses versus I_B.

The 'bathtub' curves are plotted for a reverse base voltage at turn-off of -4V. This level of reverse base drive is recommended for the BU25XXA/D range as it reduces the risk of any noise, or ring, forward biasing the base-emitter during flyback. However, in well-engineered designs the BU25XXA/D can operate just as well with a reverse base voltage at turn-off of only -1V. This tolerance to base drive is very useful to design engineers.

On the far left of the curve, at low I_B values, the device is severely underdriven resulting in a high turn off dissipation. As the base drive is increased the degree of underdrive is reduced and the device remains in saturation for a larger proportion of its on time. This is the reason for the initial decrease in Eoff with increasing I_B seen in the 'bathtub' curve. Eventually, the optimum drive is reached and the turn off dissipation, Eoff, is at its minimum value. Increasing the base drive still further results in overdrive and the appearance of an I_C tail at turn off. The result of this, as can be seen in the 'bathtub' curve, is increasing turn off losses with increasing I_B.

Typically, this curve has steep sides and a flatter central portion; this gives it the shape of the cross-section through a bathtub, hence the name 'bathtub' curve !

The BU25XXA/D technology gives a sharper looking curve but a much lower level of Eoff/Poff than competitor types. For optimised drive the BU25XXA/D technology offers world class dissipation in 16 kHz TV deflection circuits.

Process Control

The success of the BU25XXA/D range has enabled significant enhancements to be made to the benefit of both our customers and ourselves. By utilising a continuous cycle of quality improvement coupled with high volume production, Philips Semiconductors can demonstrate their excellent process control in specified h_{FE} and dissipation limits. This control is achieved by manufacturing capability rather than test selections. This process control improves manufacturing throughput and yield and, hence, customer deliveries. The improvements in manufacturing result in higher process capability indices enabling the introduction of tightened internal test specifications.

Critical Parameter Distribution Fact Sheets

Industry standard data sheets for all power semiconductor devices offer an introduction to the device fundamentals and can usually be used for a quick comparison between competitor types. Detailed use of a specific device requires much more information than is contained in any data sheet. This is particularly relevant to high voltage bipolar transistors, and especially horizontal deflection transistors. A horizontal deflection transistor is only as good as the base circuit that drives it. The growth of power MOSFET's is mainly due to the difficulties in driving bipolar transistors. However, MOSFET technology is not suitable for horizontal deflection applications, Philips Semiconductors are actively involved in supplying the support tools necessary for the successful design-in of their BU25XXA/D range.

Recognising the designers requirements Philips Semiconductors now provide critical parameter distribution fact sheets for the BU25XXA/D range. This additional data should be used in conjunction with the data sheets to give a full picture of the device capabilities and characteristics over the production spread.

The fact sheets give limit curves for the power dissipation in the device caused by turn-off, P_{off}, at a given operating frequency and range of load current, I_C all at 85˚C (a typical operating temperature for TV and monitor applications). These curves provide limits to the typical 'bathtub' curves given in data. It is important to recognise that these fact sheet curves represent the LIMIT of production when comparing the BU25XXA/D range with competitor types which offer this information as TYPICAL only, if at all. This information displays the technical performance of the device and the measurement capability available.

Contained in the fact sheets is evidence of the world class dissipation limits obtained by the BU25XXA/D range. As an example, the BU2508A/AF/AX 'bathtub' limit curves are shown in Figs.5-7.

These fact sheets also contain limit h_{FE} curves for V_{CE} = 1 V and 5 V at three different temperatures: -40˚C, 25˚C, and 85˚C. The range of temperatures chosen reflects the range of customer requirements. These limit curves define the device characteristics for all the important extremes of operation. As an example the BU2508A/AF/AX limit h_{FE} curves for V_{CE} = 1 V and 5 V at 25˚C are shown in Figs.8-9 below. The 100% test points are indicated by arrows.

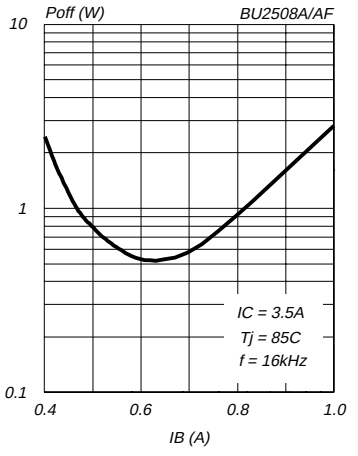


Fig.5. BU2508A/AF/AX
Max. P_{off} vs. I_B
for I_C = 3.5 A @ 85˚C

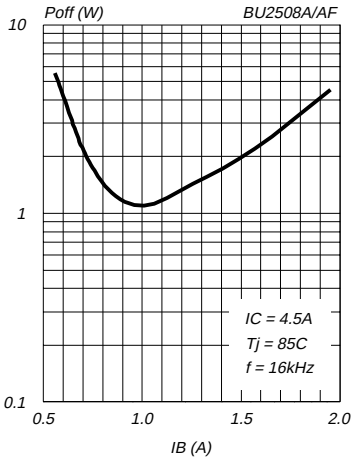


Fig.6. BU2508A/AF/AX
Max. P_{off} vs. I_B
for I_C = 4.5 A @ 85˚C

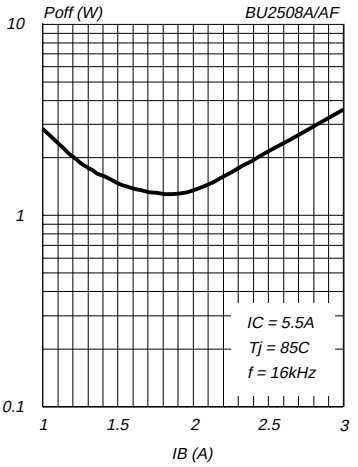


Fig.7. BU2508A/AF/AX
Max. P_{off} vs. I_B
for I_C = 5.5 A @ 85˚C

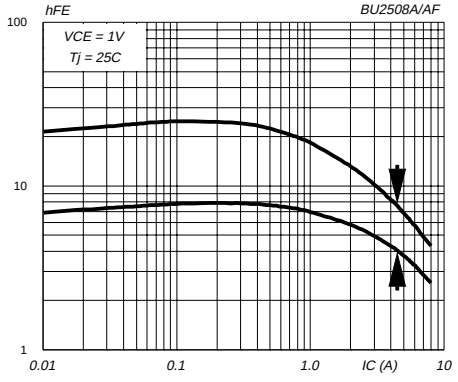


Fig.8. BU2508A/AF/AX h_{FE} vs I_C @ 1 V, 25˚C

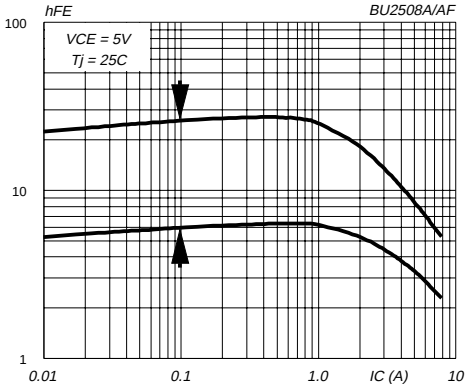


Fig.9. BU2508A/AF/AX h_{FE} vs I_C @ 5 V, 25˚C

Drive Circuits

It was stated previously that a horizontal deflection transistor is only as good as the base circuit that drives it. Philips Semiconductors address this problem by providing fact sheets with an example of a drive circuit for the target applications. The drive circuits presented are of the industry standard non-simultaneous base drive type utilising commercially available Philips components. An example of these drive circuits is shown for the BU2508A in Fig.10 below.

This drive circuit is not an end in itself but a means to an end: it produces the waveforms at the base that enable the load set by Vcc, Lc and Cfb to be switched most efficiently. For this reason the waveforms produced by this circuit are also presented in the fact sheet. Again, for the BU2508A example given above the waveforms are shown in Figs.11-15 below.

The drive circuit employed in the application could be quite different to the one given above in Fig.10 but the base drive waveforms in Figs.11 & 13 must be replicated for optimised switching.

The fundamental concept of the non-simultaneous base drive is well established in the TV and monitor industry for driving the horizontal deflection transistor. Individual designs, however, can differ significantly. A different transformer design may enable the required base current to be generated without the addition of Lb and D1, Rb. Driving Rp from a low voltage supply could reduce the cost by allowing a low voltage transistor, Q1 and capacitor, Cd to be used.

The resistor Rbe is necessary to eliminate any overshoot in the Vbe at the end of the base-emitter avalanche that could turn the transistor on during flyback. Such an event would lead to an early failure of the transistor by exceeding the forward biased safe-operating area (FBSOA). In circuits operating at higher frequencies resistive damping alone is usually not sufficient and RC damping is required.

In this application, the BU2508A could be replaced by the BU2508D in the circuit of Fig.10. This would allow the BY228 and Rbe resistor to be removed from the circuit.

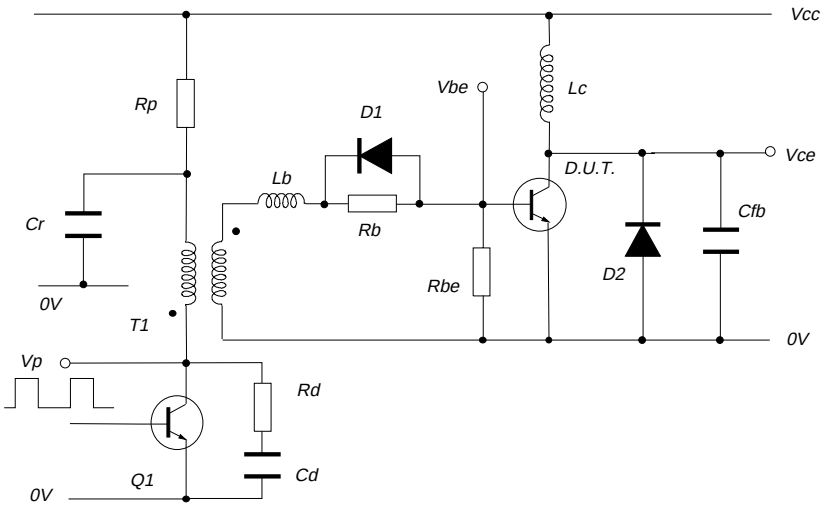


Fig.10. BU2508A 4.5 A, 16 kHz Drive Circuit

Components and values: Rp = 1 kΩ, 2 W; Cr = 100 nF; Rd = 560 Ω; Cd = 470 pF, 500 V; Q1 Philips BF819; T1 Philips AT4043/87 Transformer; Lb = 0.5 μH; Rb = 0.5 Ω, 0.5 W; D1 Philips BYV28-50; Rbe = 50 Ω; Lc = 1 mH; Cfb = 12 nF, 2 kV; D2 Philips BY228; Vcc = 115 V.

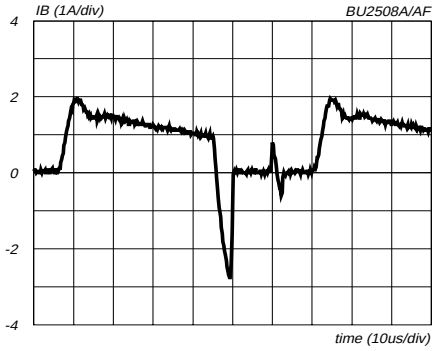


Fig.11. BU2508A/AF I_B vs. time

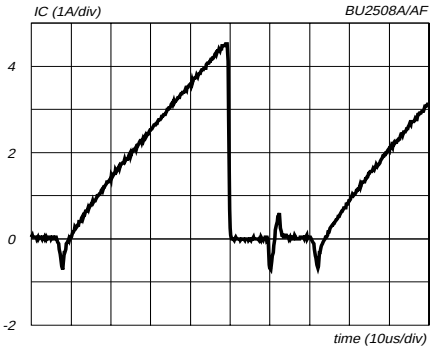


Fig.12. BU2508A/AF I_C vs. time

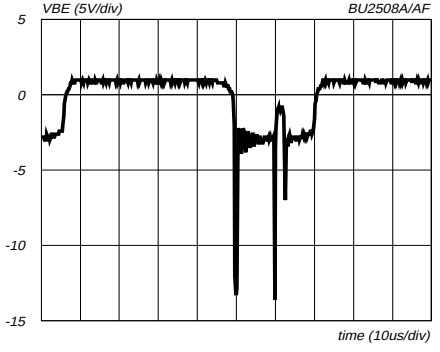


Fig.13. BU2508A/AF V_{BE} vs. time

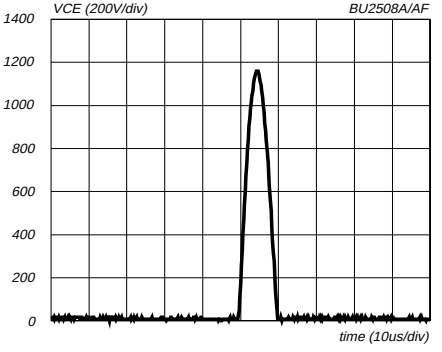


Fig.14. BU2508A/AF V_{CE} vs. time

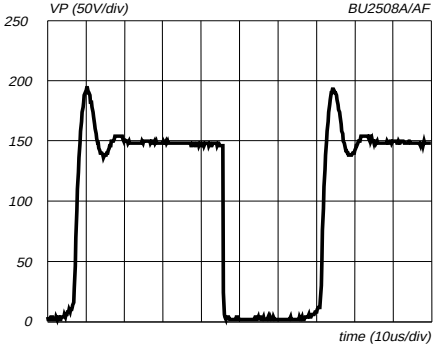


Fig.15. V_P vs. time

$I_{B(end)}$ = 0.9 - 1.1 A; I_{Cmax} = 4.5 ± 0.25 A;

$|- I_{B(off)}| \geq$ 2.0 A;

V_{CEmax} = 1100 - 1200 V

4.1.3 Philips HVT's for TV & Monitor Applications

This section simplifies the selection of the power switches required for the SMPS and horizontal deflection in TV and monitor applications. Both high voltage bipolar transistors and power MOSFET devices are included in this review. As well as information specific to the Philips Semiconductors range of devices, general selection criteria are established.

HVT's for TV & Monitor SMPS

The vast majority of television and monitors have switch mode power supplies that are required to generate an 90 - 170V supply for the line deflection stage, plus a number of lower voltage outputs for audio, small signal etc. By far the easiest and most cost effective way of fulfilling these requirements is to use a flyback topology. Discontinuous mode operation is generally preferred because it offers easier control and smaller transformer sizes than continuous mode.

For the smaller screen size TV's, where cost is a dominant factor, bipolar HVT's dominate. For large screen TV and monitors power MOSFET's are usually chosen.

The peak voltage across the switching transistor in a flyback converter is twice the peak dc link voltage *plus* an overshoot voltage which is dependent on the transformer leakage inductance and the snubber capacitance. Thus, for a given mains input voltage there is a minimum voltage requirement on the transistor. Increasing the transformer leakage and/or reducing the snubber capacitance will increase the minimum voltage requirement on the transistor.

a) Power MOSFET's

For TV's operating just with 110/120V mains applications a device which can be used with peak voltages below 400V is required. For these applications the power MOSFET is used almost exclusively. A wide variety of 400V power MOSFET's are available, leading to lower device costs, which coupled with the easier drive requirements of the MOSFET make this an attractive alternative to a bipolar switch.

For 220/240V and, more recently, for universal input mains applications where an 800V device is generally required the cost of power MOSFET was prohibitive. However, improvements both in circuit design and device quality has meant that a 600V device can be used in these applications.

Philips Semiconductors have a comprehensive range of powerMOS devices for these applications. The main parameters of these devices most applicable to TV and monitor SMPS applications are summarised in Table 1.

Part Number	V_{DSS}	$R_{DS(ON)}$	@ I_D
BUK454-400B	400 V	1.8 Ω	1.5 A
BUK455-400B	400 V	1.0 Ω	2.5 A
BUK457-400B	400 V	0.5 Ω	6.5 A
BUK454-600B	600 V	4.5 Ω	1.2 A
BUK455-600B	600 V	2.5 Ω	2.5 A
BUK457-600B	600 V	1.2 Ω	6.5 A
BUK454-800A	800 V	6.0 Ω	1.0 A
BUK456-800A	800 V	3.0 Ω	1.5 A
BUK438-800A	800 V	1.5 Ω	4.0 A

Table 1. Philips PowerMOS HVT's for TV & Monitor SMPS Applications

The V_{DSS} value is the maximum permissible drain-source voltage of the powerMOS in accordance with the Absolute Maximum System (IEC 134). The $R_{DS(ON)}$ value is the maximum on-state resistance of the powerMOS at the specified drain current, I_D.

b) Bipolar HVT's

Bipolar HVT's still have an important role in TV SMPS applications. Many new TV designs are slight improvements on existing designs incorporating a new control or signal feature (eg Fastext, SCART sockets) which do not demand the re-design of the SMPS. If there has been a good experience with an existing SMPS it is not surprising that these designs should continue in new TV models.

For 220/240V mains driven flyback converters, generally, a 1000V bipolar HVT is used. The full voltage capability of the transistor can be used as the limit under worst case conditions but it must never be exceeded. In circuits where the transformer leakage inductance is high, and voltages in excess of 1000V can occur, a device with a higher voltage handling capability is required.

Philips Semiconductors have a comprehensive range of bipolar HVT devices for these applications. The main parameters of these devices most applicable to TV SMPS applications are summarised in Table 1.

Part Number	V_{CESM}	V_{CEO}	I_{Csat}	V_{CEsat}
BUX85	1000 V	450 V	1 A	1.0 V
BUT11A	1000 V	450 V	2.5 A	1.5 V
BUT18A	1000 V	450 V	4 A	1.5 V
BUT12A	1000 V	450 V	5 A	1.5 V
BUW13A	1000 V	450 V	8 A	1.5 V
BU506	1500 V	700 V	3 A	1.0 V
BU508A	1500 V	700 V	4.5 A	1.0 V

Table 2. Philips Bipolar HVT's for TV SMPS Applications

The V_{CESM} value is the maximum permissible collector-emitter voltage of the transistor when the base is shorted to the emitter or is at a potential lower than the emitter contact. The V_{CEO} value is the maximum permissible collector-emitter voltage of the transistor when the base is open circuit. Both voltage limits are in accordance with the Absolute Maximum System (IEC 134). The V_{CEsat} value is the maximum collector emitter saturation voltage of the transistor, measured at a collector current of I_{Csat} and the recommended base current.

c) Selection procedures

Some simple calculations can be made to establish the device requirements. The first requirement to be met is that the peak voltage and current values are within the capabilities of the device. For a flyback converter the peak voltage and current values experienced by the power switch are given by the equations in Table 3.

Peak voltage across the device	$(2 \times V_{s(\max)}) + \sigma$
Peak device current	$2 \times \frac{P_{th}}{\delta_m \times V_{s(\min)}}$

Table 3. Peak Voltage and Current in a Flyback Converter.

where:

$V_{s(max)}$ = maximum dc link voltage
σ = voltage overshoot due to transformer leakage
$V_{s(min)}$ = minimum dc link voltage
P_{th} = throughput power of SMPS
δ_m = maximum duty cycle of SMPS

Note: in this example, the throughput power is equal to the input power less the circuit losses up to the power switch.

MOSFET or bipolar?

The main factors influencing this decision are ease of drive and cost, given the limitation on percentage of throughput power which can be dissipated in the power switch. MOSFETs require lower drive energy and less complicated drive circuitry. They also have negligible switching losses below 50 kHz. However, large chip sizes are required in order to keep on state losses low (especially as breakdown voltage is increased). Thus the larger chip size of the MOSFET is traded off against its capacity for cheaper and easier drive circuitry and higher switching frequencies.

For 110/120V mains driven TV power supplies the 400V MOSFET dominates. At 220/240V there is a split between bipolar and power MOSFET

Which MOSFET?

The optimum MOSFET for a given circuit can be chosen on the basis that the device dissipation must not exceed a certain percentage of throughput power. Using this as a selection criterion, and assuming negligible switching losses, the maximum throughput power which a given MOSFET is capable of switching is calculated using the equation;

$$P_{th(\max)} = \frac{3 \times \tau \times V_{s(\min)}^2 \times \delta_{\max}}{4 \times R_{ds(125C)}}$$

where:

$P_{th(max)}$ = maximum throughput power
δ_{max} = maximum duty cycle
τ = required transistor loss (expressed as a fraction of the output power)
$R_{ds(125C)}$ = $R_{DS(ON)}$ at 125˚C
$V_{s(min)}$ = minimum dc link voltage

A transistor loss of 5% of output power gives a good compromise between device cost, circuit efficiency and heatsink size (ie τ = 0.05)

Note that the $R_{DS(ON)}$ value to be used in the calculation is at 125˚C (a practical value for junction temperature during normal running). The $R_{DS(ON)}$ specified in the device data is measured at 25˚C. As junction temperature is increased the $R_{DS(ON)}$ increases, increasing the on state losses of the MOSFET. The extent of the increase depends on the device voltage, see Fig. 1.

For 400V MOSFET's $R_{ds(125C)}$ = 1.98 x $R_{DS(ON)}$ @ 25˚C, where $R_{DS(ON)}$ @ 25˚C is the value given in device data.

For 800V MOSFET's $R_{ds(125C)}$ = 2.11 x $R_{DS(ON)}$ @ 25˚C.

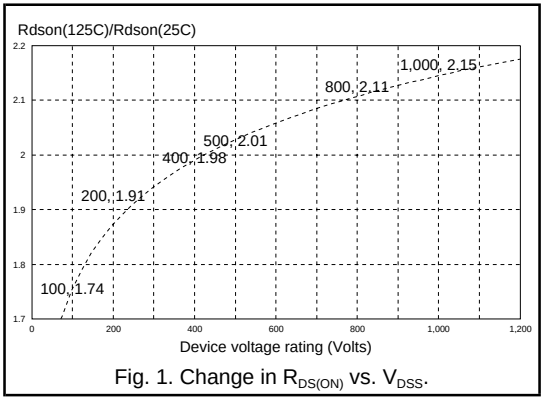


Fig. 1. Change in $R_{DS(ON)}$ vs. V_{DSS}.

Which bipolar?

For maximum utilisation of a bipolar transistor it should be run at its data I_{Csat}. This gives a good compromise between cost, drive requirements and switching losses. Using this as a selection criterion the maximum output power which a given bipolar transistor is capable of switching is calculated using the equation;

$$P_{th(\max)} = \delta_{\max} \times V_{s(\min)} \times \frac{I_{Csat}}{2}$$

where: $P_{th(max)}$ = maximum throughput power
δ_{max} = maximum duty cycle
$V_{s(min)}$ = minimum dc link voltage
I_{Csat} = I_{Csat} in transistor data

d) Selection table

Using the selection procedures just discussed, and the device data given previously, the following selection table of suitable devices for flyback converters of various output powers has been constructed.

Output Power	110/120V (ac) mains	220/240V (ac) mains
50 W	BUK454-400B	BUK454-600B BUK454-800A BUX85
100 W	BUK455-400B	BUK455-600B BUK456-800A BUT11A/BU506
150 W	BUK457-400B	BUK457-600B BUK438-800B BUT12A/BU506
200 W	BUK457-400B	BUK438-800A BUW13A/BU508A

Table 4. Power Switch Selection Table

HVT's for TV & Monitor Horizontal Deflection

This application is one of the few remaining applications which is entirely serviced by bipolar devices. The technology is not yet commercially available to provide MOSFET or IGBT devices for this application. A horizontal deflection transistor is required for each TV and monitor employing a standard cathode ray tube display.

The deflection transistor is required to conduct a current ramp as the electron beam sweeps across the screen and then withstand a high voltage peak as the beam flies back before the next scan starts. The peak current and voltage in the application define the device required. In addition to this, the deflection transistor is required to switch between the peak current and peak voltage states as quickly and efficiently as possible. In this application the switching and dissipation requirements are equally as important as the voltage and current requirements.

Standard TV switches at a frequency of 16 kHz, rising to 32 kHz for improved definition TV (IDTV). In the future, high definition TV (HDTV) will switch between 48 and 64 kHz.

Standard VGA monitors switch at 31 kHz, rising to 48 kHz for SVGA. However, many other (as yet unnamed) modes exist for PC monitors and work stations, extending up to 100 kHz switching frequencies.

Vertical deflection is much lower in frequency (50 to 70 Hz) and will not be discussed as this uses lower power devices (typically 150V / 0.5A).

a) Voltage and Current Requirements

For a given scan frequency the voltage and current requirements of the horizontal deflection transistor are not fixed. However, the suitable transistors are all linked by the relationship;

$$I_{Csat} \times V_{CESM} = constant$$

The derivation of this law is as follows:

The horizontal deflection angle (typically 110°) covered in a given time is proportional to the magnetic field sweep between the horizontal deflection coils. This is in turn proportional to the product of the number of turns on the deflection coils and the peak to peak current. The average current in the deflection coils is zero and hence the peak positive current in the coils is half the peak to peak current. These relationships yield the following equation;

$$B \propto n \times I$$

where:

B = magnetic field sweep between the horizontal deflection coils
n = number of turns on the horizontal deflection coils
I = peak positive current in the horizontal deflection coils

The inductance of the horizontal deflection coils, L, is proportional to the square of the number of turns, ie

$$L \propto n^2$$

Combining these two equations gives

$$B^2 \propto L \times I^2$$

and so for a given deflection angle and horizontal scan frequency, and therefore a given B, L x I^2 is a constant.

For a given deflection frequency the flyback time is also fixed. Flyback time is related to the deflection coil inductance, L, and the flyback capacitance, C, by the equation

$$t_{fb} \propto \sqrt{L \times C}$$

During the flyback period the energy in the deflection coils ($1/2.LI^2$) is transferred to the flyback capacitor and so the voltage across the flyback capacitor rises. Assuming all the energy is conserved during this transfer, the increase in voltage across the flyback capacitor, δV, is given by

$$\frac{1}{2} \times L \times I^2 = \frac{1}{2} \times C \times \delta V^2$$

So, if LI^2 is a constant then $C\delta V^2$ is a constant also. Therefore, as LC is a constant so is $(I\delta V)^2$. So we have:

$$\delta V \times I = constant$$

δV is the voltage rise across the flyback capacitor due to the energy transferred from the deflection coils during the flyback period. The peak voltage across the flyback capacitor, V_{peak}, is given by

$$V_{peak} = \delta V + V_{CC}$$

where: V_{CC} = line voltage (typically +150 V)

The flyback capacitor is positioned across the collector emitter of the horizontal deflection transistor. Therefore, the peak voltage across the flyback capacitor is also the peak voltage across the collector - emitter of the deflection transistor.

In order to protect the transistor against overload conditions (eg picture tube flash) a good design practice is to allow V_{CEpeak} to be 80% of the V_{CESM} rating. V_{CC} is generally around 10% of the V_{CEpeak} (in order to obtain the correct ratio of scan time to flyback time). This gives

$$V_{CESM} \geq 1.25 \times \delta V + 190$$

All the positive current in the horizontal deflection coils is conducted by the horizontal deflection transistor. However, this is not the peak current in the transistor. The transistor is normally also required to conduct the current in the primary of the line output transformer (LOT). Typically, this will increase the peak current in the deflection transistor by 40%. For optimum deflection circuit design the peak current in the transistor will be its I_{Csat} rating, ie

$$I_{Csat} = 1.4 \times I$$

Therefore, for a given deflection angle and a given horizontal scan frequency the horizontal deflection circuit can be designed around any one of a number of devices. However, the suitable devices are all linked by the equation

$$I_{Csat} \times V_{CESM} = constant$$

Summary

For a given horizontal deflection angle and horizontal scan frequency

$$V_{CESM} \geq 1.25 \times \delta V + 190$$
$$I_{Csat} = 1.4 \times I$$
$$I_{Csat} \times V_{CESM} = constant$$
$$L \times I^2 = C \times \delta V^2 = constant$$

where:

V_{CESM} = maximum voltage rating of the horizontal deflection transistor
I_{Csat} = I_{Csat} rating of the horizontal deflection transistor
δV = voltage rise on the flyback capacitor due to the energy transfer from the horizontal deflection coils
I = peak positive current in the horizontal deflection coils
L = inductance of the horizontal deflection coils
C = value of flyback capacitance

These relationships apply only for the assumptions declared previously.

b) Switching and Dissipation Requirements

In TV, for a given scan frequency the minimum on time of the transistor is well defined. For 16 kHz systems the transistor on time is not less than 26 μs and for 32 kHz systems it is not less than 13 μs. This enables the required storage time of the transistor to be well defined. For 16 kHz systems a maximum storage time of 6.5 μs is the typical requirement. For 32 kHz systems the required maximum storage time is typically 4.0 μs. For higher frequencies the required maximum storage time is reduced still further.

In monitor applications, especially multi frequency models, the on time is not well defined. There are many different frequency modes and several control ic's giving different duty cycles. However, it can be said that the higher the frequency, the shorter the storage time required.

Storage time in the circuit can always be reduced by turning the transistor off harder. However, this eventually leads to a collector current tail at turn off and as a consequence the turn off dissipation increases. Turn off dissipation accounts for the bulk of the losses in a deflection transistor and it is crucial that this is kept to a minimum. The deflection transistor must be tolerant to drive and load variations if it is to achieve a low turn off dissipation because the east - west correction on larger screen television sets means that circuit conditions are not constant. Turn off can be optimised during the design phase by ensuring that the peak reverse base current is roughly half of the peak collector current and the negative base drive voltage is between 2 and 5V.

Turn on performance is not a critical issue in deflection circuits. At turn on of the deflection transistor the I_C is low, the V_{CE} is low and, therefore, the dissipation is low. The actual turn on performance of the transistor has a negligible effect.

c) HVT's for Horizontal Deflection

The deflection circuit must satisfy any specified cost, efficiency and EMC requirements before it can be called acceptable. A very high voltage deflection transistor would allow a lower deflection coil current to be used, reducing the level of EM radiation from the deflection coils, but it would require a higher line voltage and it would also result in higher switching losses in the transistor. A very high deflection coil current would allow a lower voltage deflection transistor to be used and a lower line voltage. This would also yield lower switching losses in the deflection transistor. However, high currents in the deflection coils could lead to EMC problems, and the need to keep the resistive coil losses low would mean that thicker wire would have to be used for the windings. Above a certain point the skin depth effect makes it necessary to use litz wire.

For 16 kHz and 32 kHz applications the 1500V bipolar transistor has become the designers first choice, although many 16 kHz systems could work well using 1000V devices. However, concern over fault conditions that can cause odd high voltage pulses has seen 1500V adopted as the 'standard'. The collector currents involved range from 2.5A peak to 8A peak for TV and 3.5A peak to 7A peak for monitors. The transistors for these applications are now considered.

16 kHz applications

Table 5 lists the 1500V transistors for 16 kHz TV deflection systems and a summary of their main characteristics.

Part Number	V_{CESM}	I_{Csat}	Application
BU505/D	1500V	2A	Monochrome sets
BU506/D BU2506DF	1500V	3A	90˚ Colour; ≤ 23"
BU508A/D BU2508A/D	1500V	4.5A	110˚ Colour; 21-25"
BU2520A/D	1500V	6A	110˚ Colour; 25-29"

Table 5. Transistors for 16 kHz TV deflection

All of the above types are available in both non-isolated and isolated outlines (F-pack), except the BU2506DF - F-pack only. Isolated outlines remove the need for an insulating spacer to be used between device and heatsink. Devices are available both with and without a damper diode (eg without: BU505, BU2520A and with: BU505D, BU2520D). The BU2506DF is only available with a damper diode.

The BU25XX family is a recent addition to the range of Philips deflection transistors. Far from being just another 1500V transistor, the BU25XX has been specifically designed for horizontal deflection. By targeting the device for this very specialised application it has been possible to achieve a dissipation performance in deflection circuits which is exceptional.

The BU2520A uses the superior technology of the BU25XX family applied to a large chip area. The BU2508A has an h_{FE} of 5 at 5V V_{CE} and 4A I_C. The BU2520A has an h_{FE} of 5 at 5V V_{CE} and 6A I_C. This gives designers working on large colour television sets a high h_{FE} deflection transistor with a high current capability. The high h_{FE} reduces the forward base drive energy requirements. The high current capability enables the energy drawn from the line output transformer to be increased. Using a BU2520A device allows the EHT energy to be increased for brighter pictures (a feature of new 'black line' tubes) without having to increase the forward base drive energy to the deflection transistor.

32 kHz applications

Table 6 gives the 1500V transistors for 32 kHz deflection systems and a summary of their main characteristics.

Part Number	V_{CESM}	I_{Csat}	Application
BU2520A	1500V	6A	110˚ Colour; ≤ 28"
BU2525A	1500V	8A	110˚ Colour; ≤ 32"

Table 6. Transistors for 32 kHz deflection

For the foreseeable future 32 kHz TV will be concentrated at the large screen sector (≥ 25"). These TV's will employ diode modulator circuits lessening the need for D-type transistors. With a switching frequency twice that of conventional TV the dissipation in these devices will be higher. For this reason the non-isolated versions, with lower thermal resistance, will be prevalent in these applications.

Monitor applications

The applications given in Table 7 should be seen as an indication of the limits that successful designs have been achieved for that device type. This should help in the selection of a device for a given application at the design concept stage. For example, a 15" monitor requiring operation up to 6A at 64 kHz could use either a BU2522A, a BU2525A or a BU2527A. If the design has specific constraints on switching and dissipation then the BU2525A and BU2527A would be better. If, as well, a guaranteed RBSOA is required then the BU2527A is the best choice.

Table 7 gives the 1500V transistors for monitor deflection systems, concentrating on the common pc and industry standard work station modes.

Part Number	V_{CESM}	I_{Csat}	Application
BU2508A/D	1500V	4.5A	14", SVGA, 38 kHz
BU2520A	1500V	6A	15", SVGA, 48 kHz
BU2522A	1500V	6A	15", 64 kHz
BU2525A	1500V	8A	(17", 64 kHz)
BU2527A	1500V	6A	17", 64 kHz

Table 7. Transistors for Monitor deflection

All devices are available in non-isolated and isolated outlines. The excellent dissipation of this range of devices means that, even at monitor switching frequencies, devices in an isolated package can be used

4.1.4 TV and Monitor Damper Diodes

Introduction

Philips Semiconductors supply a complete range of diodes for the horizontal deflection stage of all volume TV and monitor applications. This note describes the range of Philips parts for the damper (also called efficiency) diode in horizontal deflection. The damper diode has some unusual application specific requirements that are explained in this section.

Damper diodes form an essential part of the horizontal deflection circuit. The choice of diode has an effect on the total circuit dissipation and the display integrity. A poor selection can lead to unnecessary power loss and a visible picture distortion.

As well as a full range of discrete devices for the damper diode application Philips offfer a range of horizontal deflection transistors with integrated damper diodes. These devices offer a cost and space saving, especially beneficial for high volume TV production.

Discrete Damper Diode Selection Guide

I_{FWM}, $I_{F(AV)}$. The quoted $I_{F(AV)}$ values do not correspond to any particular current in the application. The values are standard data format for selection purposes and comparison with competitor types. In general, the larger the $I_{F(AV)}$ the higher the deflection coil current and/or frequency in the application. A more meaningful specification is I_{FWM}, this refers to the peak operating current in a 16 kHz TV application given a standard current characteristic. The application columns in table 1 define the limit fitness for use of each diode.

V_{RSM}. The damper diode should have a voltage capability equal to the deflection transistor. In most applications this will be 1500V. The V_{RSM} value equates to the peak flyback voltage. The diode data should not be viewed as that for other diodes where it is quite common to use devices with V_{RSM} 5 or 10 times greater than the peak circuit voltage. Damper diodes will operate in horizontal deflection circuits with peak flyback voltages up to the specified limit. However, the limit V_{RSM} should not be exceeded in any circumstance. In practice, a device with V_{RSM} of 1500V will be found in applications with peak flyback voltages of 1300V in normal running; fault conditions do not usually see more than a 200V rise in flyback voltage.

Outline. The Philips range spans the available outlines for this application from axial to TO220 type. The SOD57 and SOD64 are hermetically sealed axial - leaded glass envelopes. These outlines combine the ability to house large chips with proven reliability and low cost. For high ambient temperatures with severe switching requirements the addtion of cooling fins may be necessary to achieve successful operation at the application limit.

For higher currents and frequencies there are devices in TO220 type outlines. TO220AC is a two-legged non-isolated outline. The pin-out is such that the tab is always the cathode. For an isolated equivalent outline there are SOD100 and the newer SOD113. The SOD100 is the traditional isolated TO220 outline allowing the device to be attached to a common heatsink without any separate isolation. The SOD113 is an enhanced version of SOD100 offering an improved isolation specification. Philips offer a complete range of mounting accessories for all these outlines.

	Specification			Application	
Device Type	I_{FWM},$I_{F(AV)}$	V_{RSM}	Outline	TV	Monitor
BY448	4 A	1650 V	SOD57	≤ 21", 16 kHz	-
BY228	5 A	1650 V	SOD64	25", 16 kHz	-
BY328	6 A	1500 V	SOD64	28", 16 kHz	14", SVGA, 38 kHz
BY428	4 A	1500 V	SOD64	21", 32 kHz	14", 64 kHz
BY359 BY359F(X)	10 A	1500 V	TO220AC SOD100 (SOD113)	36", 32 kHz	17", 64 kHz
BY459 BY459F	10 A	1500 V	TO220AC SOD100	HDTV	19", 1280x1024, 82 kHz

Table.1 Philips Semiconductors Damper Diode Selection Guide

Horizontal Deflection Transistors with Integrated Damper Diode

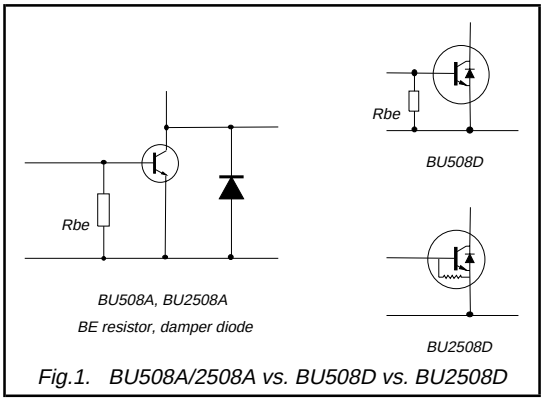


Fig.1. BU508A/2508A vs. BU508D vs. BU2508D

The range of devices available covers most high volume TV & Monitor applications where designers require a choice of devices to meet their requirements. The differences are shown in Fig. 1 above. These devices are all monolithic structures. The process of integrating the diode does not reduce the performance of the deflection transistor.

For traditional horizontal deflection circuits with a single damper diode it is easy to see the benefits of integrating the deflection transistor and damper diode. The additional dissipation in the integrated damper diode should be taken into account in the thermal management considerations. The use of the deflection transistor with integrated diode allows a simpler layout with lower component count and cost.

For circuit designs that employ a diode modulator circuit it is still quite common to employ a deflection transistor with an integrated damper diode. In these circuits the current is shared between the integrated diode and the discrete modulator damper diode. This technique allows smaller discrete diodes to be used or reduced thermal management for the discrete device. For example, this could allow the circuit designer to remove any cooling fins on an axial diode; or replace a TO220 type with a cheaper axial type of discrete diode in the modulator.

Table 2 below shows a selection of Philips Semiconductors' horizontal deflection transistors with an integrated damper diode.

I_{Csat}. This value is an indication of the peak collector current in a 16 kHz TV horizontal deflection circuit for which optimum dissipation and switching can be obtained. For the diode the I_{Csat} value should also be taken as the peak current (ignoring any instantaneous spikes at the start of scan). For higher frequency applications in monitors the I_{Csat} value reduces slightly.

V_{CESM}. The voltage capability of the deflection transistor and damper diode are the same. As for discrete devices, there is no need for excessive insets. The V_{CESM} value equates to the peak flyback voltage and, as for the V_{RSM} of a discrete damper diode, should not be exceeded under any circumstance.

Outlines. Devices are available in three different outlines, one non-isolated (SOT93) and two isolated/full-pack designs (SOT199, TOP3D). The outline is defined by the last letter in the type number, for example:

BU2508D	SOT93	non-isolated
BU2508DF	SOT199	isolated
BU2508DX	TOP3D	isolated

All three outlines are high quality packages manufactured to Philips Total Quality Management standards.

	Specification			Application	
Device Type	I_{Csat}	V_{CESM}	Outline	TV	Monitor
BU2506DF BU2506DX	3.5 A	1500 V	SOT199 TOP3D (SOT399)	21", 16 kHz	-
BU508D BU508DF	4.5 A	1500 V	SOT93 SOT199	21-25", 16 kHz	-
BU2508D BU2508DF BU2508DX	4.5 A	1500 V	SOT93 SOT199 TOP3D (SOT399)	21-25", 16 kHz	14", 38 kHz, VGA
BU2520D BU2520DF BU2520DX	6 A	1500 V	SOT93 SOT199 TOP3D (SOT399)	25-29" 16 kHz	14", 48 kHz, SVGA

Table 2 Philips Semiconductors Deflection Transistors with Integrated Damper Diode Selection Guide

Operating Cycle

The waveforms in Fig. 2 below show the deflection coil current and flyback voltage in a simplified horizontal deflection circuit. In Fig. 2 the damper diode current is highlighted. All the flyback voltage is applied across the damper diode. These waveforms are valid for both the traditional type of deflection circuit (Fig. 3) and the diode modualtor deflection circuit (Fig. 4).

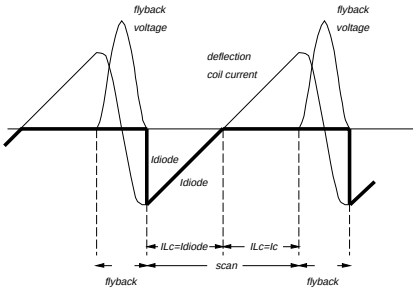


Fig. 2. Horizontal Deflection Damper Diode Operating Cycle.

During flyback the energy in the deflection coil, L_c is transferred to the flyback capacitor, C_{fb}. With the transfer of energy the voltage on C_{fb}, hence the voltage across the diode, rises sinusoidally until all the energy is transferred. Now the current in L_c is zero and the diode and C_{fb} are at the peak flyback voltage. The energy now transfers back to L_c. As the energy is transferred the voltage decreases until all the energy is back in L_c when there is no voltage across C_{fb}, and maximum current through L_c. If there was no diode present, this operation would continue with the energy transferring back to C_{fb} with the voltage continuing to decrease until all the energy in L_c had been transferred; the peak voltage now reversed. But with the damper diode in place across C_{fb} (see Figs. 3 & 4), as the voltage falls negative the diode will be forward biased and tend to conduct.

Consider now the application requirement which is to establish a peak negative current in Lc before the start of the next scan. As the decreasing voltage on C_{fb} tends to zero so the current in L_c reaches a peak negative value and the next scan can start. The transfer of energy into the capacitor has to be stopped during the scan, hence the addition of the damper diode.

Most TV & monitor display circuits will employ an element of over-scanning; this means at the start of diode conduction the beam will be off-screen. Over-scanning is introduced to reduce the effect of any spurious switching characteristics as the diode switches.

Power Dissipation

There are two significant factors contributing to power dissipation in a damper diode: forward recovery and on-state forward bias. Reverse recovery and reverse bias losses are negligible in this application. As a general rule, the total dissipation is half forward recovery and half forward bias. To explain this further we have to consider the operating cycle of the diode in detail.

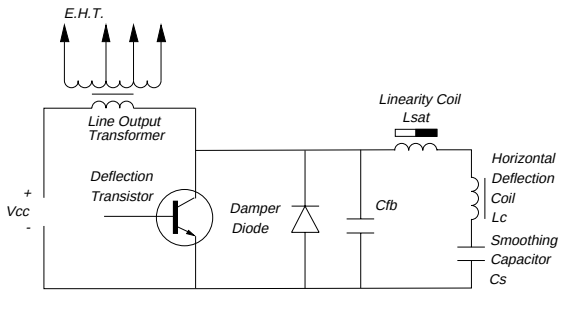


Fig. 3. Traditional Deflection Circuit.

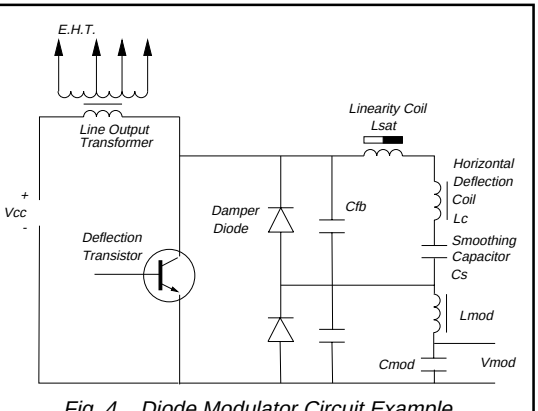


Fig. 4. Diode Modulator Circuit Example.

Forward Recovery. As the voltage goes negative the electric field builds up across the diode. The device design and process technology determine the point at which conduction starts. At the start of conduction the voltage is a maximum: the forward recovery voltage, V_{fr}. A detailed view of the damper diode voltage and current at the start of diode conduction is given in Fig. 5 below. As the current flows the voltage across the diode drops to its steady-state V_F value; the time this takes is called the forward recovery time, t_{fr}.

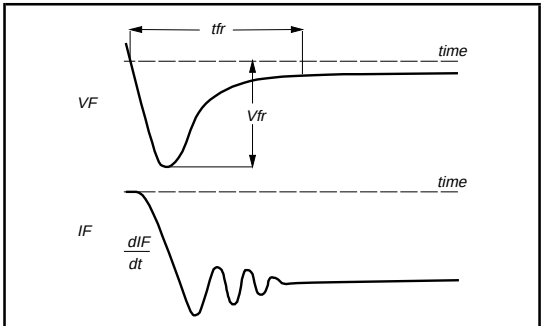


Fig.5. Damper Diode V & I Waveforms.

The values for V_{fr} and t_{fr} are application dependent. In general, V_{fr} is ≤ 20V; t_{fr} is ≤ 500ns for V_F to fall to 2V; and the rate of rise in diode current, dI_F/dt, will be between 25 - 90 A/µs. A 'good' damper diode will not only have low V_{fr} and low t_{fr} but as a result, it will also allow the current to switch to the diode faster, giving a higher dI_F/dt.

Forward Bias. As the beam scans from the left towards the centre the voltage drop across the diode is determined by the device V_F characteristic for a given L_c current. As the beam scans from left to right the diode current decreases.

Measurement of the V_F is not possible in the application. The best indication of the losses comes from the maximum hot V_F information contained in the datasheets.

Reverse Recovery & Reverse Bias. To the right of centre screen L_c current becomes positive and, hence, current no longer flows through the damper diode. In reverse recovery the damper diode does not experience any high current - high voltage characteristic that would be a cause of significant dissipation.

During flyback the diode is reverse biased, another possible cause of dissipation. The combined effects of reverse recovery and reverse bias are negligible in comparison to forward recovery and forward bias.

Picture Distortion

The diode does not start to conduct until the forward recovery voltage is approached: a device with a high forward recovery voltage, V_{fr}, will take longer to start conduction than a device with a low V_{fr}. A delay in the start of diode conduction means that the deflection coil current is dominated by the flyback capacitor, C_{fb} at the start of the scan. This can cause a visible distortion to the left-hand side of the display.

The voltage across the diode modulates the voltage across the coil. For a device with a long forward recovery time, t_{fr}, the diode forward recovery characteristics will affect the voltage across the deflection coil at the start of the scan. This can also cause a visible distortion to the left-hand side of the display.

For display circuit optimisation it is essential that the requirements for the damper diode are understood and taken into account in device selection.

TV Deflection Circuit Examples

4.2.1 Application Information for the 16 kHz Black Line Picture Tubes

With the introduction of the black line picture tubes new drive circuits are required. To have full benefits, the EHT voltage and beam current must be increased. This section describes the horizontal deflection and EHT generation. Some hints for vertical deflection and video amplifiers are given as well.

Summary

This section describes the horizontal deflection circuitry of the black line picture tube A66EAK022X11 and A59EAK022X11. To take full advantage of this new tube it must be driven at 27.5kV @ 1.3mA. This implies that in an ordinary combined EHT and deflection stage in the no load condition, zero beam current, the high voltage increases to about 29.5kV. The main change to this circuit, compared with existing circuits, is the line output transformer (AT2077/34) uses four layer DSB technology.

For the vertical deflection a minor modification on PCALE report ETV8831 is given. The video output stage suited to this tube is described in PCALE report ETV8811.

1. Introduction

One step in improving picture quality is the introduction of the black line picture tube. With this tube day-time TV viewing with a bright high contrast picture becomes possible. To achieve this the picture tube is provided with a dark screen and increased EHT power capability by means of an invar shadow mask.

When the 45AX black line picture tube is compared with the existing 45AX tubes the following modifications in the application must be made.

-Increase of the EHT power to 27.5kV @ 1.8mA beam current.

-Increase of the cut off voltage to 160V.

To cope with this high EHT power demand, a new line output transformer has been developed (AT2077/34). The main part of this section is dedicated to the horizontal deflection. For supply, vertical deflection and video amplifier details reference will be made to separate reports.

Special care is taken to suppress certain geometrical picture distortions which otherwise would become noticeable at the increased levels of dynamic EHT load variations. These distortions are the result of oscillations in the line output stage.

All measurements and circuits are based and tested on the 66FS picture tube. Since the 59FS tube is electrically identical to the 66FS tube this circuit is also suited for the 59FS picture tube. With some minor circuit modifications (component values) this circuit is also suited for 33" picture tubes.

2. Circuit Description

The horizontal deflection board is built up of four major parts, see Fig. 1.

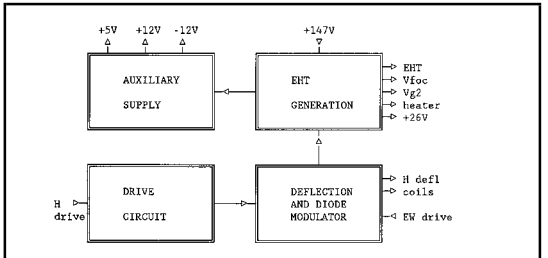


Fig. 1. Block Diagram of Horizontal Deflection Board.

In high end TV sets a lot of low voltage supply current is required. In this design a separate transformer in parallel to the line output transformer is foreseen for the generation of these auxiliary supplies. In applications where this auxiliary power is not required this part can be omitted by simply leaving out the additional transformer. The other parts of this horizontal deflection are more or less classic.

2.1 Drive Circuit

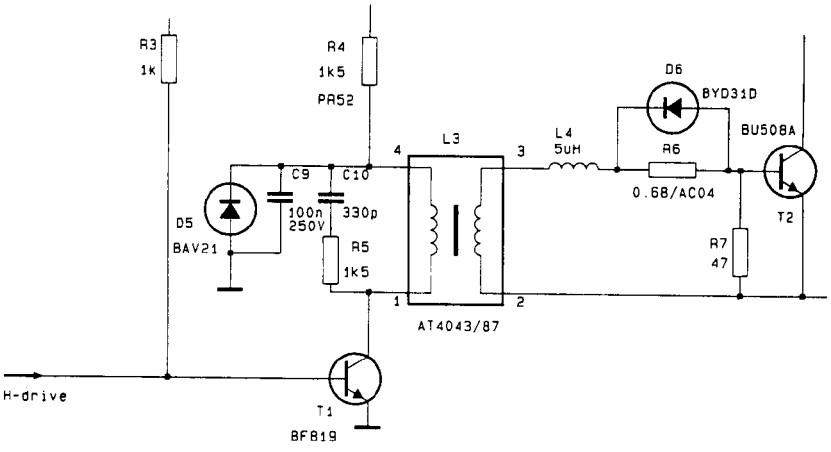


Fig. 2. Drive Circuit

The horizontal drive circuit is a classical transformer coupled inverting driver stage. When driver transistor T1 is conducting energy is stored in the transformer. When T1 is turned off the magnetising current continues to flow in the secondary side of the transformer thus turning on the deflection transistor. At this time the voltage on the secondary side of the driver transformer is positive ($V_{BE}+I_B$xR6). When the driver transistor turns on again this secondary voltage reverses and will start to turn off the deflection transistor. At the same time energy is stored in the transformer again.

During this turn off action the forward base drive current decreases with a controlled dI/dt, thereby removing the stored charge from the deflection transistor. The dI/dt depends on the negative secondary voltage and the leakage inductance. As a rule of thumb, the deflection transistor stops conducting when its negative base current is about half the collector peak current.

To prevent the deflection transistor from turning on during flyback due to parasitic ringing on the secondary side of the driver transformer a damper resistor is connected in parallel with the base emitter junction of the deflection transistor.

Also at the primary side of the driver transformer a damper network is added (R5 & C10) to limit the peak voltage on the driver transistor.

D5 is added for those applications where in the standby mode the deflection stage is turned off by means of continuous conduction of the driver transistor. The explanation is as follows:

When T1 is suddenly made to conduct continuously, a low frequency oscillation will occur in C9 and the primary of L3. As soon as the voltage at pin 4 of L3 becomes negative T2 starts conducting until the driver transformer is demagnetised. This will cause an extremely high collector current surge. D5 prevents pin 4 of L3 going negative and so this fault condition is avoided. For those applications where this condition cannot occur, D5 can be omitted.

2.2 Deflection Circuit

The horizontal deflection stage contains the diode modulator which not only provides east-west raster correction but also inner pincushion correction, picture width adjustment and EHT compensation. It is not easy to achieve optimum scan linearity over the whole screen. Either the linearity inside the PAL test circle is good and outside the circle the performance is poor, or the average performance over the whole screen is good but inside the test circle deviation is visible. In this application the S-correction capacitors C15 and C16 are balanced in such a way that a good compromise for the scan linearity is achieved.

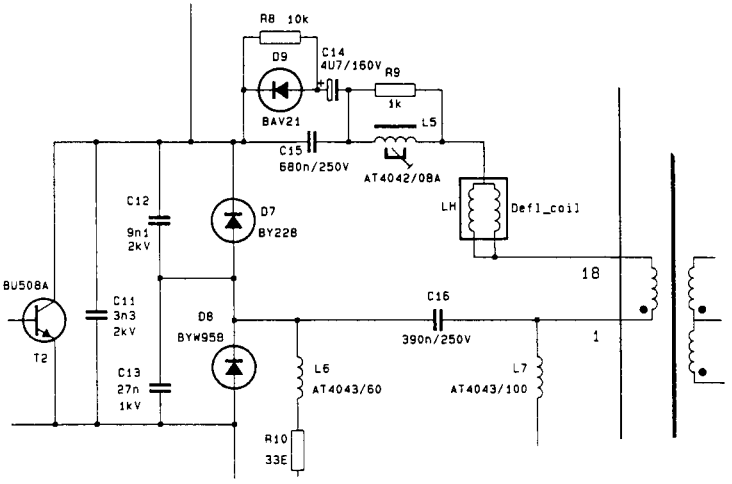


Fig. 3. Deflection Circuit

As already stated in the introduction, due to high beam current in combined EHT and deflection stages picture distortions will occur.

One of these effects is the so called cross-hatch "noses", visible as horizontal phase ringing just below each horizontal white line. During a bright horizontal line the EHT at the picture tube decreases. In the next flyback the picture tube capacitor is recharged by the line output transformer. This energy is taken from the S-correction capacitor, which must be recharged via the primary winding of the line output transformer. This action has a resonance of a few kHz and thus oscillation is visible at the screen.

To avoid this a dip rectifier is connected in parallel with the S-correction capacitor (D9, C14, R8). The energy taken from the S-correction capacitor can now be recharged by C14.

Another geometry distortion is the "Krückstockeffekt". Due to trapezium correction the EW-drive signal applied to L6 can be discontinuous. This will cause amplitude ringing at the top of the screen. An effective way to damp this ringing is a resistor in series with the EW-injection coil.

The consequence of the above mentioned measures is that the drive reserve of the diode modulator has decreased. To compensate for this a separate winding of the line output transformer is connected in series with the deflection coils.

2.3 EHT Generation

For an optimum performance the black line picture tube must be driven at an increased EHT of 27.5kV @ 1.3mA$_{av}$. This implies that the EHT in the no load condition, zero beam current, will be about 29.5kV. To generate this increased EHT a newly designed line output transformer is used with a 4-layer diode split EHT section. From an integrated potentiometer the adjustable focus and grid 2 voltages are taken.

Also the frame supply voltage (26V) and video supply voltage (180V) are taken from the line output transformer. The auxiliary windings of this transformer can be connected rather freely so that a diverse range of auxiliary supplies can be obtained. The only restriction is that the RMS value of the current in a given winding may not exceed 2A. Furthermore the supply current for the heater is obtained from this transformer just like the Φ2 feedback pulse (positive) and a (negative) pulse to synchronise the SMPS.

2.4 Auxiliary Supply

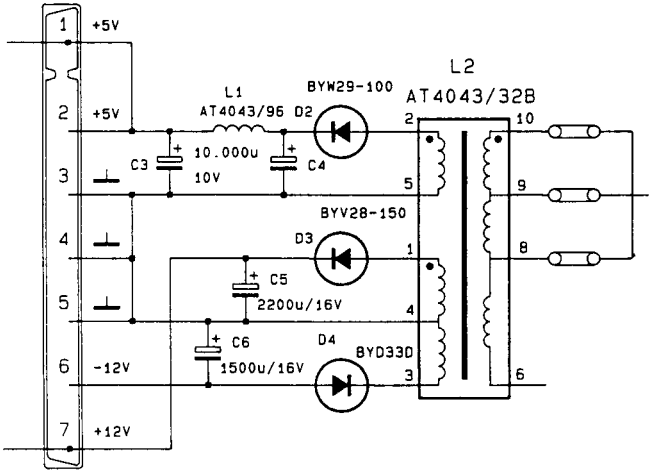


Fig. 4 Auxiliary Supply

When more auxiliary power than can be handled by the line output transformer is required, an auxiliary supply transformer, as shown in Fig. 4, is a good alternative. Such an extra transformer in parallel with the primary winding of the line output transformer is an efficient way to generate low voltage high current supplies. As the transformer is optimised for this purpose no additional stabilisation is required.

Due to the high inductance of the primary winding no influence on the collector current is noticeable. Output voltages are very close to the target values (fine adjustment with primary taps) and have low Ri (HT line is stabilised).

2.5 Additional Circuit Information

12V supply:
The SMPS used in this concept delivers 16V unstabilised. This needs to be regulated to supply the sync processing IC which operates at 12V. This regulation can be done on the sync processing board or the horizontal deflection board since this also acts as a power distribution board.

Tuning voltage:
The tuning voltage is created simply by means of a series resistor R1 and a 30V reference diode located at the tuning board.

EHT compensation:
For proper picture performance it is essential that EHT information is available to compensate picture width and height for EHT variations. For this reason the aquadag is connected to the foot point of the line output transformer. This point is connected to ground by C18 and to the 26V by a non linear resistor network (R12, D11, R13, R14). This network is designed in such a way that it matches with the non linear impedance of the line output transformer and C18 matches with the picture tube capacitance. Thus the voltage available at the foot point of the line output transformer is a good representation of the EHT variation. This EHT information is sent to the geometry processor TDA8433. This information can also be used for beam current limiting. It must then be fed to the video processor for contrast/brightness reduction.

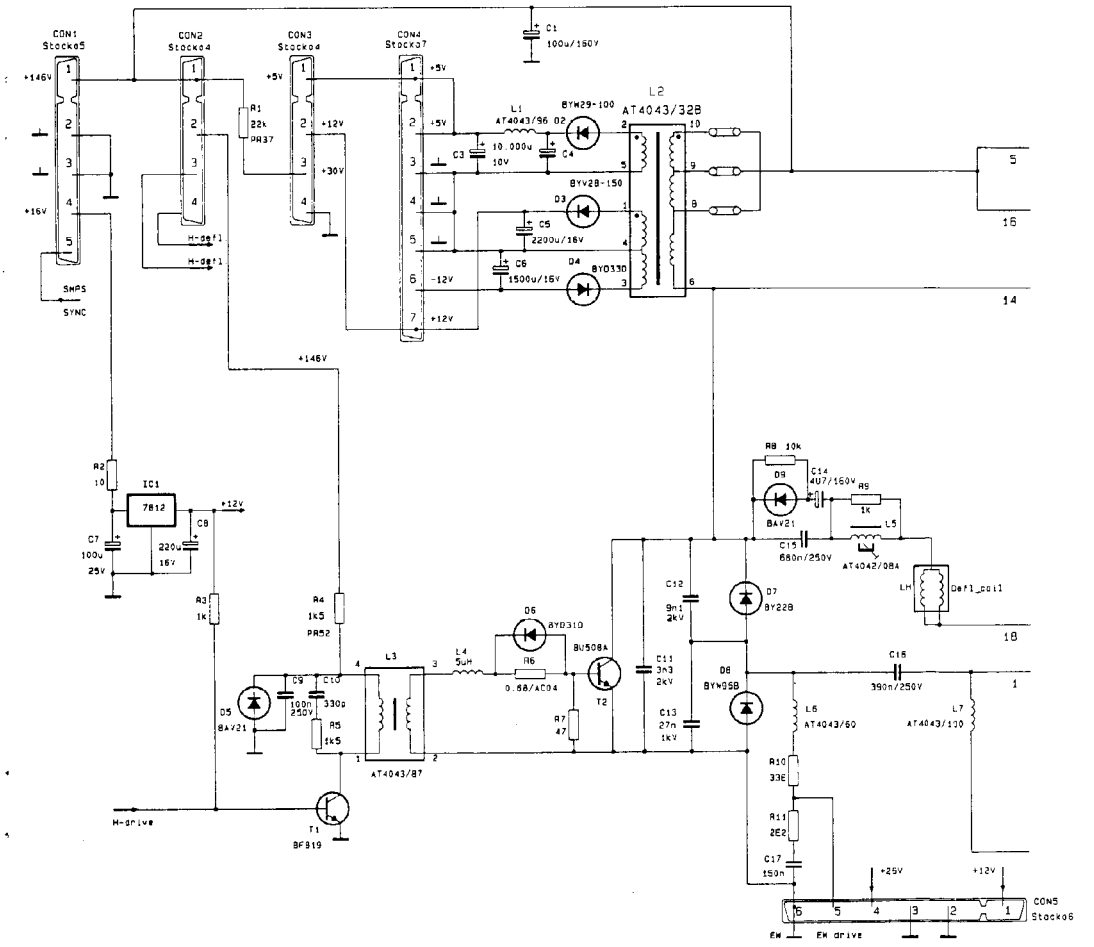


Fig. 5. Circuit Diagram (continued on next page)

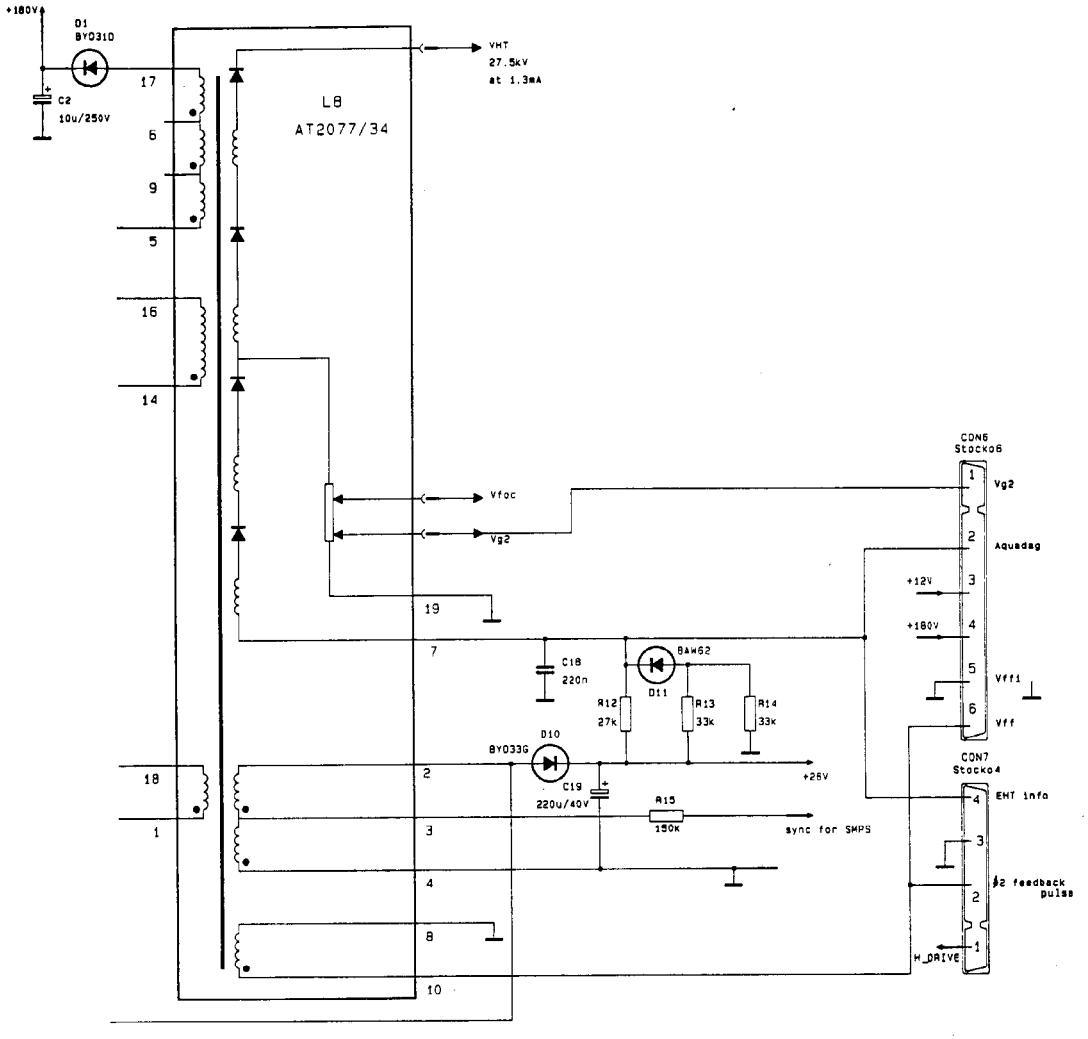
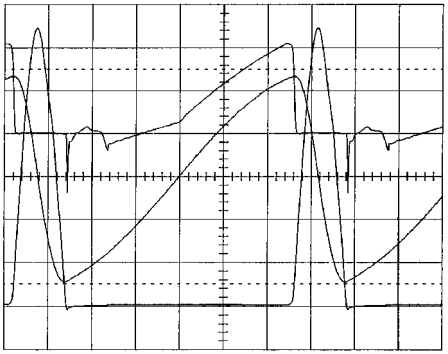


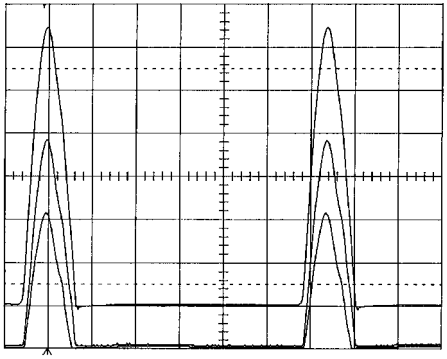
Fig. 6 Circuit Diagram (continued from previous page)

3. Oscillograms

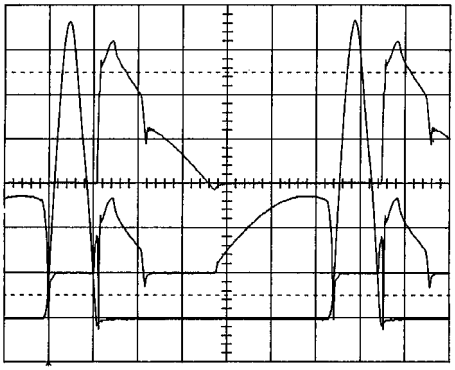


Oscillogram 1:
In this oscillogram the lower trace is the voltage across the deflection transistor (200V/div). The middle trace is the current in the horizontal deflection coil (1A/div). The upper trace is the collector current in the deflection transistor (2A/div). The time base is 10µs/div.

Remarks:
At the end of flyback there is a negative overshoot at the collector voltage. This is caused by the relative slow forward recovery of the damper diode. A part of this current is reverse conducted by the deflection transistor. About 12µs after the start of the scan the deflection transistor is turned on and starts reverse conducting and takes over a part of the current in the damper diodes. See also oscillogram 3.

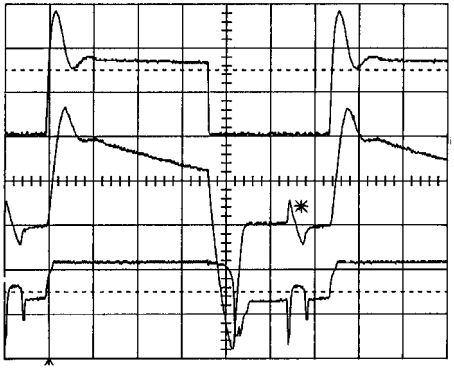


Oscillogram 2:
The upper trace is the voltage across the deflection transistor (200V/div). The lower two traces are the minimum and maximum voltage in the diode modulator (cathode D8) with nominal EW and amplitude settings (50V/div). The time base is 10µs/div.



Oscillogram 3:
In the upper trace the current in the upper diode is shown (1A/div). The middle trace is the current in the lower diode (1A/div). The time base is 10µs/div.

Remarks:
12 µs after the start of the scan the deflection transistor is turned on. Current in the diode modulator is then taken over by the deflection transistor. See also oscillogram 1.



Oscillogram 4:
In the upper trace the collector voltage of the driver transistor is shown (100V/div). The middle trace is the base drive current of the deflection transistor (1A/div). The lower trace is the base emitter voltage of the deflection transistor (5V/div). The time base is 10µs/div.

Remarks:
The overshoot at the collector voltage of the driver transistor is damped by R5 and C10. The current spike in the base drive current (marked with *) is the reverse conduction of the deflection transistor during the forward recovery of the damper diode. See also oscillogram 1.

4. Vertical Deflection, Synchronisation and Geometry Control

The vertical deflection, synchronisation and geometry control circuits are based on an existing PCALE report (ref 3). Because for this application another tube and line output transformer are used some minor modifications are required (component values), see Fig. 7.

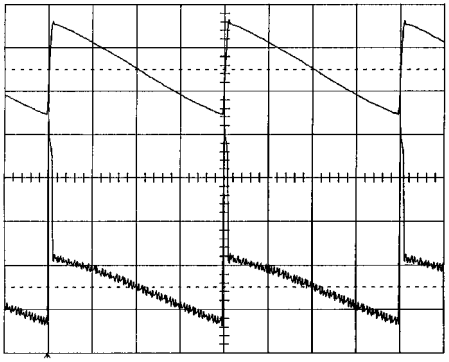
- Due to the increased deflection current, the vertical feedback resistor must be decreased: one of the 2.2Ω resistors becomes 1Ω.

- Due to the increased beam current, the EHT compensation network at pin 24 of the TDA8433 needs to be modified: 120kΩ → 100kΩ, 82kΩ → 150kΩ, 27kΩ → 33kΩ, 68 nF → 10 nF.

- For additional phase shift pin 14 of the TDA2579 is biased with a current from a negative voltage source (rectified from the Φ_2 feedback pulse). While this feedback pulse is smaller than in the original circuit, the 240kΩ resistor must be increased to 1.2MΩ.

Orientation values for the TDA8433 register settings are:

reg	hex
00	25
01	5A
02	07
03	2C
04	2B
05	16
06	16
07	15
08	22
09	21
0A	21
0B	0F
0F	04



Oscillogram 5:
Vertical deflection current (1A/div) and the output voltage (pin 5) of TDA3654 (10V/div). The time base is 5ms/div.

Remarks:
The noise on the output voltage is cross talk from the line deflection coils.

5. Video Amplifiers

The gun of this picture tube is a new design and has its optimum performance at a cut off voltage, V_{CO} = 160V. This implies that the video supply voltage should be at least 20V higher, so $V_{video} \geq 180V$. A video amplifier very well suited for this purpose is the TDA6100.

The RMS voltage of the heater winding of the line output transformer is $V_{10} = 7.35V_{RMS}$, so a series resistor must be used (3.9Ω; 400mW).

6. References

Information from this section was extracted from "Application information for the 16 kHz black line picture tube A66EAK022X11 and A59EAK022X11"; ETV89010 by Han Misdom.

1. "Some aspects of the diode modulator"; EDS7805 by C.H.J. Bergmans.
2. "A synchronous 200W Switched Mode Power Supply intended for 32kHz TV"; ETV89009 by Henk Simons.
3. "Deflection processor TDA8433 with I^2C-bus control"; ETV8831 by D.J.A. Teuling
4. "Application of the TDA6100 video output stage"; ETV8811 by D.J.A. Teuling

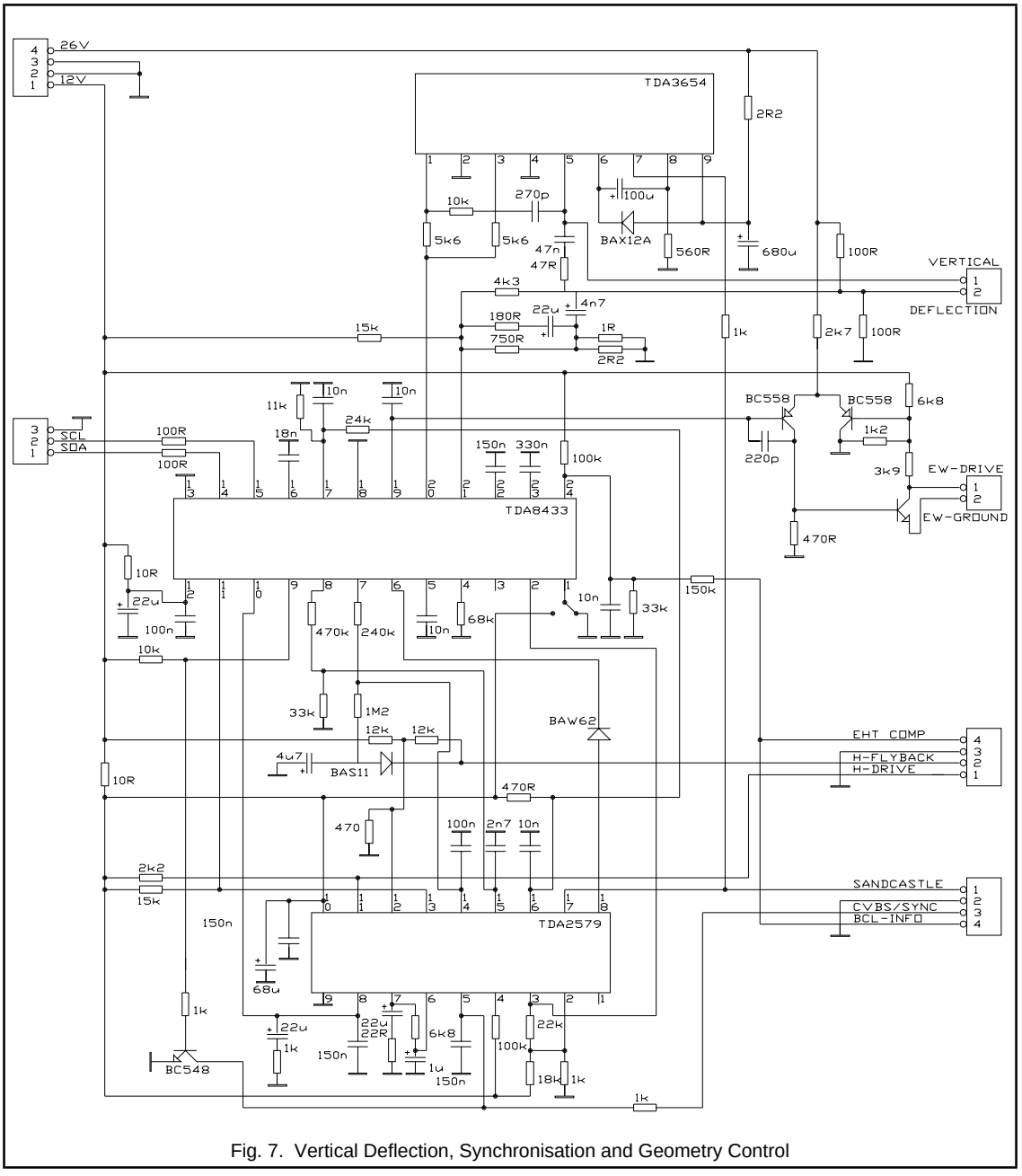


Fig. 7. Vertical Deflection, Synchronisation and Geometry Control

4.2.2 32 kHz / 100 Hz Deflection Circuits for the 66FS Black Line Picture Tube

This report contains a description of deflection circuitry (horizontal 32 kHz, vertical 50-120 Hz) for the 66FS picture tube A66EAK22X42. This design is intended for flicker free TV applications. Provision is made to supply the power for the frequency conversion box.

Summary

The 66FS picture tube is compatible but not identical with the types of the 45AX range. To obtain the typical Black line high contrast and high brightness, the beam current and EHT must be increased at nominal operating conditions. This higher EHT also improves the spot quality. The deflection current is increased because of the higher EHT and reduced sensitivity of the deflection unit.

In comparison with laboratory report ETV8713, describing deflection circuits for 45AX, most modifications are found in the horizontal deflection stage. To generate the increased EHT power a new line output transformer (LOT) with a four layer EHT coil is used. To handle the higher deflection currents two transistors are used in parallel and also two flyback capacitors are used. We have also taken the opportunity to introduce the TDA8433. This deflection processor -in BiMos technology- is the successor of the TDA8432.

The vertical deflection stage is redesigned in such a way that vertical shift signals can be inserted without bouncing effects. The insertion of vertical shift signals is necessary in 100 Hz operation for a proper interlace.

1. Introduction

In this report a description is given of double line and frame frequency (32 kHz; 100 Hz) deflection circuits for the 66FS picture tube A66EAK22X42. The report is based on report ETV8906, describing these circuits for the 78FS picture tube [1]. By changing some component values the pcb for the 78FS can also be applied to drive the picture tube A66EAK22X42. In the line output stage the output transistor BU2508 is used.

2. General description

2.1 Block diagram

The block diagram is given in Fig. 1. The main interconnections are given as well. The separate blocks can be recognised in the circuit diagram.

The separate H and V sync and V shift are available from the frequency conversion box.

2.2 Circuit architecture

A key component in this set up is the deflection processor TDA8433. The horizontal and vertical picture geometry can be controlled by means of I^2C bus commands. Because this deflection processor has no vertical oscillator, there will be no vertical deflection when there are no vertical sync pulses applied to the set. For laboratory purpose a separate vertical oscillator is added to make the monitor part a self contained unit. When incorporated in a receiver this vertical oscillator can be omitted. When there are no vertical sync pulses, the guard circuit of the vertical output stage will blank the video information. This prevents spot burn-in of the tube.

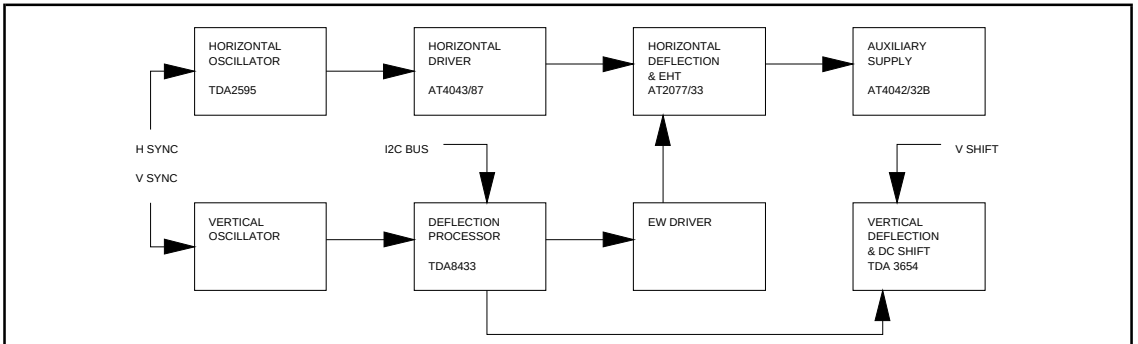


Fig. 1 Block diagram

The vertical deflection stage consists of the well known TDA3654 vertical output IC. To make vertical shift insertion possible, the output stage is slightly redesigned. This ac coupled output stage now has a quasi dc coupled behaviour.

The EW driver is a voltage amplifier, acting as a buffer between the deflection processor and the diode modulator.

The block "horizontal oscillator" consists of the TDA2595 with its Φ1 and Φ2 loop, the horizontal oscillator itself and sandcastle generation. The other features of this ic are not used.

Coupling between the TDA2595 and the deflection stage is made by the horizontal driver stage. This stage is a transformer coupled inverting driver stage.

The horizontal deflection stage is a classic concept. It consists of a combined deflection and EHT generation. It also comprises linearity correction, S-correction, inner pin cushion correction and a dc shift circuit. The LOT (AT2077/33) belongs to the transformer family DSB (diode split box) and has four EHT layers. It delivers the following voltages:

* EHT = 27.5 kV @ 1.3mA
* Focus = 0.22 - 0.30 x EHT
* Vg_2 = 0.011 - 0.033 x EHT
* Heater ≈ $10.4V_{RMS}$
* Video supply = 192V
* Frame supply = 28V
* Φ2 ref. pulse = $+40V_{pp}$

Furthermore the LOT has some taps which can be useful when the application is modified.

In parallel to the primary winding of the LOT the auxiliary supply transformer (AT4043/32B) is located. This auxiliary supply delivers the following voltages:

* +5V @ 5A
* +15V @ 1A
* -12V @ 1A

These supply voltages are intended for the digital and analog signal processing circuits.

The philosophy behind this circuit needs some further explanation.

It is very difficult to generate exactly 5V at the output of an SMPS or LOT. Due to an optimum winding design of this kind of transformer, the voltage ratio per turn is high (2 - 5V per turn). This implies that a stabilizer is required. A switching post regulator adds to the circuit complexity and cost. A dissipative series stabiliser needs at least 2V, so for a 5A supply the losses are already 10W.

The auxiliary transformer used in this concept is optimised for generating these low voltages at high currents. The winding design is such that no stabilizer is required after the rectifier. Due to the high primary inductance of this transformer the collector current increase of the deflection transistor is negligible.

If the auxiliary loads are low, this auxiliary supply transformer can be omitted and the unused taps of the LOT can be used to generate these voltages.

3. Circuit description

Using circuit diagram blocks the total concept will be explained. This will be done with reference to the function blocks of Fig. 1. The complete circuit diagram is given in Figs. 11-13.

3.1 Vertical oscillator

As already stated in section 2.2 this vertical oscillator can be omitted in a final design. The circuit is shown in Fig. 2.

This oscillator is the well known astable multivibrator built up around T8 and T9. This oscillator is free running at 45 Hz and can be synchronised up to at least 120 Hz. T7 is an additional sync transistor and is ac coupled to the vertical sync signal (TTL level).

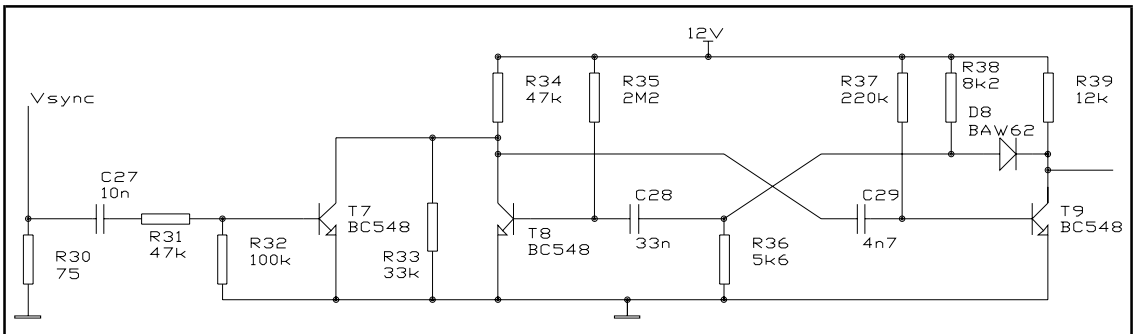


Fig. 2 Vertical oscillator

3.2 Deflection processor TDA8433

The TDA8433 is an analog, I²C bus controlled, deflection processor. It generates the vertical deflection current waveform and the EW (East-West) waveform. The necessary corrections on these waveforms are I²C bus controlled. This ic also includes some DACs and ADCs. They can be used for control functions of other circuitry [2].

The resistor at pin 4 determines the reference current for this ic. Pin 2 is the vertical sync input. At the capacitor at pin 5 (C-flyback) a triangle waveform is generated which is used for internal timing. This signal is used to generate the vertical sawtooth at pin 22 (C-saw). At pin 23 (C-amp1) a storage capacitor of the amplitude stablisation loop is found whose voltage determines the amplitude of the sawtooth. The V-sync input can only handle unequal spacings of the pulses if there is a 2-sequence (e.g. Teletext 312-313 lines). A 4-sequence from the 100 Hz box cannot be handled by the amplitude loop.

The vertical sawtooth is internally connected to the "geometry control" section. In this section S-correction, vertical shift and linearity correction are added to the sawtooth by I²C commands. The amplitude is controlled by pin 24 (EHT-comp) to compensate for EHT variations.

From here the signal goes to one input of the internal error amplifier. The other input is connected to pin 21 and the output to pin 20. By means of an I²C command the external input pin can be selected as an inverting or non-inverting input. This provision is made to handle both non-inverting and inverting vertical output stages.

The block "geometry control" also generates the EW parabola. The I²C bus controllable functions are: parabola, corner, trapezium and picture width. By means of the signal at pin 24 this signal is corrected for EHT variations. The EW drive output is available on pin 19.

On the digital side of this IC we find the following functions:

Pin 15 (SCL) is the Serial CLock and pin 14 (SDA) is the Serial DAta. Pin 1 is the address pin and can either be connected to ground or +12V. The three external DA converters can be controlled by the bus: DACA, DACB & DACC. With DACA the horizontal free funning frequency of the TDA2595 can be adjusted. The other two DACs (pin 7 & 6) are not used. They can be used for H-shift and H-phase control. See appendix A.

Pins 9 and 10 are output switch functions: not used in this application. When pin 10 is programmed high, it can be used as an input pin. Together with pin 17 it forms a comparator. Pin 10 is connected to the Φ1 voltage of the TDA2595 and pin 17 to the reference voltage. In this way an I²C bus signal is available whether the horizontal oscillator is in centre, locked and mute or coincidence so information can be sent to the IN-input. This also makes automatic f_o adjustment possible.

The supply part of this IC contains 4 pins. Pin 18 is ground for the geometry and sawtooth part: pin 13 is ground for the output stages and I²C bus. Pin 12 is the +12V input and at pin 16 an external capacitor is required for filtering the +5V (internally generated).

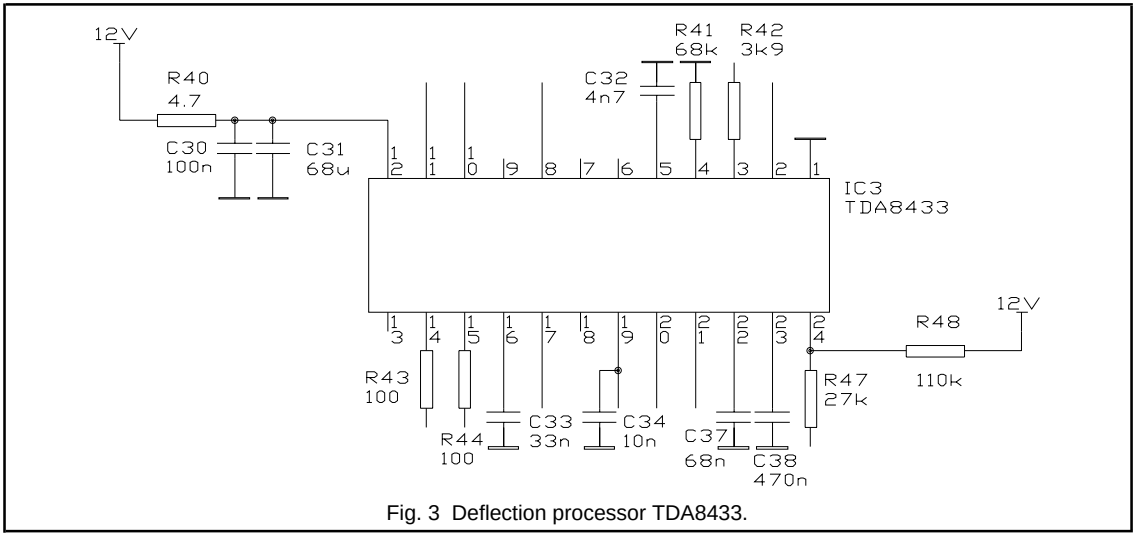


Fig. 3 Deflection processor TDA8433.

3.3 Vertical output stage

The vertical output stage is controlled by the well known TDA3654. To make this stage suited for 100 Hz TV some modifications of the ordinary solution are required. The circuit is shown in Fig. 4.

A damper network is located in parallel to the vertical deflection coil. The values depend on the characteristics of the deflection unit. The line ripple that is injected from the horizontal deflection coil is damped by the series connection of R55 and C48. R55 reduces the line ripple to an acceptable value. C48 is added to block the relatively low vertical deflection voltage in order to limit the dissipation in R55. A resonant circuit is created by C48 and the inductance of the deflection coil. R54 is a critical damper for this circuit to minimise excessive oscillations after the vertical flyback.

The deflection current is sensed by two 1.5 Ω resistors in parallel and fed back to the deflection processor. The network C36, R45 and C35 is added for a stable loop transfer because of the non resistive load at the output of the TDA3654.

The output stage is ac coupled. The dc bias point is fixed by the resistors R60 and R61. By the V-shift setting of the TDA8433 vertical shift of the picture is possible.

An additional shift circuit is connected in parallel to the dc shift circuit to make an alternating frame shift possible. It consists of T11 and its series elements. When T11 is conducting a small dc current will flow through the deflection coil. Due to the S-correction of the vertical deflection current a smaller current is required at the top and bottom than in the middle of the tube to guarantee proper interlacing across the whole screen. Therefore, the waveform of the shift current is derived from the parabola voltage of C49. A potentiometer is provided because this interlace setting is critical.

The drive signal required for this alternating frame shift is generated by the 100 Hz conversion box.

If two independent shift signals are needed, the whole circuit must be duplicated.

3.4 Horizontal oscillator

The horizontal oscillator used is the TDA2595. The horizontal sync signal (TTL level) is divided and ac coupled to the input pin 11. At pin 14 the reference current is set by a 13 kΩ resistor. The sawtooth capacitor for the oscillator is connected to pin 16. The free running frequency is 31.25 kHz and determined by the value of its capacitor and the reference current. By varying the reference current the free running frequency can be adjusted. This is done using the DAC-A output (pin 8) of the TDA8433 via resistor R25, see section 3.2.

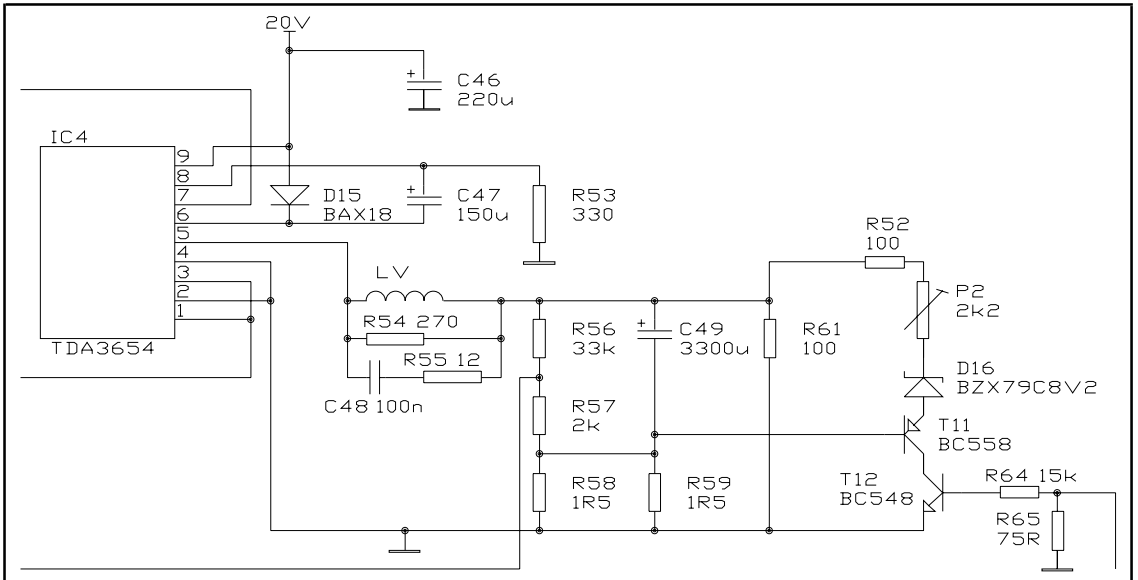


Fig. 4 Vertical output stage

This oscillator is locked to the incoming sync signal by a PLL (Phase Locked Loop). The starting point of the horizontal sawtooth is compared with the horizontal sync. If this starting point is not in the middle of the horizontal sync pulse, an error signal will appear at pin 17. Via R27 the current of pin 14 is affected and thus the horizontal phase can be locked. The loop filter consists of C25, R28 and C26.

The output of the oscillator is internally connected to a second PLL Φ2 and to a phase shifter. The phase shifted signal is available via an output stage at pin 4 (horizontal output). This signal drives the deflection stage. A feedback signal of the deflection stage is applied to the other input of the Φ2 phase detector (pin 2). In this way the horizontal flyback of the deflection stage is locked to the oscillator and thus to the sync as well. The loop filter of Φ2 consists of one capacitor at pin 3. This second PLL has a much larger bandwidth to compensate for the storage time variations in the deflection transistors.

At pin 6 a two level sandcastle pulse is available. It is mixed with the vertical blanking signal of the TDA8433 or the flyback of the TDA3654 to generate a three level sandcastle. See also the description of TDA8433 section 3.2 and TDA3654 section 3.3.

Pin 7 is the mute output. This signal is sent to the TDA8433 so that "oscillator locked" information is available at the I^2C bus.

As these kinds of ic are sensitive to supply pollution provision is made for a local supply filter R21, C18 and C19.

For layout recommendations see section 4.

3.5 Horizontal drive circuit

The horizontal drive circuit is a classical transformer coupled inverting driver stage. When driver transistor T1 is conducting, energy is stored in the transformer. When T1 is turned off the magnetising current continues to flow in the secondary side of the transformer thus turning on the deflection transistor. At this time the voltage on the secondary side of the driver transformer is positive ($V_{BE}+I_B*R6$). When the driver transistor turns on again this secondary voltage reverses. At the same time energy is stored in the transformer again.

During this turn off action the forward base drive current decreases with a controlled dI_B/dt, thereby removing the stored charge from the deflection transistor. The dI_B/dt depends on the negative secondary voltage and the leakage inductance. When the drive circuit is designed properly, the deflection transistor stops conducting when its negative base current is about half the collector peak current.

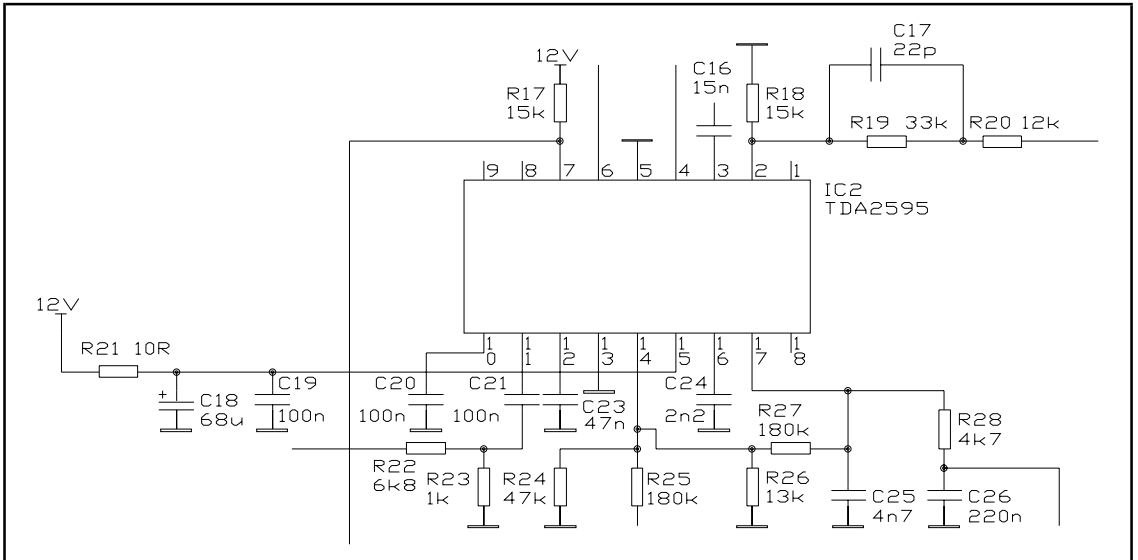


Fig. 5 Horizontal oscillator

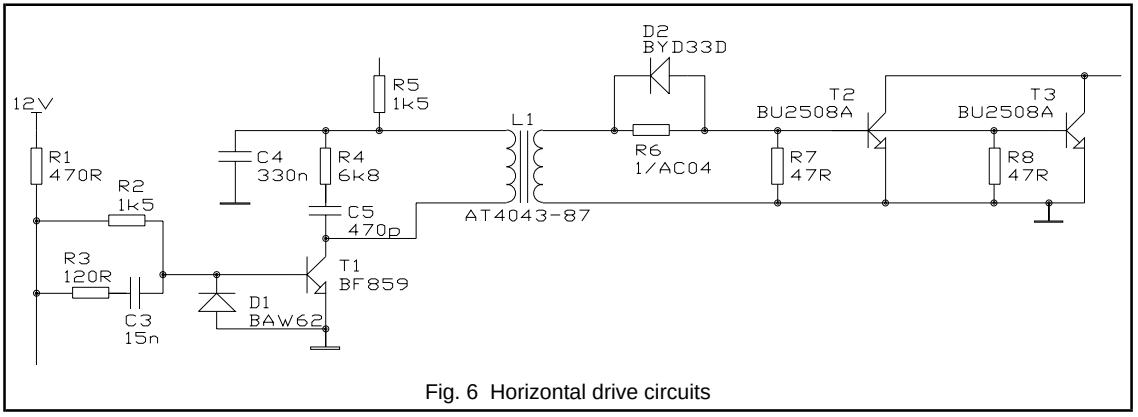


Fig. 6 Horizontal drive circuits

To prevent the deflection transistor from turning on during flyback due to parasitic ringing on the secondary side of the driver transformer a damp resistor is connected in parallel with the base emitter junction of the deflection transistor.

Also at the primary side of the driver transformer a damp network is added (R4 & C5) to limit the peak voltage on the driver transistor.

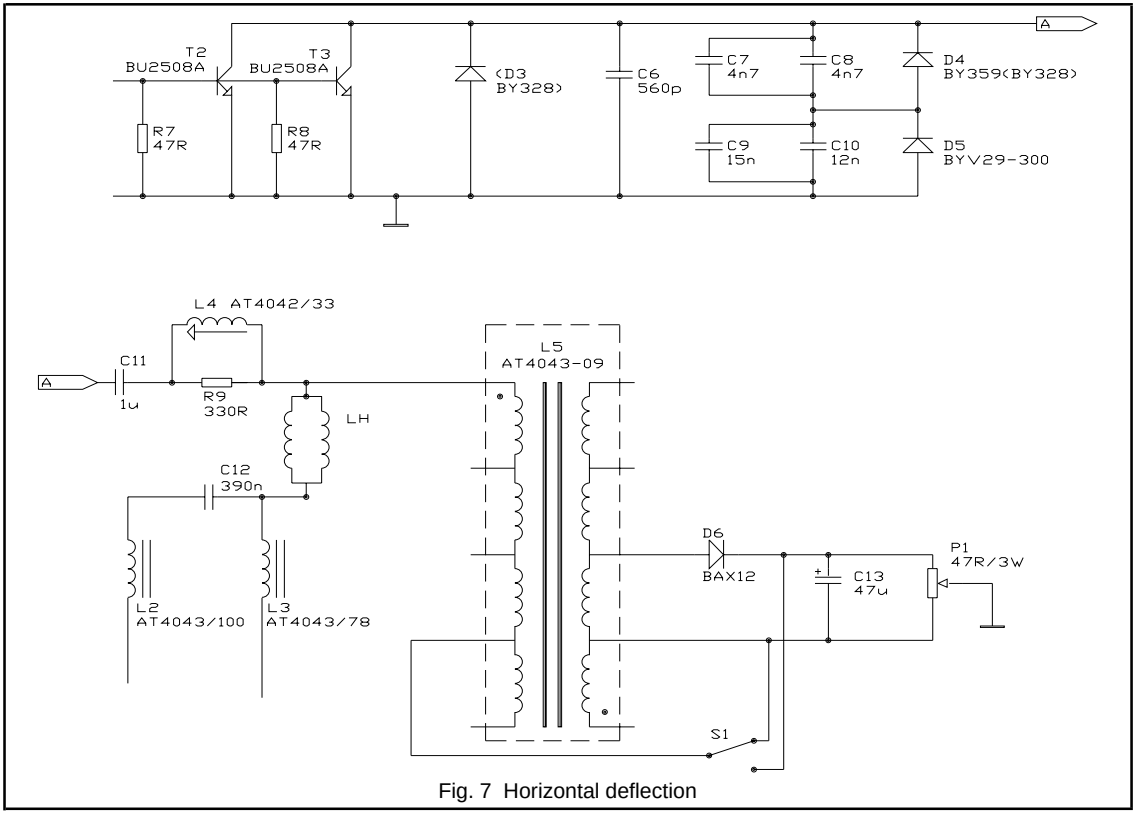


Fig. 7 Horizontal deflection

3.6 Horizontal deflection

The horizontal deflection is the classical deflection stage with the diode modulator which not only provides the EW raster correction but also inner pincushion correction. Due to the high frequency in combination with large currents some problems do appear here. The horizontal deflection coil needs 10.4A peak-to-peak. This results in a collector peak current of 6-7A, too much to handle with one BU2508A. So, two transistors are used in parallel. If the print layout is made in a proper way no special precautions are required to use this type of transistor in a parallel configuration. (NB the circuit was constructed before the BU2525A became available.)

For the flyback capacitor the current is too high as well. So, here, also, two devices are used in parallel. The S-correction capacitors do not have problems in handling the current.

There are two possible solutions for the damper diodes. The BY359 is a high current damper diode available in isolated and non-isolated TO220 packages. This device has been re-designed for operation as a damper diode specifically for 32 kHz deflection systems. An alternative solution is to place a third diode in direct parallel with the collector-emitter's of the deflection transistors. This option allows two cheaper axial diodes to be used in the modulator, eg BY328. This option is shown in Fig. 7.

For full performance of scan linearity a horizontal dc shift circuit is incorporated. In an ordinary TV set the horizontal off centre of the picture tube is compensated by the phase shift of the horizontal oscillator. This, however, introduces a linearity error in the deflection. In many cases this error is acceptable; if not, it can be compensated by means of an adjustable linearity corrector.

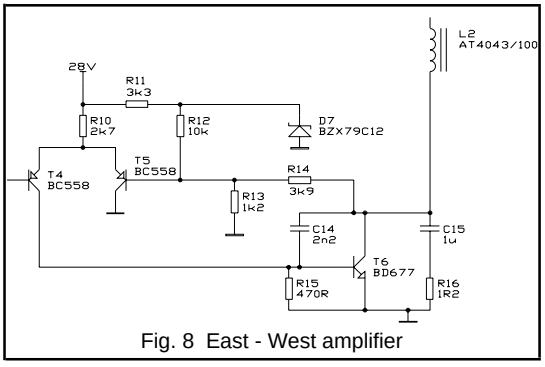


Fig. 8 East - West amplifier

The most proper way of picture alignment is the following: the linearity corrector is only used for compensating the linearity error caused by the resistive part of the impedance of the horizontal deflection yoke. The off centre of the tube is compensated by a shift circuit. Therefore, a dc shift circuit is incorporated. This circuit has been built up around L5. With P1 the amount of shift current can be adjusted and with S1 the polarity can be selected. The horizontal shift can be made bus controlled by using DAC-B or DAC-C of the TDA8433. A suggestion for a suitable interface is given in Appendix 2.

3.7 East - West correction

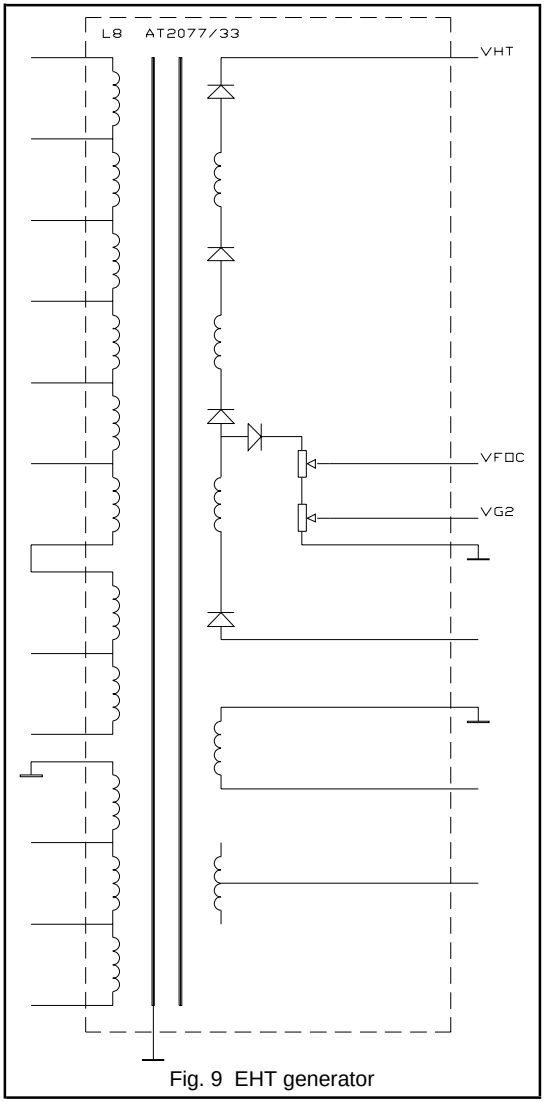


Fig. 9 EHT generator

The EW waveform is generated by the deflection processor TDA8433. An external amplifier feeds this correction to the horizontal deflection stage. It is injected in deflection via

L2. The possible corrections are: picture width, EW parabola, corner correction, trapezium and EHT compensation.

The EW amplifier is shown in Fig. 8. It consists of a Darlington power transistor, T6, a differential amplifier, T4 & T5, and a feedback network R13 R14. R12 is added for proper dc bias. Because this amplifier has a non real load, special attention is paid to loop stability. Across T6 there is a miller capacitor, C14. The line ripple current of L2 flows mainly through C15 and R16.

3.8 EHT generation

The darker glass requires a higher EHT power for an equal light output. An increase of only the beam current has two disadvantages: a larger spot size and a higher drive from the video amplifiers. An increase of only the high voltage would come in conflict with the legislation on X-ray radiation.

As a compromise an EHT of 27.5kV @ 1.3mA is chosen. A new design of LOT is used, see Fig. 9. This LOT is a four layer diode split box (DSB) design with extra high voltage capability. From an integrated potentiometer the adjustable focus and grid 2 voltages are taken.

3.9 Auxiliary supply

Some of the auxiliary supplies are taken from the LOT such as heater, video and frame supply. The other auxiliary supplies are taken from a separate transformer. The philosophy behind this concept is explained in section 2.2.

The auxiliary transformer is connected in parallel to the LOT. On the secondary side of this transformer the auxiliary voltages are taken. These outputs supply the signal processing circuitry (5V @ 5A, 12V @ 1A, -12V @ 1A).

The primary inductance of this transformer is relatively high, so the increase of collector current in the deflection transistor is low. To adjust the output voltage the primary winding has some taps. Due to the relative high ESR of the 5V smoothing capacitors a π-filter is required.

With moderate current levels all the auxiliary supplies can be taken from the LOT.

4. PCB design considerations

For general information see reference 3.

4.1 TDA2595

The following tracks and pins of the TDA2595 are critical and need special attention:

* The track length at pin 14 - reference pin - to its peripherals should be kept as short as possible.

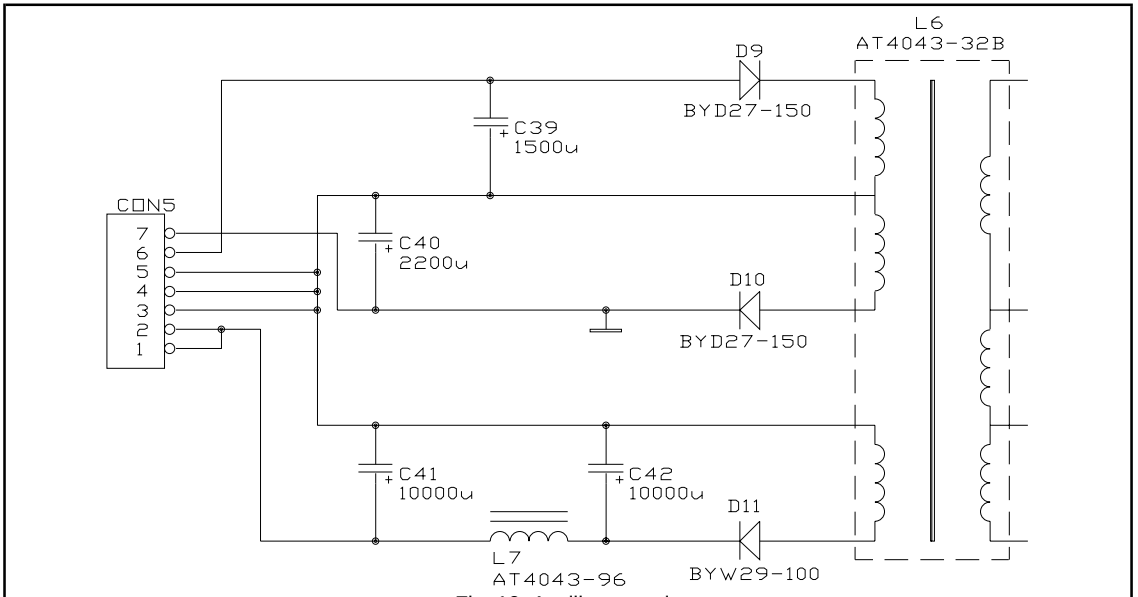


Fig. 10 Auxiliary supply

* The peripheral components connected to pins 14, 16, 3, 17 and 15 should be connected directly to the ground of this ic.
* The ground track of this ic may not carry current from other parts of the set.
* As this ic is sensitive to high frequency ripple on the supply rail, local decoupling is essential.

4.2 TDA8433

The following tracks and pins of the TDA8433 are critical and need special attention:

* The components connected to pins 4, 5, 12, 16, 19, 22 and 23 should be connected to the analog ground (pin 18) and as close as possible.
* The track length of the pins 4, 5, 22 and 23 should be as short as possible.
* The ground track of this ic may not carry current from other parts of the set.
* Local decoupling is essential because this ic is sensitive to high frequency ripple on the supply rail.

4.3 Horizontal deflection and supplies

This kind of circuit carries currents with high dI/dt. The loops that contain these currents should have an area as small as possible to limit magnetic radiation. Examples are the loop of deflection coil with the deflection transistors, diodes and flyback capacitors. Also the loop formed by smoothing capacitor C43, primary of LOT and deflection transistor should be kept small.

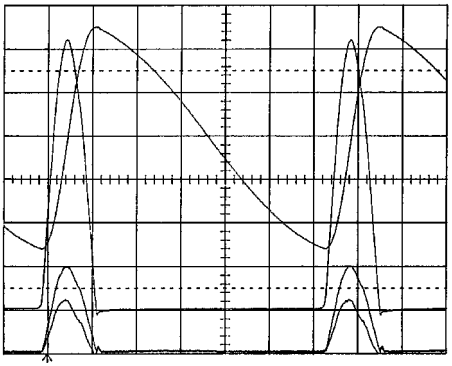
In case of rectifiers the ground track between transformer winding and smoothing capacitor may not be a part of any other ground track.

4.4 Drive circuit

To ensure current balance in the deflection transistors, the base and emitter tracks of the two transistors should be as similar as possible to create the same impedances for both transistors.

5. Oscillograms

All oscillograms were taken under nominal load conditions of the auxiliary supply and 1mA beam current.



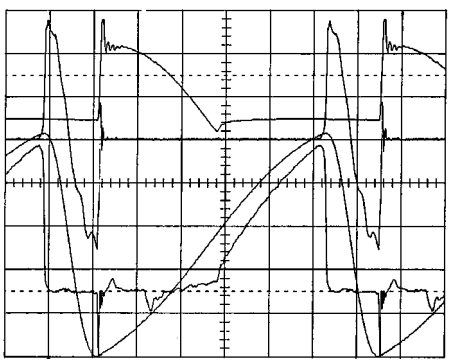
Oscillogram 1:

In this oscillogram the upper two traces show the average deflection current (2A/div) and the voltage across the deflection transistors (200V/div). The peak V_{CE} is 1244V.

The lower two traces are the minimum and maximum values at the mid-point of the diode modulator (100V/div) due to EW modulation.

Remarks:

At the end of flyback there is a negative over shoot at the collector voltage. This is caused by the forward recovery of the damper diode.



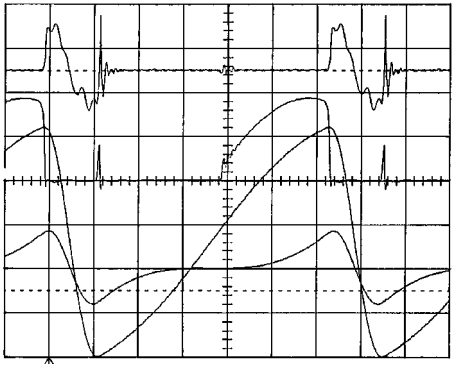
Oscillogram 2:

The lower trace is the current in the deflection transistors. The upper trace is the current in damper diode D4 and the middle trace is the current in the upper flyback capacitors (C7 + C8). All current settings 2A/div.

Remarks:

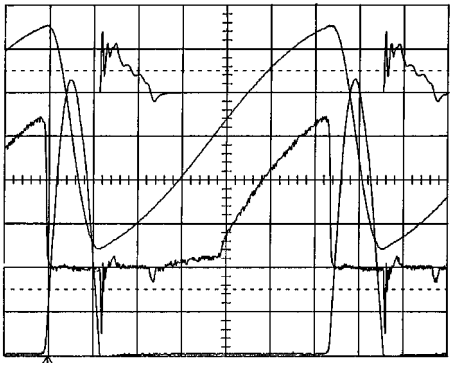
At the end of flyback the current in the flyback capacitor is taken over by the damper diodes. Due to parasitic capacitance and inductance ringing occurs. 5µs later there

is a negative current in the deflection transistor. This is reverse conducting of the base-collector of the transistor caused by the fact that the base drive is already turned on.



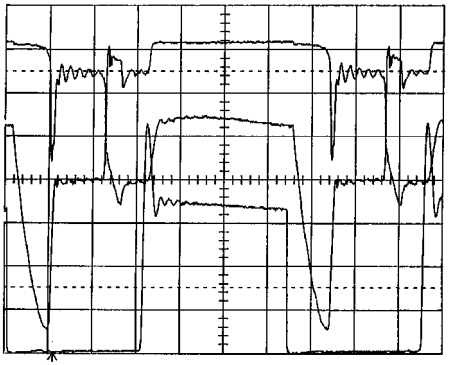
Oscillogram 3:

In this oscillogram the upper trace is the current in the lower flyback capacitors C9 + C10. The second trace is the current in the diode D5. In the bottom part the current in the bridge coil is given and the deflection current is shown once more as a reference. All settings 2A/div.



Oscillogram 4:

In this oscillogram the deflection transistor I_C and V_{CE} are given as a reference. The upper trace is the current in the third diode D3. As soon as the deflection transistor is turned on the current of D3 is taken over by the transistors. All current settings 2A/div.



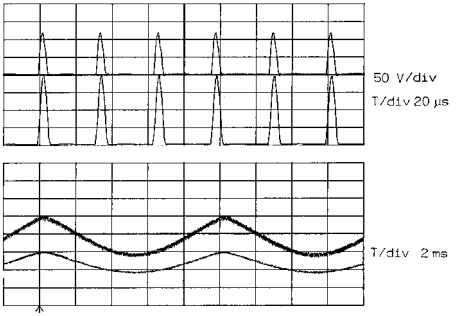
Oscillogram 5:

The upper trace is the V_{BE} of the deflection transistors (5V/div). The middle trace is the I_B of the deflection transistors (1A/div). The lower trace is the V_{CE} of the drive transistor T1 (50V/div).

Remarks:

The over shoot at the rising edge of the driver transistor is caused by the leakage inductance of the driver transformer. By means of the damping network R4, C5 this over shoot is limited. This network is chosen in such a way that the ringing is critically damped.

The base drive circuit is designed in such a way that the peak of the negative base drive current, I_{Boff}, is approximately half the collector current, I_C. During turn off the V_{BE} of the deflection transistor should remain negative. To achieve this the ringing is damped by R7 and R8.

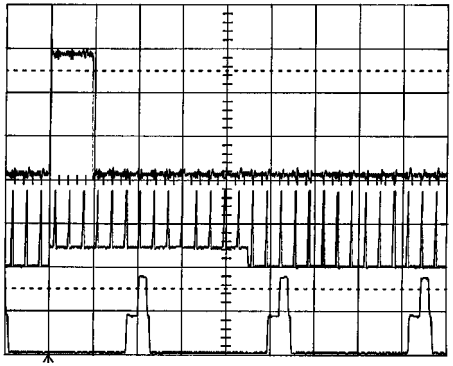


Oscillogram 6:

This split screen oscillogram was made with two different time base settings. In the upper grid the minimum and maximum values of the flyback pulses across C9 + C10 of the diode modulator are given under nominal conditions. The lower grid shows the amplified EW drive signal (collector T6 5V/div) and the output of the TDA8433 (pin 19 2V/div).

Remarks:

At the collector of T6 some line ripple is visible.

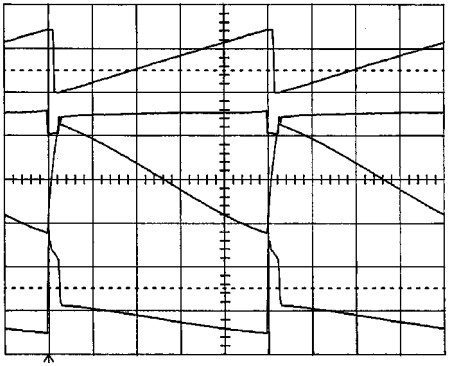


Oscillogram 7:

The upper trace gives the vertical sync signal (1V/div, 100µs/div). The middle trace is the sandcastle (5V/div, 100µs/div). The lower trace is the sandcastle during vertical scan (5V/div, 10µs/div).

Remark:

This three level sandcastle pulse is the sum of the two level sandcastle of the TDA2595 and the vertical blanking of the TDA8433.

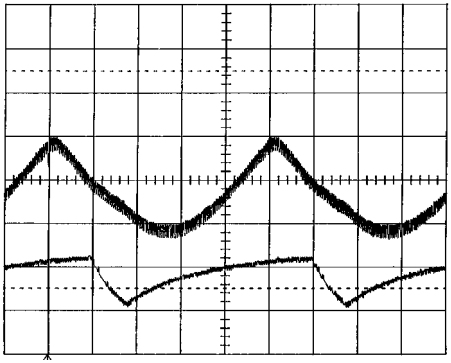


Oscillogram 8:

The upper trace is the generated sawtooth at pin 22 of the TDA8433 (5V/div). The second trace is the output signal of the error amplifier of the TDA8433 pin 20 (5V/div). The third trace is the sawtooth current in the vertical deflection coil (1A/div). The lower trace is the output signal of the vertical output amplifier TDA3654 pin 5 (20V/div).

Remark:

Due to the L/R of the vertical deflection coil the current in the coil can not follow the fast retrace time of the sawtooth generator. The output amplifier clamps after the flyback to 2xVb. When the control loop locks after the flyback, a slight voltage overshoot can be found at the output of the TDA3654. This is damped by C48, R55 and R54.



Oscillogram 9:

The lower trace is the voltage at the foot point of the line output transformer (10V/div). This signal is a representation of the EHT variations needed by the anti breathing.

The upper trace is the EW waveform at T6 (5V/div). On the EW waveform a correction signal is added to prevent the picture from breathing.

6. References

Information for this section was extracted from "32kHz/100Hz deflection circuits for the 66FS Black Line picture tube A66EAK22X42"; ETV89012 by J.v.d.Hooff.

1. P.C.A.L.E. report ETV8906. "32 kHz / 100 Hz deflection circuits for the 78FS picture tube" by Mr. J.A.C. Misdom.

2. C.A.B. report ETV8612. "Computer controlled TV; the deflection processor TDA8432" by Messrs. E.M. Ponte and S.J. van Raalte.

3. C.A.B. report ETV8702: "EMC in TV receivers and monitors" by Mr. D.J.A. Teuling.

7. Circuit diagrams

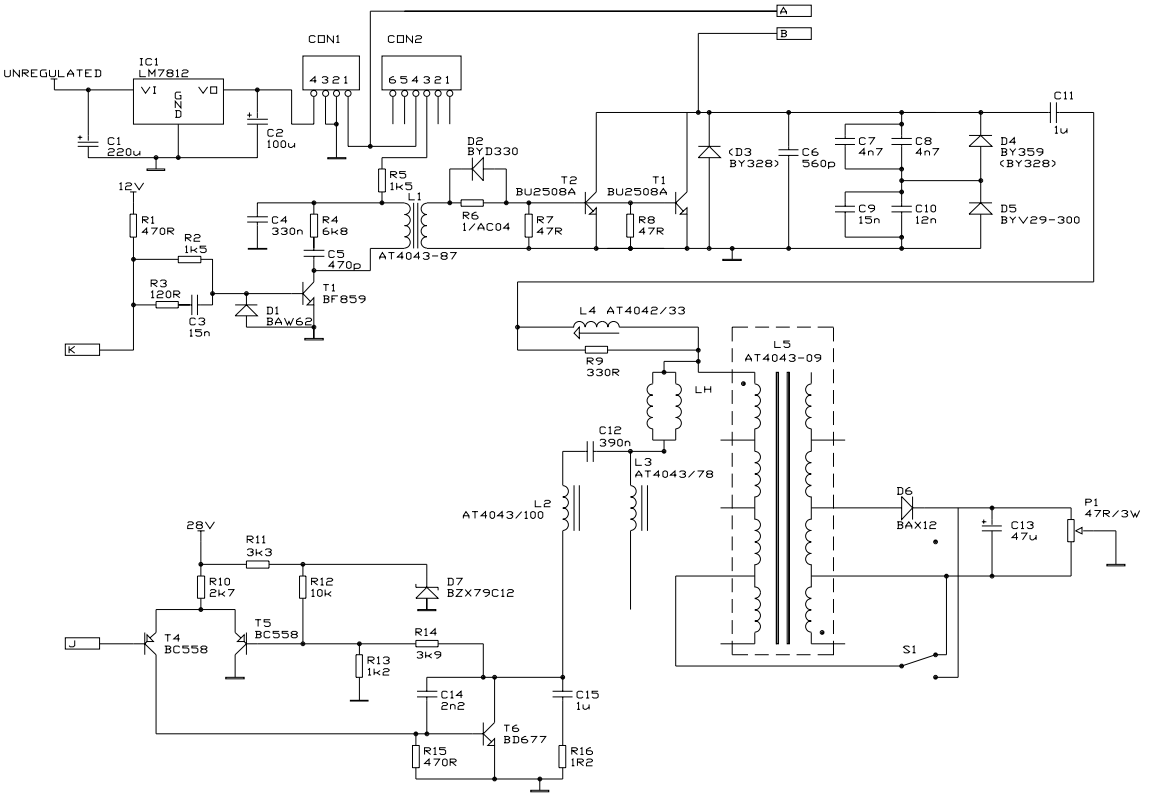


Fig. 11 Horizontal Deflection and EW Amplifier

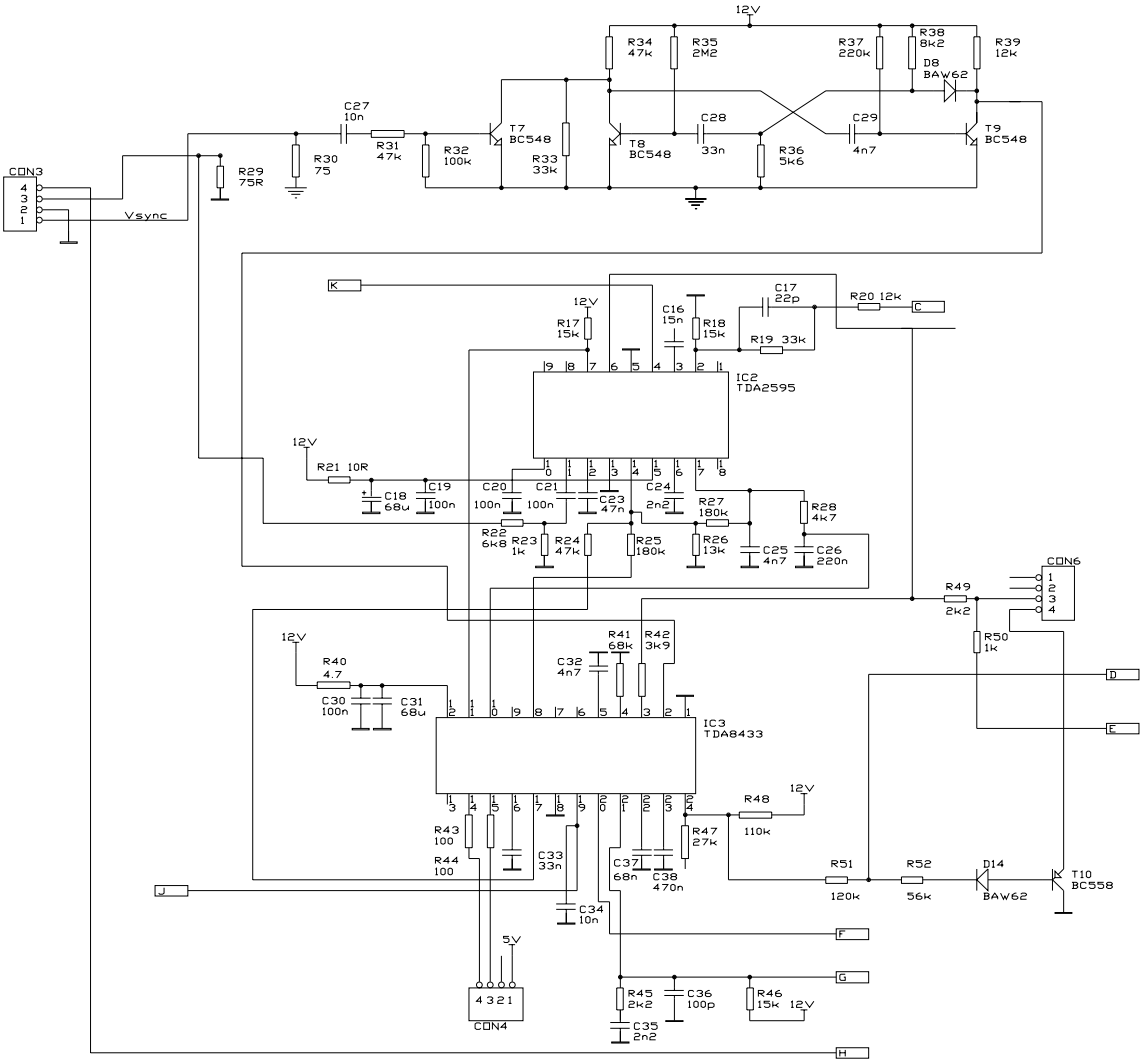


Fig. 12 Deflection Processor and Horizontal & Vertical Oscillators

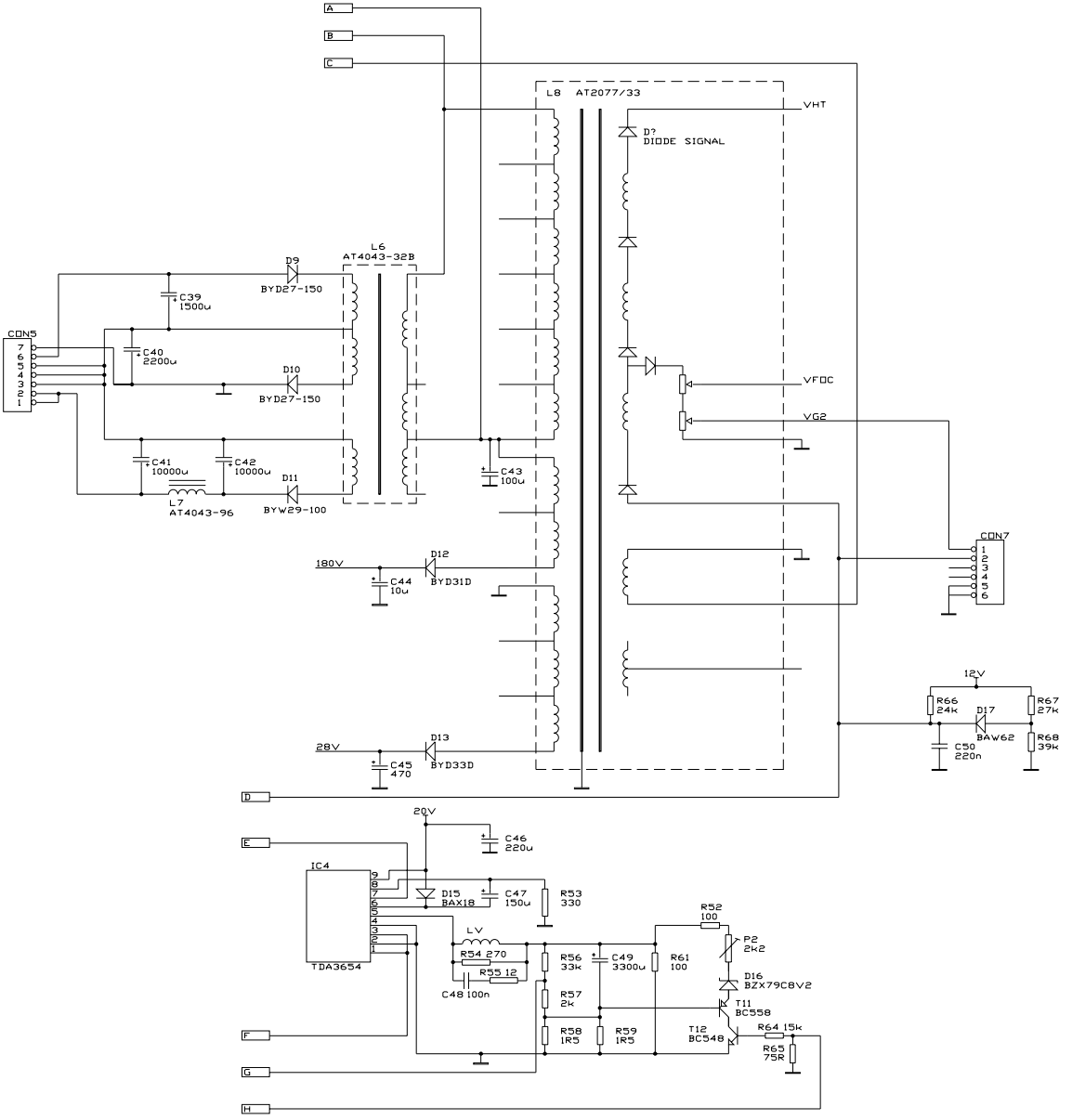


Fig. 13 Auxiliary supply, EHT Generator and Vertical Output Stage

Appendix A

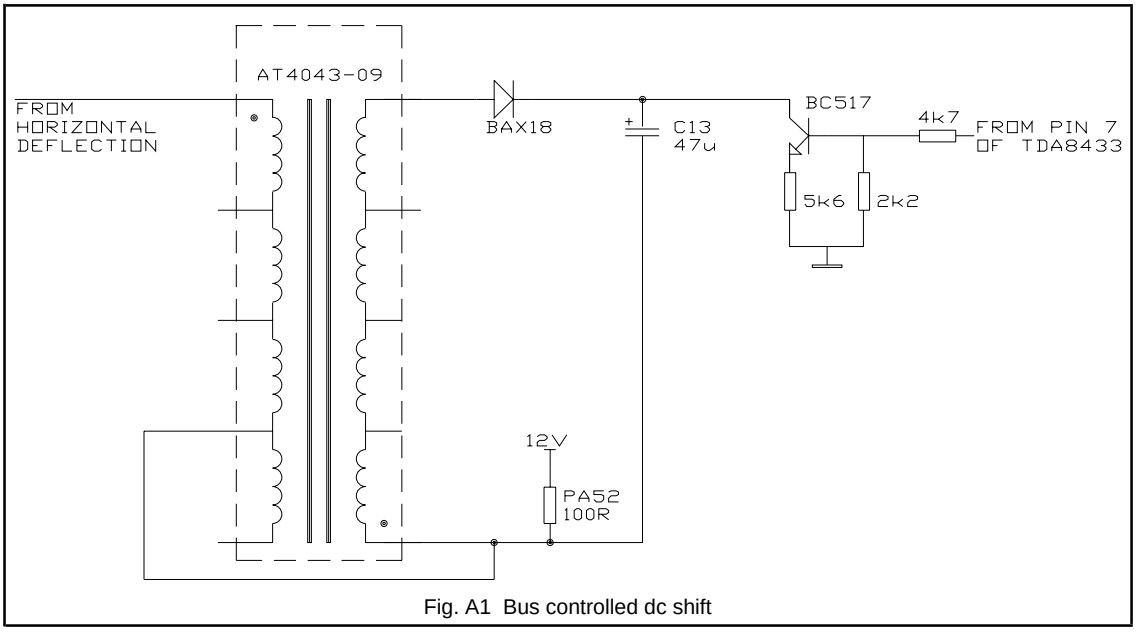


Fig. A1 Bus controlled dc shift

The deflection processor TDA8433 has three DAC's. In this application only one DAC (DAC-A) is used. In this section some ideas are given to use the other two DAC's.

DAC-B is a 6-bit DAC, like DAC-A, and is controlled by the H-PHASE register. Its output voltages can be controlled from 0.5V to 10.5V typically. The output resistance is less than 1kΩ.

DAC-C is a 2-bit DAC and is controlled by the VTRA and VTRC bits. Its typical output characteristic is:

VTRA	VTRC	Output voltage	Output resistance
0	0	12V	7.5kΩ
0	1	5.3V	3.3Ω
1	0	1.7V	1.0kΩ
1	1	0.3V	<1kΩ

All settings in the set that are now manual controls can be made I^2C bus controlled by using one of these DAC's. The only restriction is that the alignment is controlled with a dc voltage. Otherwise an interface circuit is needed.

Appendix B

As a degaussing circuit the following suggestion is given.

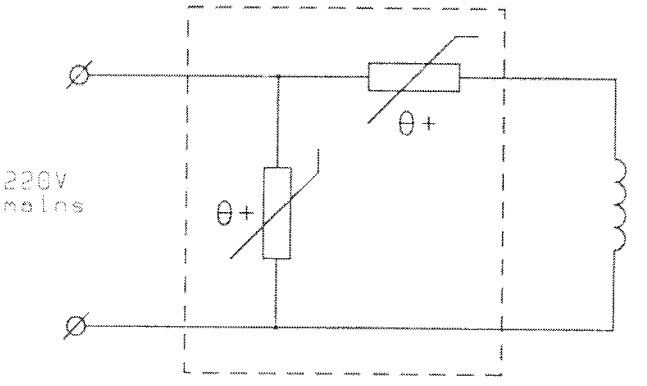
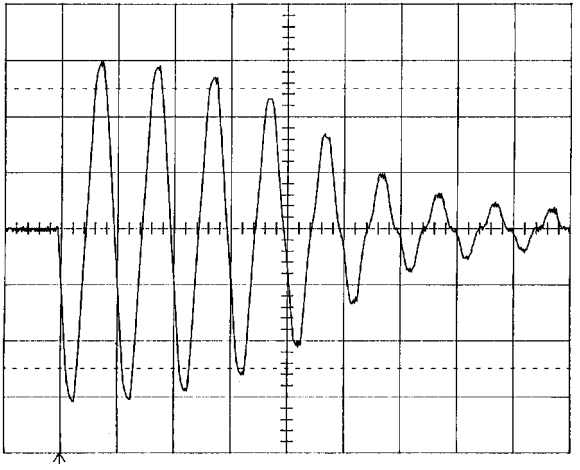


Fig. B1 Degaussing Circuit

Parts list:

Dual degaussing PTC : 2322 662 96116

Degaussing coil : 3111 268 20301



Oscillogram 10:

Current in degaussing coil 2A/div.

SMPS Circuit Examples

4.3.1 A 70W Full Performance TV SMPS Using The TDA8380

The following report describes the operation of a 70W full performance switched mode power supply for use in television.

The TDA8380 SMPS control ic is used in a mains isolated, asynchronous flyback converter configuration.

The power supply incorporates the following features:

- Full mains range (110 - 265Vrms)
- AT3010/110LL SMPS transformer
- BUT11A switching transistor
- Standby (suppression of output voltages by 50%)
- Standby supply (5V, 100mA)
- Facility for synchronisation (using a pulse transformer)
- Short start-up time (less than 0.3 sec at 220Vrms)
- Provision for anti-breathing circuit
- Output voltages 147V/57W, 25V/5W, 16V/7.5W

A full description of circuit operation, a circuit diagram and circuit performance figures are given.

A further additional circuit diagram is included in which the above power supply incorporates a power MOS switching transistor for a mains range of 90 - 135Vrms. Also details are given on an extension to the power capability of the supply, up to 120W output, for European mains using the bipolar switching transistor.

1. Introduction

The TDA8380 control ic has been designed to enable safe, reliable and efficient SMPS to be realised at minimum cost for TV and monitor applications. For further information on the ic, reference should be made to 'Integrated SMPS Control Circuit TDA8380' (ref. 1).

The 70W design employs a currently available AT3010/110LL foil wound transformer and the BUT11A bipolar switching transistor.

Feedback is taken from the secondary side to give less than 1% line and load regulation over the whole range. The output voltage is suitably divided down and compared in an error amplifier with a fixed reference voltage. The error amplifier then drives an optocoupler, which passes the error signal to the primary side directly into the TDA8380. A secondary side error amplifier is used to reduce the importance of the optocoupler characteristics.

Standby is achieved by injecting a signal into the feedback loop on the secondary side, suppressing all output voltages by 50%. A 5V standby supply is available relieving the need for a separate standby supply. During standby conditions the line output oscillator is halted to disconnect the main B+ load.

Synchronisation of the power supply to external control circuits is possible through a loosely coupled pulse transformer.

Appendix A gives a circuit diagram and a short description of the use of the power MOS switching transistor in the 70W supply. The mains range is 90 - 135Vrms.

Appendix B gives notes on how to extend the power capability of the 70W power supply to 105W, 32 kHz and 120W, 30 kHz. Both these power supplies have a mains range of 180 - 265Vrms.

2. TV SMPS design

Flyback versus Forward Converter.

Although this ic can be applied in any type of SMPS, for example in FORWARD (or Buck) or FLYBACK (or Buck-boost) converters, the preferred SMPS type for TV applications is the Flyback converter. This is mainly because it allows for mains isolation of the TV chassis. Other advantages it affords in comparison with a forward converter are:

(a) It does not need 'crow-bar' protection against the input voltage appearing across the chassis in the event of short-circuit failure of the power switching transistor.

(b) The load permissible on auxiliary output supplies is not related (and, therefore, not limited) by the main line timebase supply (B+ voltage) load. Thus the auxiliary supply is available when there is no B+ voltage load, and this is important for servicing and fault finding on a TV chassis.

With the Flyback converter, however, mains pollution and visible interference require to be minimised by careful PCB layout and customarily a mains input filter is used.

Discontinuous versus Continuous Current Mode Operation:

Operation can be in the 'continuous' or in the 'discontinuous' current mode.

In the discontinuous mode the power switching transistor is not allowed to switch on until the SMPS transformer core is demagnetised. This has the advantages:

(a) It is inherently a safer mode of operation, since for all operating conditions, other than a dead-short of the output or a very severe overload transient occurring when the power transistor is conducting near peak current, it is not possible for the core to saturate. To protect for these two exceptions, the very fast (second level) current protection is included.

(b) Steep current pulse edges at switch-on are eliminated (important from point of view of Radio Frequency Interference problems).

Satisfactory performance, in terms of voltage regulation and input mains voltage range, can be obtained using the discontinuous mode which is, therefore, preferred for TV applications.

For this type of converter, the voltage transfer function can be deduced from the Volt-second equilibrium condition for a unity turns ratio transformer:

$$Vi \times d \times T = Vo \times \overline{d} \times T$$

$$\frac{Vo}{Vi} = \frac{d}{\overline{d}} \qquad (1)$$

where: $\overline{d} = (1 - d)$

Taking into consideration the transformer turns ration n = Np/Ns, then:

$$\frac{n \times Vo}{Vi} = \frac{d}{\overline{d}} \qquad (2)$$

where: T = oscillator period
Np = transformer primary turns
Ns = transformer secondary turns
d = on time of output transistor
$\overline{d}$ = conduction time of output rectifier
Vo = output B+ voltage
Vi = input DC voltage

The limit condition for 'discontinuous' current mode operation occurs at minimum input voltage and maximum load.

Thus, for this condition $\overline{d} = (1 - d)$

so that

$$\frac{n \times Vo}{Vimin} = \frac{dmax}{(1 - dmax)} \qquad (3)$$

The power output (including losses supplied via the transformer) is:

$$P = \frac{Vi^2 \times d^2}{2 \times Lp \times f} \qquad (4)$$

where: Lp = primary inductance of transformer
f = frequency of operation

from which general expressions for d, Lp and f can be obtained in terms of the power.

Thus, for a given transformer (n,Lp) the value of dmax can be calculated from (3) and the required frequency of operation from:

$$f = \frac{dmax^2 \times Vimin^2}{2 \times P \times Lp} \qquad (5)$$

The peak current in the power switching transistor is given by:

$$Ip = \frac{Vi \times d}{Lp \times f} \qquad (6)$$

The peak voltage across the power switching transistor (excluding ringing) is:

$$Vi + (n \times Vo)$$

Since most transformers produce ringing, a clamp circuit may be necessary and in order to slow the rising edge of the voltage a snubber circuit is usually required.

3. General circuit description

This section gives an overall general description of the power supply.

Fig. 1 shows a block diagram of the circuit functions. Descriptions of specific circuits will be carried out in the next section.

3.1 Mains filter

This is positioned at the ac mains input. Its function is to minimise mains pollution resulting from RFI generated within the SMPS due to fast transients of voltage and current. It is designed to meet the required mains pollution regulations (C.I.S.P.R. Special Committee on Radio Frequency Perturbation).

3.2 Rectification and Smoothing

The mains voltage is rectified and smoothed to provide a dc supply which is switched through the SMPS transformer.

3.3 SMPS Controller

This drives the power switching transistor regulating the frequency and the amount of current pulsed through the transformer primary. Thus, the controller regulates the energy transferred to the secondary windings. A voltage feedback signal which is representative of the output voltage is fed back to the controller in order to regulate the output voltage. At start up the supply voltage for the controller ic is derived from the rectified mains. A 'take-over' winding on the transformer supplies the ic once normal operation is established.

3.4 Transformer secondary circuits

The dc output voltage is obtained by simple rectification and smoothing of the transformer secondary voltage.

3.5 Feedback Attenuator

The output voltage to be regulated is fed back via an attenuator to the error amplifier.

3.6 Error Amplifier

The error amplifier compares the feedback signal with a fixed reference voltage to give an error signal which is passed to the primary side via an optocoupler.

Mains isolation is provided within the optocoupler and the power transformer, between the input primary and take-over, and the output secondary windings.

4. Detailed circuit description

This section gives a detailed description of each of the functions of the power supply circuit (Fig. 2).

4.1 Mains Input and Rectification

Diodes V1 to V4 rectify the ac mains voltage and, together with a smoothing capacitor C13, provide a dc input HT voltage for the SMPS. R1 is placed in series with the input to limit the initial peak inrush current whenever the power supply is switched on when C13 is fully discharged.

C1 and C3 together with L1 form a mains filter to minimise the feedback of RFI into the mains supply.

C6 to C9 suppress RFI signals generated by the rectifier diodes.

Asymmetrical mains pollution is reduced by the insertion of R26 and C18 between primary ground ('hot side') and secondary earth ('cold side') of the power supply. These components are required to satisfy the mains isolation requirements.

4.2 Control ic TDA8380

This section describes the function of each pin of the TDA8380 and its associated components.

Pin 1 - Emitter of Forward Drive Transistor:

The TDA8380 incorporates a direct drive output stage consisting of two NPN transistors. The collector and emitter of each are connected to separate pins of the ic (pins 1,2,15,16). The forward base drive current for the switching transistor is limited by R15. C16 acts as a voltage source equal to the zener voltage of V7 and is used for the negative base drive.

When the reverse drive transistor is turned on the zener voltage appears across L2, causing stored charge to be removed from the switching transistor, thereby ensuring correct storage time and minimum transistor dissipation during turn-off.

Pin 2 - Collector of the Forward Drive Transistor:

Connected through a resistor to the ic reservoir capacitor.

Pin 3 - Demagnetisation Sensing

Demagnetisation protects the core of the transformer against saturation by sensing the voltage across a transformer winding. In this application operation is in the discontinuous current mode. Sensing is achieved by resistor R10 from the take-over winding of the transformer to pin 3 of the ic. Fig. 3 illustrates demagnetisation operation at low mains where the turn-on pulse is delayed until demagnetisation of the transformer is complete.

Pin 4 - Low Supply Trip:

Connected to the ic ground (pin 14), the low supply protection level is 8.4V.

Pin 5 - IC supply:

On power-up the ic supply is first drawn from C15. This capacitor is charged up directly from the rectified mains through bleed resistors R21 and R24.

Once the SMPS is running, the supply for the ic is taken over by the SMPS transformer. R12 prevents peak rectification of spikes. V8 rectifies the flyback signal which is smoothed by C15 to give a dc level. R16 limits the current drawn by the forward drive transistor. R9 and C5 provide a filtered dc supply to pin 5.

Pin 6 - Reference Current:

This pin allows the external setting of the IC current source. This is set by R11.

Pin 7 - Voltage Feedback:

This is the input to the internal error amplifier for primary side feedback. Feedback in this case is taken from the secondary side and passed through a separate secondary side error amplifier where it is compared with a reference voltage. The error signal is then passed directly into the duty pin (pin 9) via an optocoupler.

To ensure that the Transfer Characteristic Generator (TCG) in the ic remains optional a 'pseudo' feedback voltage from the 'take-over' winding of the SMPS transformer is applied to pin 7. R3 and R4 provide a nominal 2.5V level at pin 7 during normal operation of the power supply.

Pin 8 - Stability:

This is the output of the error amplifier which is left open circuit.

Pin 9 - Duty:

This is the input to the pulse width modulator and is directly driven by the optocoupler transistor. R2, C2 and C27 form a frequency compensation network.

Pin 10 - Oscillator:

The frequency of the internal oscillator is set here by C4 and R11 on pin 6 (nominally 25 kHz).

Pin 11 - Synchronisation:

This is achieved by a loosely coupled pulse transformer passing sync pulses from the secondary to the primary side of the power supply (see later section).

Pin 12 - Slow Start:

The slow start option is selected here by the use of capacitor C11. Fig. 4 shows a typical slow-start.

Pin 13 - Over-Current Protection:

To keep the collector current of V10 within safe operating limits over-current protection is incorporated into the power supply. R27 is the collector current monitoring resistor providing a negative going signal. This voltage is then shifted to a positive level with respect to ground potential by a reference current from the ic flowing through R14. An extra voltage shift is provided by R34 which varies with the ic supply voltage. This is particularly useful in output short circuit conditions. If the main regulated output is progressively short circuited, then all SMPS transformer flyback voltages will decrease, respectively, and hence the shift level of the current protection function leading to lower short circuit output currents (current foldback). The signal at pin 13 is then compared with two internal voltage levels to provide the two forms of current protection.

(The addition of R34 may not work in other power supplies using the TDA8380 because careful attention has to be given to the ratio of current through R34 to current output at pin 13 and to the start-up sequence of the power supply at different mains and loads. Conventional current protection can be achieved by omitting R34 and changing R14 to 13 kΩ and V13 to BYW95C).

Fig. 5 illustrates the current protection waveform.

Pin 14 - Ground

Pin 15 - Emitter of Reverse Drive Transistor:

Grounded to the emitter of the switching transistor.

Pin 16 - Collector of reverse drive transistor.

4.3 Error Amplifier

The external error amplifier consists of two PNP transistors, V15 and V16, connected to form a high gain comparator. The stabilized reference voltage for the comparator is derived from a series-connected resistor R28 and zener diodes V5 and V6 at the SMPS output. The voltage to be compared with the reference voltage is a sample of the 147V output derived from a potential divider (R29, R31 and R5). The optocoupler is directly driven with the error signal from the comparator. The level of the 147V output can be adjusted by R5.

4.4 Standby

In standby mode the power supply output voltages are suppressed to 50% of their normal level. Standby is achieved by reducing the reference voltage used in the comparator circuit and thus the power supply regulates at a lower output voltage level. A +5V dc level is applied to the standby input, which turns transistor V14 on. The voltage reference level is halved from 12.4V to 6.2V and the main 147V output is reduced to 75V. In this condition the power supply still maintains a 5V standby supply. In the television receiver during standby the line output oscillator should be halted to disconnect the main 147V load.

To return the power supply to its normal operating levels, the standby input is removed.

The speed of transition to and from standby is controlled by the time constant of R13, R32 and C23.

4.5 Synchronisation

Synchronisation of the power supply is achieved by a loosely coupled mains isolated pulse transformer. Sync pulses of +5V are applied to the sync input at a frequency slightly lower than the free running frequency of the power supply. R6 limits the current in the primary winding of the pulse transformer and R8 loads the secondary winding. The pulse transformer differentiates the sync pulse input to create negative and positive going transitions of the sync input. The ac coupling (C14) shifts the entire signal positive and the internal circuitry of the ic clamps the negative going excursions to 0.85V. The positive going spikes are removed by a transistor in the ic and the negative going spikes are used to synchronise the oscillator. Fig. 6 shows plots of how the power supply is synchronised to a lower frequency.

A series RC network (C28, R35) is connected from pin 11 to ground to filter out high frequency noise which may interfere with synchronisation.

If the synchronisation option is not to be used, the sync input may be left open circuit. Another alternative is to short-circuit C14 and remove T2.

4.6 Beam Current Limiting (BCL)

Anti-breathing technique, whereby the 147V voltage is reduced for increasing beam current in such a manner as to compensate for the increase in picture size due to the fall in EHT. The components concerned are R30, C24, R7.

4.7 Power Switching Transistor

Pulsing of the transformer is carried out by the BUT11A bipolar power transistor under the control of the TDA8380.

Fig. 7 shows plots of the current through and voltage across the BUT11A. The base drive waveforms are shown in Figs. 8(a)-(b) during standby conditions.

Fig. 9 is a plot of the instantaneous power dissipated in the transistor during turn-off.

4.8 Snubber Network

A snubber network has been added across the switching transistor to protect it from excessive switching dissipation and to suppress ringing on the SMPS transformer.

The dV/dt limiter consists of V9, C17, R22 and R23. When V10 is switched off, part of the energy stored in the leakage inductance of the SMPS transformer will charge C17. When V10 is switched on again this energy is dissipated in R22 and R23. When such a network is omitted, this energy must be dissipated in the switching transistor itself.

R22 and R23 are calculated in such a way that they also act as a network, damping the residual energy in the winding capacitance of the transformer when the secondary rectifiers have stopped conducting.

4.9 Outputs

There are three secondary rectifiers; the 147V (scan voltage for deflection stage), 25V (audio supply) and 16V (small signal supply). The 5V standby supply is derived from a regulator connected to the 16V output.

R25 and C25 form a damping network to dissipate the energy in the high frequency ringing on the B+ secondary winding. Fig. 10 shows the current through and voltage across the B+ winding.

A short circuit or overload of these outputs will cause the power supply to repeatedly go through the slow start procedure.

5. Performance specification

Mains input:		110 - 265V ac	50 - 60 Hz
Outputs:	B+	147 V	57 W
	Audio	25 V	5 W
	L.T.	16 V	7.5 W
	Standby	5 V	0.5 W
Switching frequency:			25 kHz
Efficiency (normal operation):			72 %
Line and load regulation:			0.1 %
Start-up time (220V rms, full load):		300 msec (B+) 225 msec (+5 V standby)	
Max. collector current:		2.3 A	
Max collector voltage:		870 V	
Forward base current:		Normal operation	0.30 A min. 0.39 A max.
		Standby (*)	0.20 A min. 0.24 A max.
ic supply voltage:		Normal operation	18.5 V min. 21.0 V max.
		Standby (*)	8.8 V min. 9.7 V max.

Ripple output voltage (110V rms, 50 Hz, full load):

Frequency	B+ (mV)	L.T. (mV)	Audio (mV)	Standby (mV)
25 kHz	600	230	145	20
199 Hz	230	50	60	-

* The only load in this condition is the standby load.

6. Output short-circuit foldback

The SMPS incorporates duty factor foldback protection for short circuits on the 147V (B+) output. Fig. 11 shows the plot of the foldback characteristic for increasing load on the 147V output using conventional protection and current foldback techniques.

8. References

Ref. 1. "Integrated SMPS Control Circuit TDA8380".
Philips Components Publication Number 9398 358 40011
December 1988.

Appendix A

70W FULL PERFORMANCE USING POWER MOS (BUK456-800A)

A power MOS switching transistor was incorporated into the 70W power supply design. This new power supply has a mains range of 90 - 135V rms. A circuit diagram is given in Fig. 12. Oscillograms of the power MOS gate and drain switching waveforms are given in Figs. 13 and 14.

Alterations to Existing 70W Bipolar Transistor Design

(i) The value of C17 in the snubber is smaller, hence less dissipation in the snubber resistors. The dV/dt at the drain is now higher, but the power MOS transistor has much lower switching losses than the bipolar transistor.

The smaller value of C17 causes the 100 kHz ringing on the primary winding of the SMPS transformer after flyback to be more prevalent. This ringing has an effect on the demagnetisation function causing premature operation. To overcome this a resistive divider network has been used on pin 3 to minimise the effect of ringing.

(ii) The value of R14, the current protection shift register, is increased. This is to compensate for the fact that the power MOS transistor does not suffer from storage effects at turn-off.

(iii) The filtering on the take-over winding for the ic supply is increased. This is because the average current demanded by the gate drive of the power MOS is much less than in the case of the bipolar transistor. Energy in switching spikes on the flyback voltage cannot be channelled into the gate of the power MOS and so has to be dissipated in increased filtering.

A smaller value for the gate-source resistor is used to provide extra loading on the transformer winding.

(iv) C13 is increased to filter the higher current ripple at low mains voltages.

(v) A larger heatsink for the switching transistor is necessary due to the higher on-resistance of the power MOS transistor facilitating the need for higher heat dissipation.

Performance Specification

Mains supply:	90 - 135V rms		
Switching frequency:	20.8 kHz		
Outputs:	B+	147 V	57 W
	Audio	25 V	5 W
	L.T.	16 V	7.5 W
	Standby	5 V	0.5 W
Regulation:	0.1 %		
Peak drain voltage:	650 V		
Peak drain current:	2.3 A		
Start-up time	300 msec		

Addendum

Alternative Cheap BUT11A Base Drive Design Eliminating 5 W Zener Diode

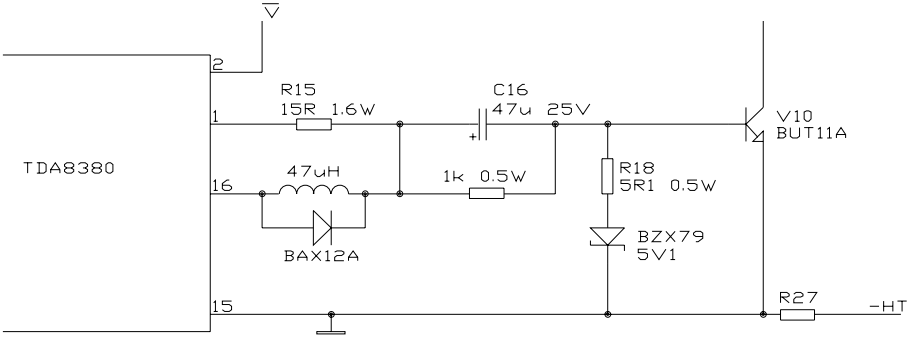


Fig. A1 - Alternative Cheap BUT11A Base Drive.

An alternative base drive for the power switching transistor (BUT11A) has been designed to eliminate the 5W zener diode 1N5339B (V7) to reduce cost.

Alternative Low Cost Base Drive

This design has not been implemented into a PCB design yet, but the existing PCB design requires little alteration to accommodate the changes.

When the forward drive resistor is turned on at the start of the duty cycle, a current defined by R15 passes through C16 and into the base of the BUT11A. The 1 kΩ resistor in parallel with C16 discharges the capacitor when the SMPS is off to help starting at low mains. When the reverse drive transistor is turned on, the 5.1V zener diode appears across C16 clamping the voltage across it, thus a reverse current flows from the base of the BUT11A through C16 and L2 turning off the power switching transistor. Some forward current does flow through the 5.1V zener diode, but not enough to warrant a power zener. The BAX12A diode across the inductor is to prevent large negative going spikes appearing at pin 1 of the ic; this can also be used in the previous base drive.

Base Measurements

Forward base current:	250mA min 400mA max
Standby mode (standby load only)	190mA min 250mA max
BUT11A storage time:	1.4µsec

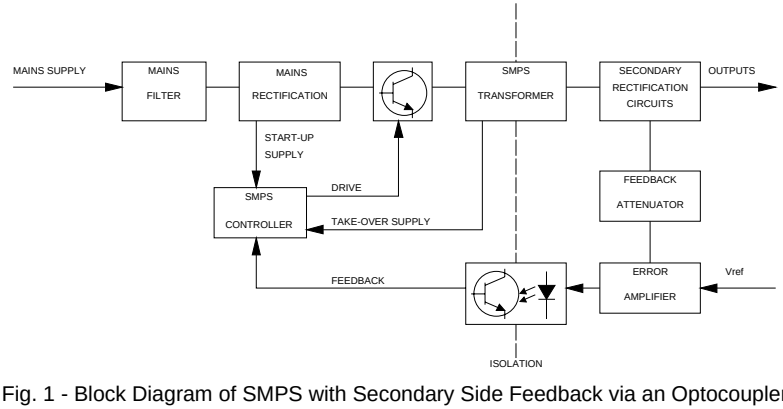


Fig. 1 - Block Diagram of SMPS with Secondary Side Feedback via an Optocoupler

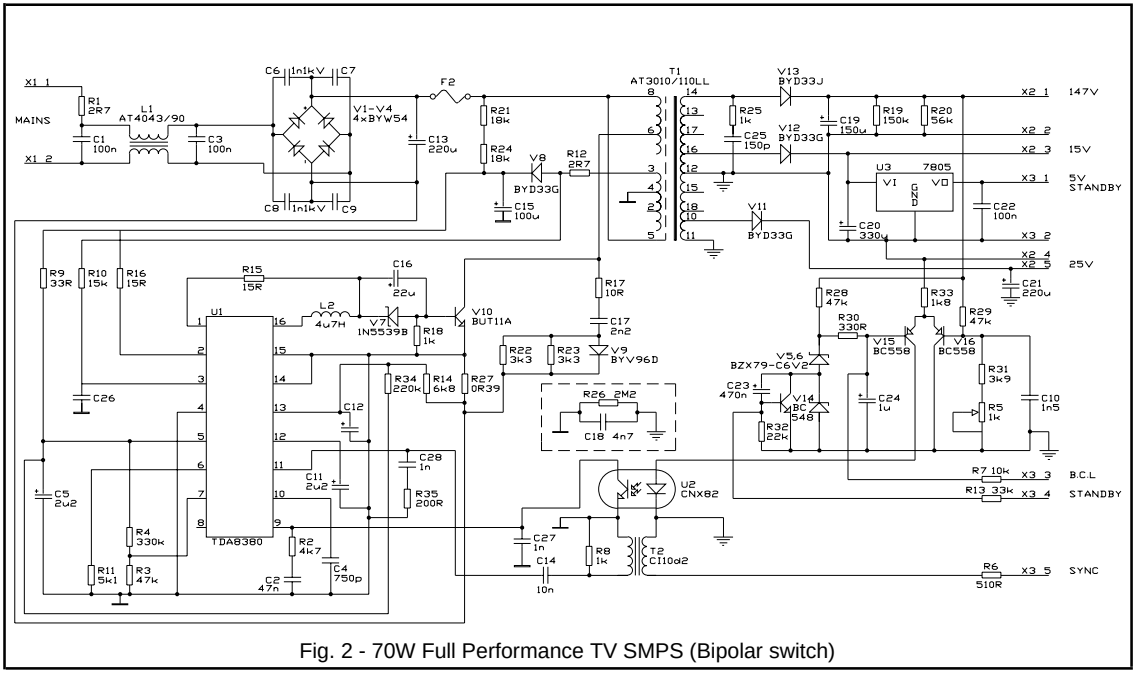


Fig. 2 - 70W Full Performance TV SMPS (Bipolar switch)

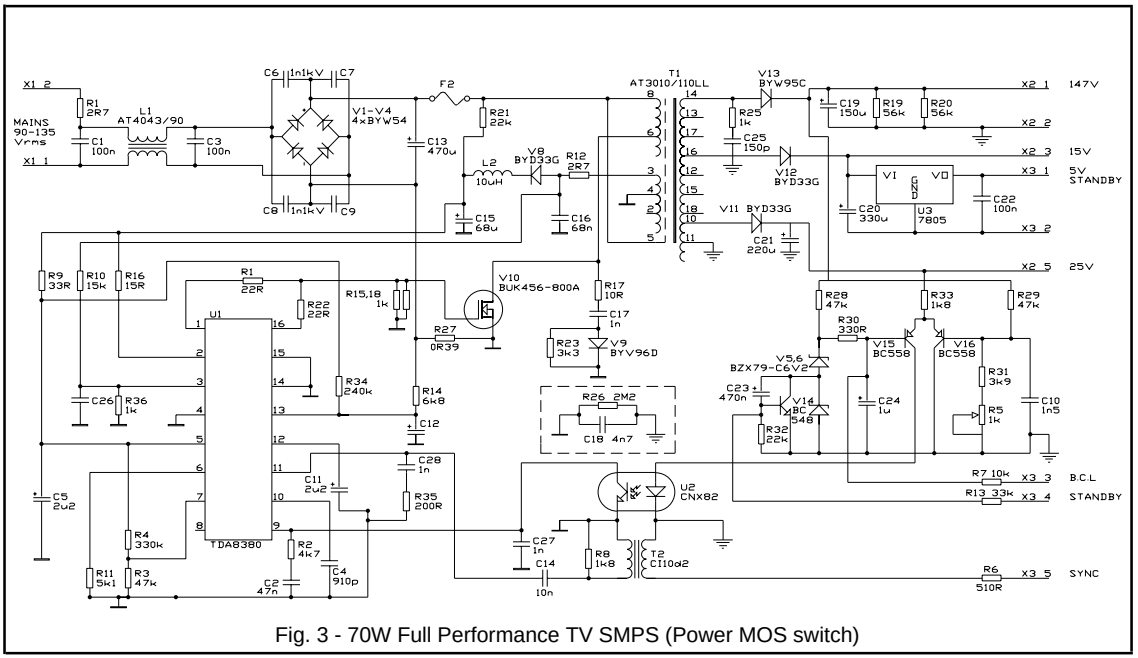


Fig. 3 - 70W Full Performance TV SMPS (Power MOS switch)

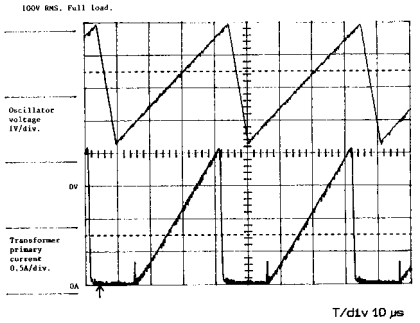


Fig. 4 - Demagnetisation operation. Oscillogram of the Oscillator Waveform and Transformer Primary Current

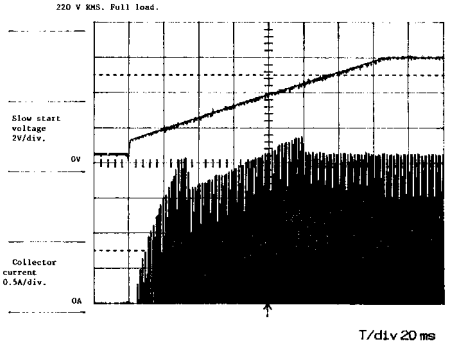


Fig. 5 - Slow Start. Oscillogram of the Voltage at the Slow Start Pin (TDA8380) and Current through the Switching Transistor.

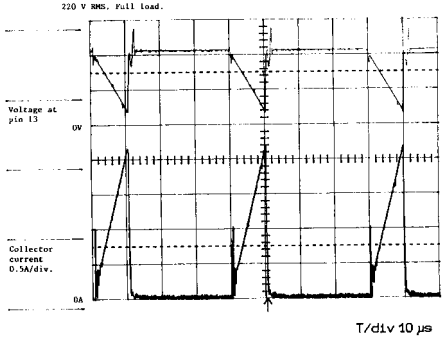


Fig. 6 - Current protection. Oscillogram of voltage at Pin 13 (TDA8380) and the Current through the Switching Transistor

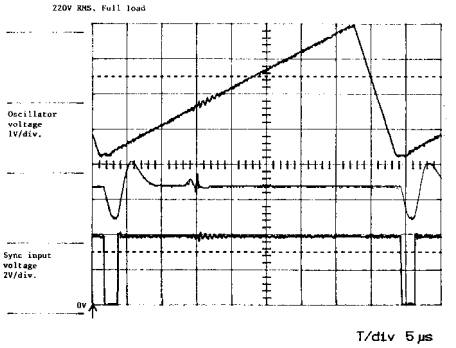


Fig. 7 - Synchronisation. Oscillogram of Oscillator Voltage, Voltage at Pin 11 (TDA8380) and Sync Input Voltage

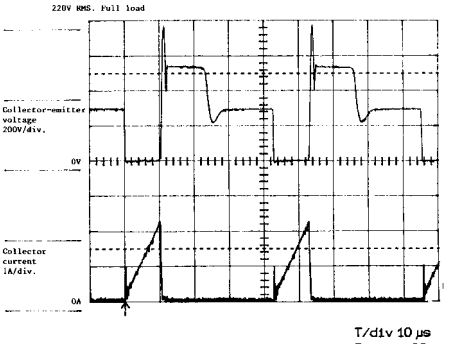


Fig. 8 - Switching waveforms. Oscillograms of the current through and voltage across BUT11A.

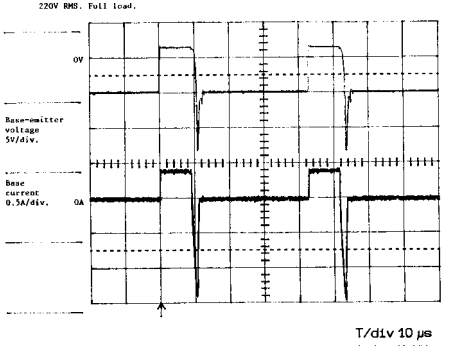


Fig. 9 - BUT11A Base Waveforms. Oscillograms of Base-Emitter Voltage and Base Current Waveforms for BUT11A

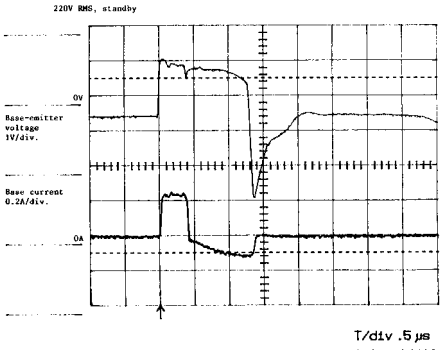


Fig. 10 - BUT11A Base Waveforms During Standby. Oscillograms of Base-Emitter and Base Current Waveforms for BUT11A in Standby Conditions

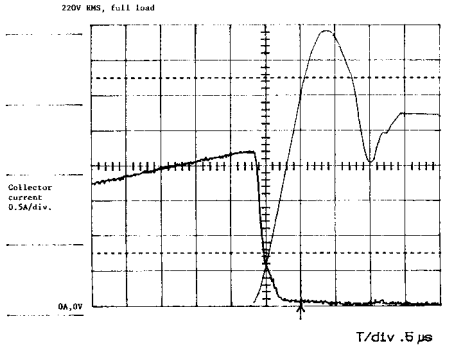


Fig. 11 - Turn off dissipation in BUT11A. Oscillogram of Collector-Emitter Voltage and Collector Current for BUT11A

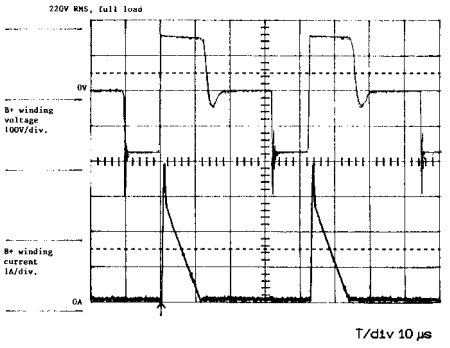


Fig. 12 - B+ Winding. Oscillogram of Voltage Across and Current Through the B+ Winding

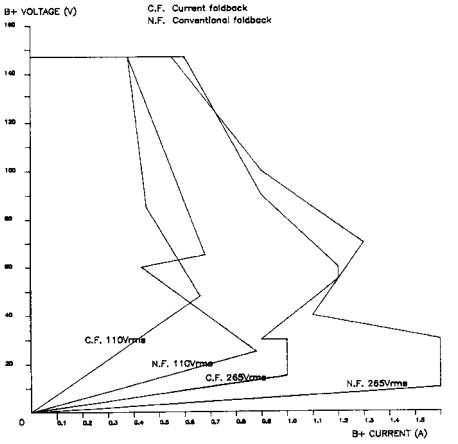


Fig. 13 - Plot of Duty Factor Foldback using Current Feedback and Conventional Foldback Techniques

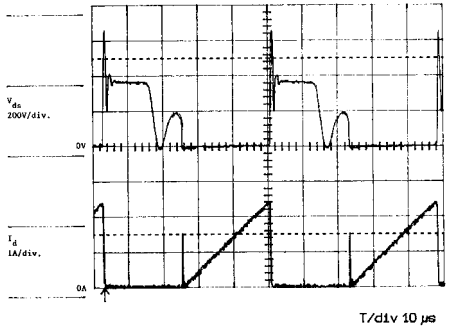


Fig. 14 - Oscillogram of Drain-Source Voltage and Drain Current for Power MOS Transistor (BUK456-800A) at Full Load, 110V rms

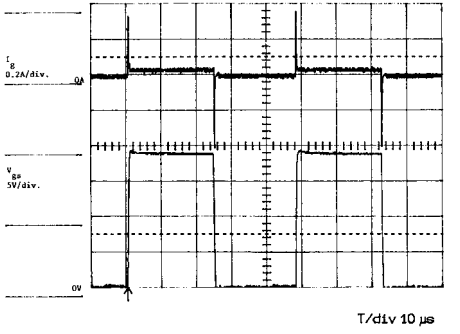


Fig. 15 - Oscillogram of Gate Current and Gate Source Voltage for Power MOS Transistor (BU456-800A) at Full Load, 110V rms

4.3.2 A Synchronous 200W SMPS for 16 and 32 kHz TV

Description of 200W Switched Mode Power supply incorporating the AT3020/01A transformer, the TDA8380 control IC, one opto-coupler for feedback, synchronisation and remote on/off. The SMPS is intended for TV and can be synchronised to 32 kHz by flyback pulses of either 32 or 16 kHz. A 5V standby supply is also provided.

1. Introduction

In this report a description is given of a 200W SMPS circuit and evaluation board, incorporating the TDA8380 control IC, the new SMPS transformer AT3020/01A and the BUW13 power switching transistor. The SMPS is a flyback converter that has been designed to handle a maximum average output power of 200W and a peak power of 250W. The free running frequency of the SMPS is 34 kHz, while it can also be synchronised down to 32 kHz by either 16 or 32 kHz line flyback pulses. For testing purposes no pre-loading is required. The circuit operates at a mains input voltage of 185-265V_{RMS}, 50-60Hz. The output voltages are 150V, 32V and 16V. The 150V output is short circuit proof, while the 32V and 16V can be made short-circuit proof.

A new wire wound SMPS transformer has been designed. This transformer, the AT3020/01A with an EE46/46/30 core (grade 3C85), has a new winding technique which makes the RFI screens superfluous. Thanks to its low leakage inductance, the efficiency of the system is high (88%).

The control IC TDA8380 receives its start-up supply from the rectified mains voltage. The takeover supply is derived from a flyback and forward auxiliary winding on the transformer. This IC offers many attractive operating features: it directly drives the power switching transistor and incorporates several overload protections.

Due to its high current h_{FE}, the BUW13 was chosen as the power switching transistor. For an output power of up to 150W, the BUT12 can be used. A CNG82 opto-coupler is used for feedback. If synchronisation is not required, the cheaper CNX82A can be used.

For the supply of some digital IC's in the standby mode, a small self-oscillating supply is used: the so called µSOPS (5V, 300mA). In the standby mode the output voltages will be fully suppressed.

A printed circuit board (no 3634) is available incorporating the 200W SMPS and µSOPS but without mains filter.

2. Circuit description

2.1 Block Diagram

Fig.1 shows the block diagram of the 200W mains isolated flyback converter.

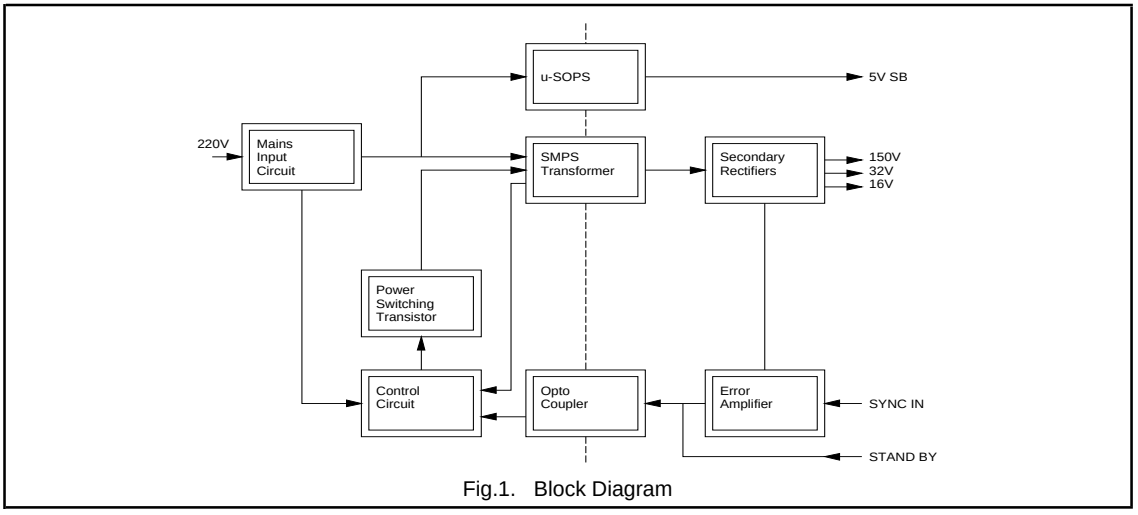


Fig.1. Block Diagram

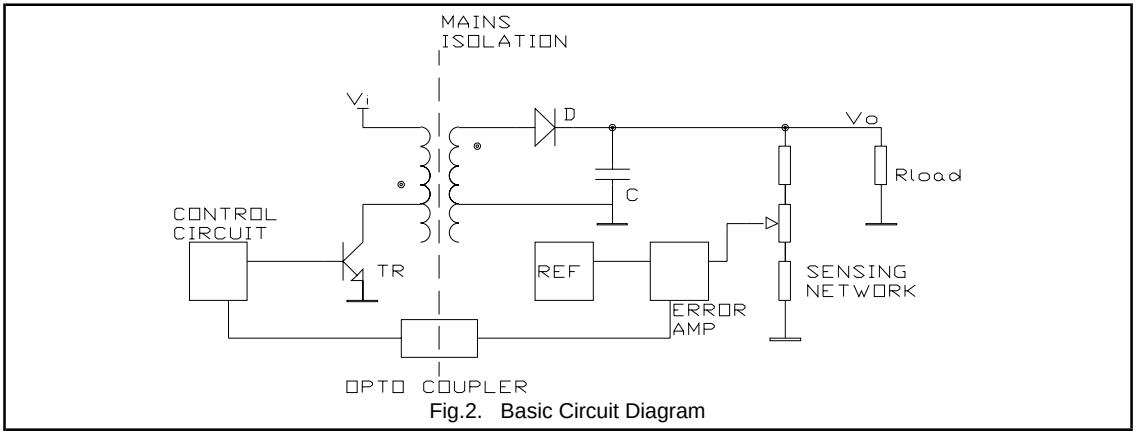


Fig.2. Basic Circuit Diagram

The 200W SMPS evaluation board does not contain an RFI filter, fuses or a degaussing circuit. These components should be located on the inlet of the mains cord into the TV set. The mains input voltage is rectified by bridge rectifying diodes and the dc supply to the SMPS transformer (AT3020/01A) is smoothed by a 220µF buffer capacitor. The control IC TDA8380 derives its start-up supply from this dc voltage and as soon as the IC supply voltage exceeds a certain limit, the IC is initialised. Hereafter, the duty factor of the SMPS power switching transistor (BUW13) increases slowly from zero upwards and its rate of increase is controlled until the SMPS output voltage reaches its nominal level. The take over supply is derived from a flyback and forward rectifier connected to an auxiliary winding of the SMPS transformer. The SMPS is a flyback converter that operates in the discontinuous mode. At the secondary side the flyback voltage is rectified. One of the output voltages is fed back via an attenuator circuit to the error amplifier. The error signal is sent back via the opto-coupler circuit to the duty cycle control input of the IC TDA8380.

For standby purposes the µSOPS delivers a 5V supply. In the standby mode the output voltages will be fully suppressed. The SMPS runs at a fixed frequency of 34 kHz, however, it can also be synchronised down to 32 kHz by either 16 or 32 kHz line flyback pulses.

2.2 Basic Operation

Fig.2 shows the basic circuit of the mains isolated flyback converter.

The control IC TDA8380 directly drives the power output transistor. When the transistor conducts, a linear increasing current flows through the primary winding of the transformer. As a consequence energy is stored in the transformer. After switching off the transistor, the stored energy is transferred into the load via diode D. The attenuated output voltage Vo is compared with the reference voltage, REF, in the error amplifier. The error signal is fed back via the opto-coupler to the control IC. By controlling the duty cycle of the drive pulses the output voltage Vo is kept constant.

The flyback converter under discussion has been designed for the discontinuous current mode. The principle of this circuit has already been described in chapter 2 "Switch Mode Power Supplies". For a nominal output voltage of 150V, 185V_{RMS} mains, a maximum load of 250W and a fixed free running frequency of 34 kHz, the primary inductance of the transformer can be calculated. The required primary inductance is Lp = 420µH ± 10%.

An attractive feature of this SMPS is that it can be synchronised down to 32 kHz by either 16 or 32 kHz line flyback pulses.

3. Circuit diagram

The circuit diagram is given in section 8, Fig.3; detailed information about several parts of the supply follows.

3.1 Mains input

The diode bridge D1 to D4 rectifies the mains input voltage and the dc supply to the SMPS is smoothed by C5. Capacitors C1 to C4 suppress the RFI generated by the diodes in the mains bridge rectifier. If C5 is fully discharged, the inrush current has to be limited by R1 to protect the bridge rectifier diodes. During continuous operation of the SMPS this resistor is for efficiency reasons short circuited

by a thyristor, THY1. After the soft start of the SMPS, thyristor THY1 is fired continuously by the peak voltage clamp of the SMPS via R3 and C6.

3.2 Start-up supply

The control IC TDA8380 receives its start-up supply from the mains rectified voltage by the low wattage resistor R4. The IC is initialised as soon as the voltage on the supply pin 5 reaches 17V. This takes approximately 1.5s (Oscillogram 6). Shorter times are possible by lowering the value of R4. During the time leading up to the initialisation of the IC, the base coupling capacitor C10/C11 is pre-charged. So, the power switching transistor T1 is switched off correctly during the start up period. With a duty cycle from zero onwards, the SMPS starts up. The take over supply is derived from a forward and flyback auxiliary winding on the transformer (AT3020/01A). The forward rectifying diode D7 ensures that a temporary decrease of the supply voltage of the IC is restricted. After a while the flyback rectifying diode D6 directly provides all the current needed by the IC. During continuous operation of the SMPS the supply voltage for the IC is about 17V.

3.3 Control IC

The integrated SMPS control circuit TDA8380 offers many attractive operating features. It controls the SMPS power throughput and regulation by pulse-width modulation. It can directly drive the power switching transistor and it can operate at a fixed frequency or a line locked frequency. A detailed description is given in Reference [1]. The function of each pin is described below.

Pin 1 Emitter of the forward drive transistor. It directly drives the power transistor with a source current of about 0.7A.

Pin 2 Collector of the forward transistor. This pin is connected via R14 to the supply. Resistor R14 and R15 mainly determine the source current of the power switching transistor.

Pin 3 Demagnetisation sensing. For this flyback converter, operating in discontinuous mode, the voltage across the SMPS transformer is sensed via R12 and R13.

Pin 4 Low supply-voltage protection level. This pin is connected to ground, so the min. V_{cc} of the IC is set at 8.4V.

Pin 5 IC supply. When the mains input is applied to the SMPS, the IC supply reservoir capacitor C9 is charged by a current determined by resistor R4. When the voltage at pin 5 reaches 17V, the IC initialises and diode D6 rectifies the flyback signal from winding 10/11 of the SMPS transformer to supply the IC with 17V.

Pin 6 Master reference current setting. Resistor R11 sets the master reference current for the TDA8380 to 600μA.

Pin 7 Voltage feedback and overvoltage protection. The flyback signal from winding 10/11 of the SMPS transformer is smoothed by D6/R7/C9, to give a dc level that varies in proportion to variations in the 150V output. This level is reduced by the divider R9/R10 and fed to pin 7.

Pin 8 In this application the feedback amplifier of the TDA8380 is not used. However, an overvoltage on pin 7 will still activate a protection and slow start sequence.

Pin 9 Output of the error amplifier. Not used.

Pin 10 Oscillator. A 680pF capacitor C15 is connected to this pin; together with resistor R11 (4k3) the oscillator frequency is set to 34 kHz.

Pin 11 Synchronisation. The trailing edge of the positive sync-pulses, which are superimposed on the linear feedback signal, synchronise the oscillator.

Pin 12 Slow-start (capacitor C17) and maximum duty cycle (R20).

Pin 13 Over current protection. The over current protection safeguards the power switching transistor for being overloaded with a too high collector peak current. For that reason resistors R22 to R26 in the emitter circuit of the power switching transistor sense the collector current. This negative going signal is dc shifted into a positive signal with respect to ground by a dc current from pin 13 flowing through R21, while C18 removes the spikes.

Pin 14 Ground

Pin 15 Emitter of the reverse drive transistor, connected to ground.

Pin 16 Collector of the reverse drive transistor. See drive of the BUW13 SMPS power transistor.

3.4 SMPS Transformer

As already mentioned before, the transformer (AT3020/01A) has been designed to handle a maximum output power of 200W and a peak power of 250W. The nominal primary inductance is 420μH. To keep the leakage inductance (~2%) as small as possible, a turns ratio of 1:1 was chosen. The magnetic circuit of the transformer comprises two Ferroxcube E46/23/30 cores, grade 3C85. The coil is built-up in layers of copper wire, separated from each other by insulation foil. Thanks to a clever winding design no screens had to be applied, and as a result, the size of this transformer could be reduced significantly with respect to the transformer described in Reference [2].

The energy stored in the leakage inductance will be dissipated in the dV/dT limiter (D8/C13/R19) and peak voltage clamp (D5/C7/R5); the energy stored in the parasitic winding capacitance in the power switching transistor T1 and damping networks (R6/C8 and R37/C28).

3.5 Power switching transistor

By fixing the primary inductance of the transformer and its operating frequency, the collector peak current of the power switching transistor is fixed. At a peak output power of 250W the I_c peak is approximately 6.5A. On the other hand, the maximum base drive is determined by the control IC TDA8380: $I_{source\ max}$ = 0.75A. The BUW13 has a sufficient high current gain and, moreover, the I_{boff} could be kept within the limit of the control IC: $I_{sink\ max}$ = 2.5A. For slightly lower maximum power (150W) the BUT12 can be used as the power switching transistor. Note that, in that case, current sensing resistor R21 has to be reduced.

The correct forward drive of the transistor is provided by the supply voltage of the IC and R14/R15, resulting in an I_{bon} of 0.7A. To obtain a correct negative base drive, the bias voltage across C10/C11 is kept constant by three BAW62 diodes (D9 to D11). During turn off, inductor L1 (1.7μH) in combination with the bias voltage, determines the negative base current (-dI/dt) of the power switching transistor. R17 and C12 damp the ringing of the base-emitter and prevents parasitic switch on of T1 during the flyback.

3.6 Secondary rectifiers

The three secondary flyback rectifiers deliver the 150V (line deflection supply), 32V (audio supply) and 16V (small signal supply). A 12V stabiliser is not provided on the PC board. The load determines the dissipation in the rectifying diodes and hence the size of the heatsink (D15) and copper area. The number of electrolytic capacitors is determined by the load (ripple current) and the ESR of the capacitors.

To prevent interference between the SMPS switching frequency and the line frequency an L-C filter has been added. The inductor is L2 while the capacitor is located on the line deflection board. If the SMPS is running in the synchronous mode, the filter action is not required and L2 can be replaced by a 1 Ω resistor. The feedback voltage for the control circuit is taken in front of this L-C filter.

To prevent cross-talk, the audio supply is brought out floating. The negative of the 32V supply is connected to ground via R38 to prevent static charge of this transformer winding if kept unused. If there is an overload on the 32V or 16V supply, the currents in the secondary transformer windings can be excessive before the over-current protection of the IC is activated. The use of a fuse or fusible resistor (1Ω / 4W) at position J3 and a fusible resistor (1Ω / 1W) at J4 will make the SMPS short circuit proof also on these two outputs.

3.7 Error amplifier

The error-amplifier consists of a single transistor T5. The base of this transistor receives the filtered and divided output signal while the emitter is connected to the reference voltage (ZD3). The output current of this error-amplifier is fed to the opto-coupler. As the current through T5 and hence its gain will settle at a value inversely proportional to the current gain of the opto-coupler, the SMPS loop gain will be independent of tolerance or ageing of the opto-coupler. The current through ZD3 is fixed by R42 at 2mA. By keeping it constant, the temperature dependence of the Vbe of T5 is compensated by that of ZD3 [3].

3.8 Opto-coupler

For feedback and mains isolation an opto-coupler (CNG82) is used. As already mentioned before, the opto-coupler is driven in such a way, that the large variation of IC/IF of the opto-coupler is filtered by means of R27 and C19. The emitter of the transistor drives the output-amplifier T2. This transistor is used for keeping the operating voltage of the phototransistor constant; this keeps the bandwidth high.

Except for feedback, the opto-coupler is also used for synchronisation. For this purpose, the sync pulses are superimposed on the linear feedback signal. The slower CNX82A can also be used at the expense of the wave-shape and delay of the sync pulse. Then at 16 kHz the maximum power will be restricted somewhat due to unequal duty factors of the odd and even SMPS pulses.

For standby operation, the opto-coupler diode is driven in forward (IF = 2mA) either by switch-on transistor T6 or by externally driving resistor R43. In this mode the output voltages will be switched off.

3.9 Standby supply

For the supply of some digital IC's in the standby mode, a small self-oscillating, current-mode controlled flyback converter delivers 5V/300mA. It uses the same mains input filter, bridge rectifier and RFI/safety capacitor C22 as the main SMPS. For mains isolation and power conversion a small transformer (AT3006/300) is used. The power switching transistor BUX87 requires a small heatsink [4].

4. Synchronisation

The SMPS can be synchronised down to 32 kHz by either 16 or 32 kHz (±4%) negative-going pulses on pin 5 of J17, with a pulse width of 18% of the line time (Eg. line flyback pulses). The amplitude of the sync-pulse measured at the sync-input, should lie between 2 and 6V. The sync-pulses are superimposed on the linear feed back signal. This can only be done, if they do not affect the voltage stabilisation. To obtain short rise and fall times of the sync-pulse at the sync-input of the TDA8380, the CNG82(A) should be used. Capacitor C16 ac couples the sync-pulses to pin 11 of the

TDA8380. The oscillator sawtooth is triggered by the trailing edge of the positive sync-pulse at pin 11 and all subsequent sync-pulses are ignored until the oscillator sawtooth is completed. The oscillator is then inhibited until the end of the next positive sync-pulse. The free-running oscillator frequency is determined by R11 (4k3) and C15 (680pF). Both components should be 1% tolerance types.

If synchronisation of the SMPS is not needed, the following components can be deleted: C19, C35; R29, R27, R49, R50, R51; D18, R19; T2. The opto-coupler CNG82 can be replaced by the CNX82A. Jumpers J1 and J2 should be in place.

5. Mains interference

RFI measurements are made of the SMPS (200W) together with the µSOPS and a mains input filter, consisting of the AT4043/93 and two X-capacitors (220nF). The results must stay below the limits of EN55013, which are drawn in the graph shown later. The measurements just meet the limits. If the SMPS is used with more than 165W input power, measures must be included to meet the IEC552-2 standard on mains pollution by higher harmonics.

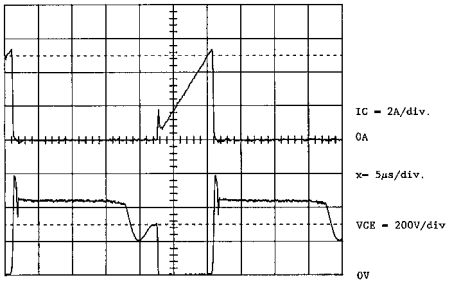
6. Performance

INPUT	185-265V RMS		50/60Hz
OUTPUTS	150V 1.0A STABILISED		LINE SCAN
	32V 1.5A UNSTABILISED		AUDIO
	16V 0.2A UNSTABILISED		SMALL SIGNAL
RIPPLE peak to peak	150V	≤10mV	SWITCHING FREQUENCY
		≤20mV	100Hz
	32V	≤150mV	SWITCHING FREQUENCY
		≤10mV	100Hz
	16V	≤50mV	SWITCHING FREQUENCY
		≤10mV	100Hz
EFFICIENCY	88%		200W LOAD
SWITCHING FREQ.	34kHz		

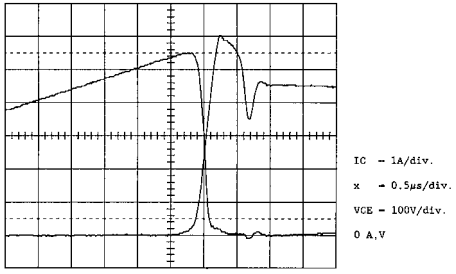
7. Oscillograms

The oscillograms have been made at the following conditions, unless otherwise indicated.

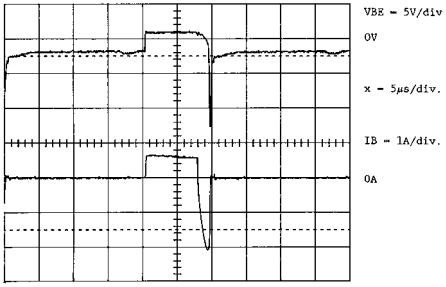
V_{input} = 220V RMS Load = 200W not synchronised.



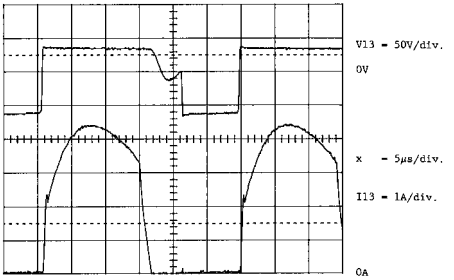
Oscillogram 1. Collector Current and Collector Voltage of the BUW13.



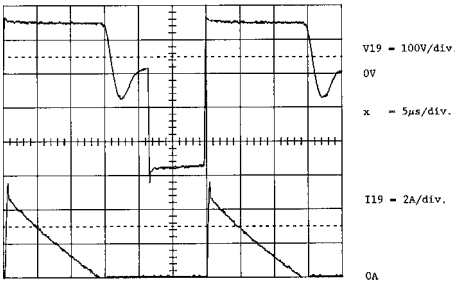
Oscillogram 2. Collector Current and Collector Voltage of the BUW13.



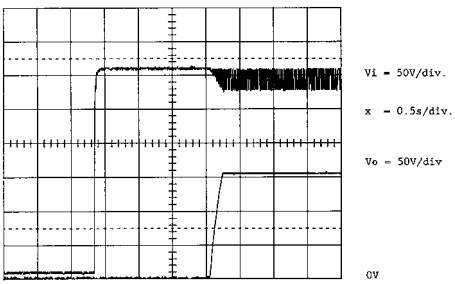
Oscillogram 3. Base Emitter Voltage and Base Current of the BUW13.



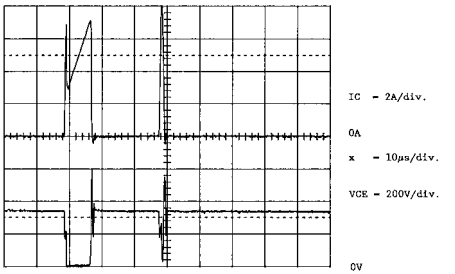
Oscillogram 4. Voltage and Current at pin 13 of the transformer.



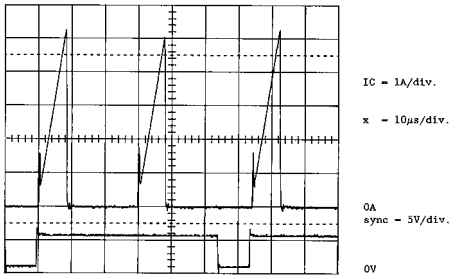
Oscillogram 5. Voltage and Current at pin 19 of the transformer.



Oscillogram 6. SMPS switch on behaviour.



Oscillogram 7. BUW13 Collector Current and Voltage at short circuit 150V output.



Oscillogram 8. BUW13 Collector Current and 15.625kHz sync pulses.

References

Information for this section was extracted from "Synchronous 200W Switched Mode Power Supply for 16 and 32 kHz TV"; ETV89009 by H.Simons.

[1] Integrated SMPS control circuit TDA8380. Philips Semiconductors Publication Number 9398 358 40011 Date: 12/88.

[2] ETV8711 A 200W switched mode power supply for 32kHz TV. Author: H.Misdom. Date: 01/09/87.

[3] ETV89003 Novel optocoupler circuit for the TDA8380. Author: H.Verhees. Date: 2/89.

[4] ETV8834 A dual output miniature stand by power supply. Author: H.Buthker.

8. Circuit diagram.

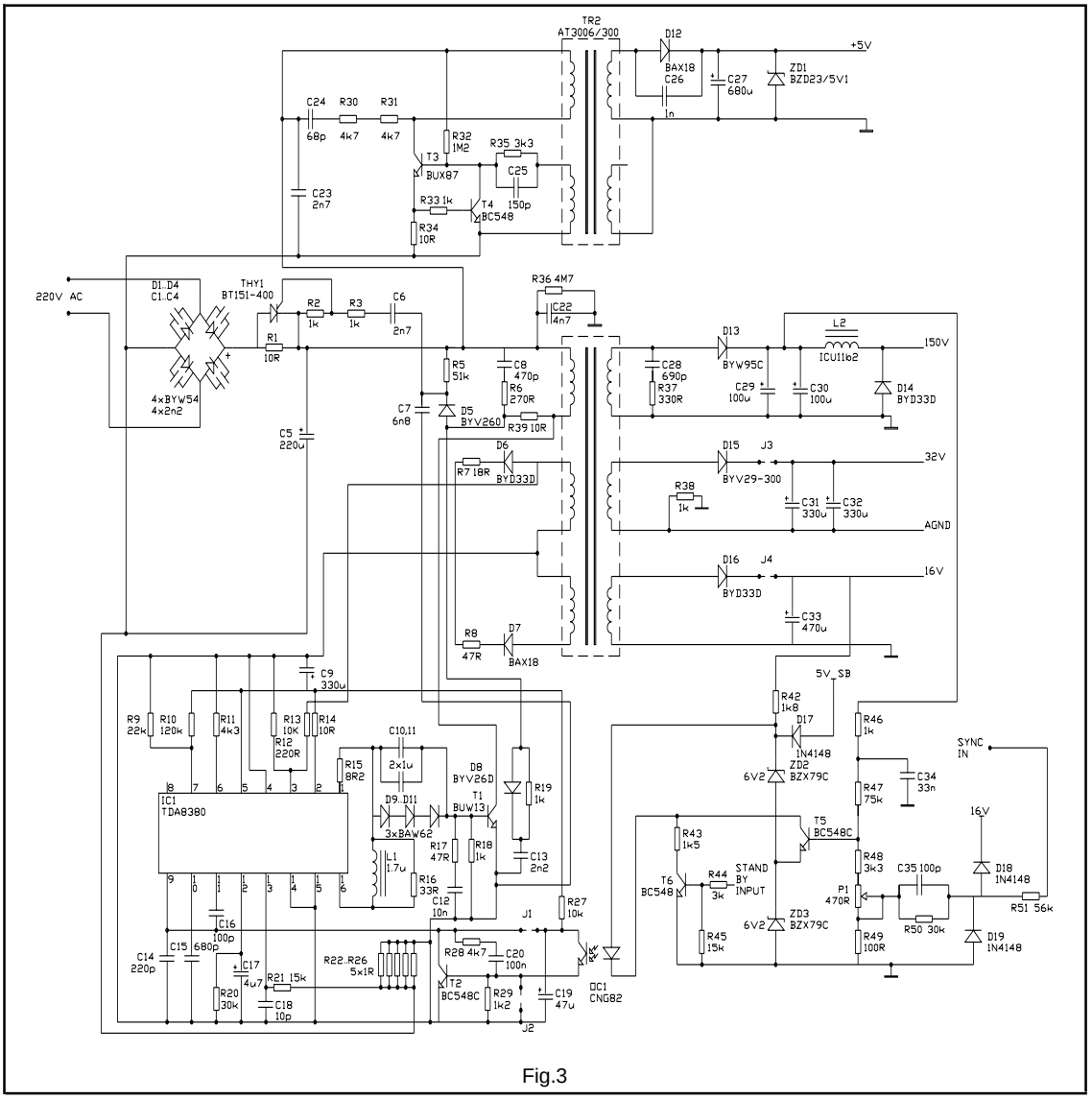
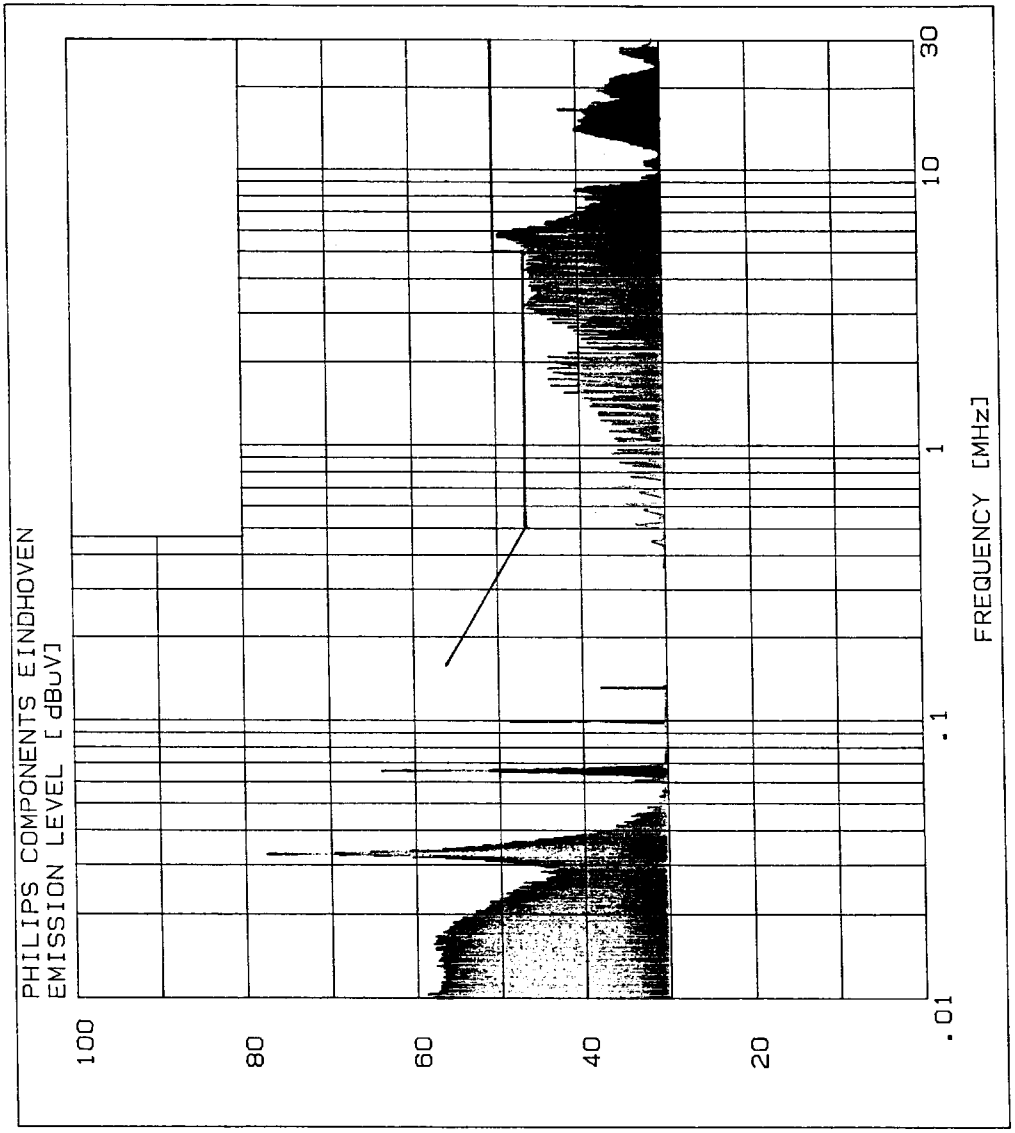


Fig.3

9. RFI measurement



Monitor Deflection Circuit Example

4.4.1 A Versatile 30 - 64 kHz Autosync Monitor

This section describes the supply and deflection circuits for driving the 15" FS M36EDR colour monitor tube. Key features of this monitor design are auto synchronisation, full mains range, dc control, good picture stability and high contrast. The circuit uses a low number of components without making compromises to the performance.

1. Introduction

The increasing number of suppliers of video interface cards, creates a variety of video standards. The most widely used standard at this moment is the VGA mode. Already this standard gives a choice of three different modes, giving resolutions between 720x350 to 640x480 pixels. The horizontal frequency is fixed at 31.5 kHz, while the vertical frequency varies between 60 and 70 Hz.

New standards, with resolutions up to 800x600 and even 1024x768 pixels, are becoming popular very rapidly, although the old standards are still present on these new interface boards.

This increase in resolution calls for larger screens, compared to the nowadays widely spread standard 14" tube, due to the minimum discernible detail at a convenient viewing distance. Furthermore, the electronic drive circuits of the picture tube have to be able to adapt to the various standards.

As a successor of the standard 14" high resolution colour picture tube, the 15" Flat Square M36EDR series tubes offer a noticeable increase in useful screen area (14": 190x262 mm2; 15": 210x280 mm2), while the total cabinet size hardly increases, and offering a resolution up to 1024x768 pixels (pitch is .28mm.). The M36EDR series offers a wide range of deflection impedances and an excellent performance with respect to convergence and geometry distortion, resulting in simple deflection electronics. For the end user, the tube offers a very pleasant flat and square screen, with hardly any disturbing visible effects.

To display the new, as well as the old video standards, on this new tube, the electronic circuits are becoming more complex. For example, to display 768 lines, without disturbing screen flicker, the line frequency must be increased to 57 kHz. The horizontal deflection circuit described in this report is able to synchronise over a continuous frequency range from 30 to 64 kHz, while the vertical frequency may vary between 50 and 110 Hz. The circuit is built around the advanced monitor deflection controller TDA4851, significantly reducing the component count of the total circuit, while providing a high standard of performance. The vertical deflection output stage is the TDA4861. This power operational amplifier offers the designer great flexibility with respect to input signals and supply voltages.

The increase in resolution also demands that the video channels are able to drive the picture tube with ever higher frequencies, due to the increasing amount of pixels on one video line in a decreasing period of time (increase of line frequency). For example, to display 1024 pixels on one line at 57 kHz line rate, the video amplifiers must be capable of handling dot frequencies up to 65 MHz.

This report covers the electronic circuits for driving the horizontal and vertical deflection coils of a 15"FS tube, for generating all the grid voltages necessary for this tube (the cathodes are driven by the video amplifiers), and a full mains range supply, generating the supply voltages.

2. Supply

This autosync monitor is equipped with a full mains range switched mode power supply (90 - 265Vac) with a maximum output power of about 90W [1]. This mains isolated power supply is running asynchronous, because of the large frequency range of the horizontal deflection stage.

To handle the required output power a new wire wound SMPS transformer, the CE422v, was designed. The controller IC is the TDA8380 [2] directly driving the power switch BUT11A. Feedback is obtained through an opto-coupler circuit that senses the +155V output, the line supply voltage. The output voltages of the SMPS are:

+ 155 V	@ 350 mA	Horizontal deflection and EHT generation
+ 10.5 V	@ 450 mA	Vertical deflection
- 10.5 V	@ 650 mA	Vertical deflection and CRT heater
+ 30 V	@ 30 mA	Vertical deflection (flyback)
+ 12 V	@ 400 mA	Video, IC and small signal supply

The +12V supply is derived from the +17V supply rail by means of a separate voltage stabiliser.

An extra winding on the transformer, not used in this circuit, delivers a -17V supply. The rectifier and smoothing capacitor are not implemented in this design.

As this switched mode power supply is running asynchronous, additional measures are taken to prevent interference. All output lines are equipped with LC or RC filters.

The +155V rail is protected against short circuit by means of the TDA8380, while the +12V output is protected by the IC voltage stabiliser. To make the low voltage outputs protected against short circuit, fuses or non flammable resistors are used in the output lines.

2.1 Degaussing

The demo monitor is equipped with a conventional automatic degaussing circuit, making use of one duo PTC. For full mains range application the inrush and steady state current are just on the limit. If support is needed please contact the local or regional sales/application office.

2.2 Provisions for full-mains range

To make the SMPS full mains range the following provisions are made:

The slow start capacitor C15 is reduced to 0.47µF to shorten the start up time.

The overcurrent protection is extended in order to ensure proper working of the IC with respect to the first trip level.

The IC supply capacitor C13 is increased to 220µF to prevent excessive voltage drop during start up.

3. Deflection

The deflection circuit is greatly simplified by making use of the advanced monitor deflection controller TDA4851. This is an upgraded version of the TDA4850 mainly with respect to horizontal line jitter. To accommodate a horizontal frequency range from 30 to 64 kHz, the input frequency is continuously monitored by an F/V converter, in order to adapt the central frequency of the TDA4851. The minimum and maximum frequencies of this circuit are limited by an upper and lower clamp.

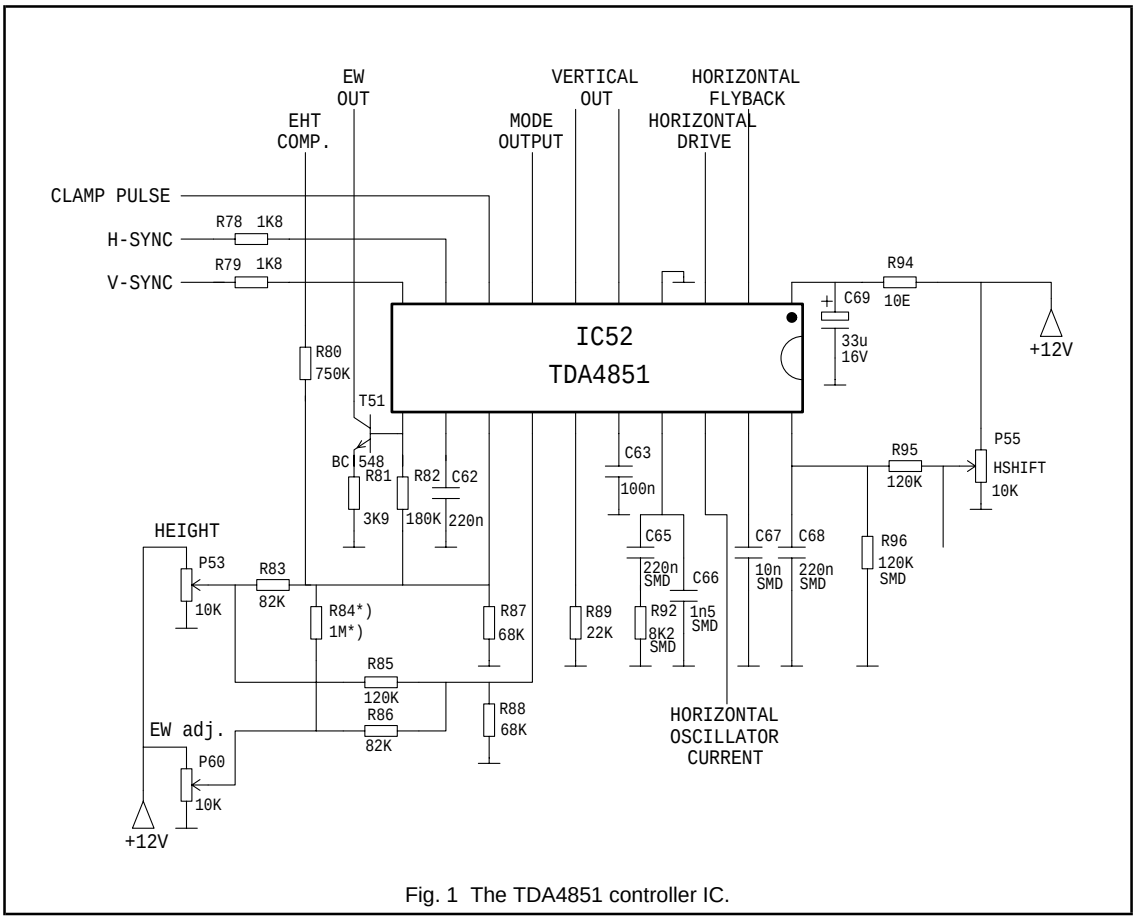


Fig. 1 The TDA4851 controller IC.

The TDA4851 drives a line driver stage and a, so-called, T-on driver stage. The line driver is of the well known transformer coupled non-simultaneous type, giving the designer a free choice where to put the line output transistor with respect to the supply voltage. The T-on driver stage drives a switching transistor, synchronised with the horizontal frequency to control the horizontal scan voltage. The conducting period of this switch is kept constant over the whole frequency range, resulting in a constant picture width, independent of the scan frequency.

The TDA4851 also drives the vertical output stage TDA4861. DC coupling of the deflection coil to this amplifier, together with the high linearity of the drive signals from the TDA4851, offer an excellent linear vertical deflection, without bouncing effects after a mode change.

East-west correction of the horizontal deflection and picture width control is performed by the width control stage.

Horizontal S-correction is performed by one fixed capacitor, plus a selection of three additional capacitors. This minimum set-up is chosen to keep the circuit simple, while giving the minimum amount of distortion at four selected frequencies. The S-correction capacitor selection circuit drives floating FET switches.

Vertical S-correction is achieved by modulation of the vertical amplitude control current with a parabola voltage.

The line output transformer AT2090/01 generates the anode, focus and grid 2 voltages for the picture tube. The built-in bleeder with smoothing capacitor provides an excellent source for retrieving EHT information. This information is used to stabilise the picture width and height.

The primary winding of the line output transformer is also used as the choke of the switch mode scan control stage. This architecture has the advantage of using only four wire wound components: LOT, bridge coil, base drive transformer and horizontal linearity coil.

The auxiliary windings on the line output transformer deliver supply voltages for the grid-1 circuit and video output stages and provide information for the protection circuit.

The various circuits will now be discussed in detail in the next sections.

3.1 Advanced monitor deflection controller TDA4851

The heart of the deflection circuit is the advanced monitor deflection controller, the TDA4851, see Fig. 1. This deflection controller is driven by separate horizontal and vertical synchronisation pulses. Although the TDA4851 can process a sync-on-green signal, this is not implemented in this monitor. The polarity of these pulses can be chosen freely, except for VGA modes, their amplitude must be TTL level. With these pulses, the horizontal and vertical oscillators are synchronized. The horizontal output drives the line driver, the vertical drive signals are connected to the vertical output stage IC51. A parabola voltage for driving the east-west correction stage and a clamping signal for the video stages are also generated by the TDA4851.

3.1.2 Horizontal part

The horizontal oscillator is synchronized with the pulse on pin 9: TTL amplitude, positive or negative polarity and accepting composite sync (sync-on-green is not implemented in this design). The catching range is limited to ±6.5%. The oscillator frequency is set by C67 and the dc current in pin 18, which in this application is set by a dc current source, driven by the frequency to voltage converter. Compared to the TDA4850, the current in pin 18 of the TDA4851 is approximately 10 times higher to achieve a lower phase jitter.

The low-pass filter in the first phase locked loop is connected to pin 17. In a single frequency application, the values of the filter components are fixed. For a frequency range from 30 to 64 kHz, the values of the filter components are set by the lowest frequency, resulting in a less than optimum response for the higher frequencies. For reasons of simplicity, the filter is fixed here, but should be adapted to the actual frequency for best response.

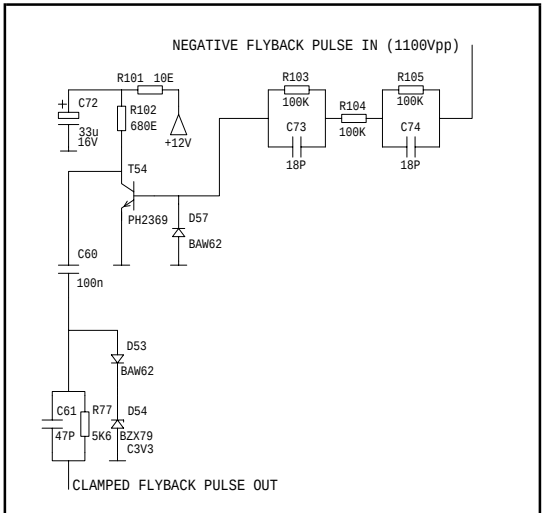


Fig. 2 Horizontal flyback pulse coupling to the TDA4851.

The synchronised horizontal oscillator drives the second phase locked loop, in which the horizontal flyback pulse is used as feedback to position the horizontal drive pulse in relation to the horizontal sync pulse. Low-pass filtering is performed by capacitor C68 connected to pin 20. Phase shift can be accomplished with a dc current in pin 20.

Nominal phase shift is set with resistor R96. User adjustable phase control is available through P55, controlling the dc current in pin 20.

The horizontal flyback pulse is connected to pin 2. The TDA4851 expects a positive flyback pulse, see Fig. 2. The negative flyback pulse from the line output stage is inverted and ac coupled to pin 2 of the TDA4851.

3.1.3 Vertical part

The vertical oscillator can be synchronized with a pulse on pin 10 (or combined sync to pin 9) over a range of 50 to 110 Hz without adjustment and with constant amplitude output signal. Frequency determining elements R89/C63 and the amplitude stabilisation loop capacitor C62, should not be changed.

The output signals of the vertical part are two balanced currents, available on pins 5 and 6. Both currents consist of an equal dc part and an adjustable sawtooth part. The adjustment is achieved by means of controlling the dc current in pin 13. There are five signals which determine the current in pin 13:

1. R87 sets the nominal dc current;
2. P53 allows user control of the picture height via R83;
3. By means of R82, the amplitude control current is modulated with a parabola current. In this way, vertical S-correction is achieved. The disadvantage of this method, is that the amount of S-correction is dependent on the setting of the east-west control potmeter P60.
4. R84 compensates for a change of the east-west correction voltage (explanation: when the east-west voltage on pin 11 is changed by means of the 'EW par.' potmeter P60, the mean dc voltage on pin 11 changes, influencing the vertical amplitude via R82). The influence of the east-west setting on the vertical amplitude is small, therefore, R84 is marked optional, it's not absolutely necessary.
5. Changes in the EHT voltage compensate the vertical amplitude via R80.

3.1.4 East-west parabola

A parabola voltage is available on pin 11, for driving the pincushion correction stage. The bottom of this parabola voltage, equal to the middle of the screen, is set internally on 1.2V, independent of the amplitude setting. In this way, adjusting the parabola amplitude changes the horizontal width in the corners only, while the amplitude in the middle of the screen remains constant.

Amplitude adjustment of the parabola voltage is achieved by a dc current in pin 14. No user control is available, adjustment is only possible with P60 on the main deflection/supply printed circuit board. The amplitude of the parabola voltage is corrected for changes in the vertical amplitude setting by means of R85. The amplitude of the parabola voltage is independent of the vertical scan frequency.

The parabola voltage from pin 11 is connected to the base of T51. The collector current is then transferred to the picture width driver. In that stage the amplitude is multiplied with the horizontal frequency, to achieve a correction independent of the horizontal frequency.

3.5 Miscellaneous I

A clamping signal for the video pre-amplifier, ic TDA4881, is generated in the TDA4851. This clamping signal is available on pin 8, and is only present when horizontal sync pulses are present on pin 9.

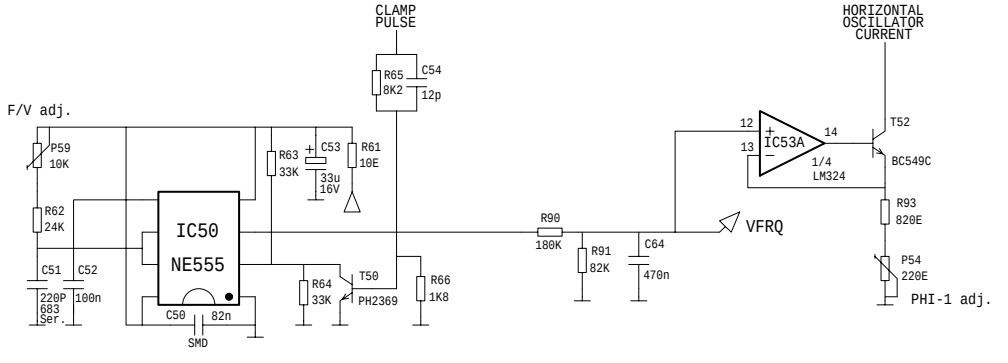


Fig. 3 Frequency to Voltage Converter and Current Source.

The mode input/output pin 7 is connected to a switching transistor T76. This transistor is driven by comparator IC56B. This comparator detects whether or not the incoming horizontal frequency is below 33 kHz. In this case, the TDA4851 assumes a VGA signal is present, resulting in an automatic adjustment of the vertical amplitude, depending on the sync. polarity. Above 33 kHz, the internal mode detector of the TDA4851 is switched off with T76, to prevent automatic vertical amplitude adjustment.

3.2 Additions to the TDA4851 for auto-sync operation

Since the catching range of the horizontal section of the TDA4851 is only ±6.5%, the frequency range from 30 to 64 kHz cannot be covered without extra circuits. To accommodate the specified range, the horizontal oscillator current (pin 18) is constantly adapted to the incoming horizontal sync pulse frequency. This is achieved by means of a frequency to voltage converter driving a current source. To protect the power output stages from too low and too high frequencies, voltage clamps on the drive voltage of the current source keep the frequency of the horizontal oscillator of the TDA4851 within the specified limits of 30 to 64 kHz.

3.2.1 F/V Converter

The frequency to voltage converter is built around one-shot IC50, see Fig. 3. R65/66 attenuate the signal from pin 8 of the TDA4851 in such a way that only the horizontal clamp pulses (5.5Vpeak) and the vertical blanking pulses (1.9Vpeak) do not drive T50. This has the advantage that the incoming horizontal sync pulse is not disturbed in any way, and the sync pulse polarity and amplitude variations of the incoming sync pulse are of no influence to the circuit.

The output pulses of IC50 pin 3 are attenuated and filtered with R90/91 and C64. The dc voltage VFRQ is used to drive the current source and the S- correction capacitor selection circuit. The width of the output pulse of the one-shot can be adjusted with P59 (F/V adj.). This potmeter should be adjusted in such a way, that the switching of the S-correction capacitors is performed at the desired frequencies.

The conversion factor S of this F/V converter is:

$$S = \{t_c + 1.1 \times (R_{62}+P_{59}) \times C_{51}\} \times \{R_{91} / (R_{90}+R_{91})\} \times U_o$$

where:

t_c width of the TDA4851 clamp pulse: 1µs

$1.1 \times (R_{62} + P_{59}) \times C_{51}$ width of the output pulse of the one-shot IC50: 5.81 - 8.23µs

$R_{91} / (R_{90} + R_{91})$ attenuation of the output pulse: 0.313

U_o amplitude of the output pulse: 10.8V

The duration of the output pulse of the one-shot is affected by the trigger pulse. During time t_c the output voltage is already high, while the charging of C51 is halted. This results in:

$$S = 23.0 \text{ to } 31.2 \text{ mV / kHz}$$

The voltage VFRQ can be found with the following formula:

$$V_{FRQ} = F_H \times S$$

where F_H is the horizontal scan frequency. With S = 27.1mV/kHz, this results in:

$$V_{FRQ}(31.47 \text{ kHz}) = 31470 \times 27.1 \times 10^{-3}$$

$$V_{FRQ}(31.47 \text{ kHz}) = 853 \text{ mV}$$

and:

$$V_{FRQ}(63.69 \text{ kHz}) = 63690 \times 27.1 \times 10^{-3}$$

$$V_{FRQ}(63.69 \text{ kHz}) = 1726 \text{ mV}$$

Because the resistor divider for the s-correction capacitors is fixed, the conversion factor S is adjusted to the voltage VREF, feeding the divider.

3.2.2 Current source

The current source for driving pin 18 of the TDA4851 is build around op. amp. IC53A and T52.

The collector current of T52 can be adjusted with P54 to adapt to the actual conversion factor S and for the tolerance on the oscillator capacitor C67 on pin 19 of IC52. This must be done after the conversion factor S is adjusted with P59 to the correct s-correction switching frequency.

3.2.3 Voltage clamps

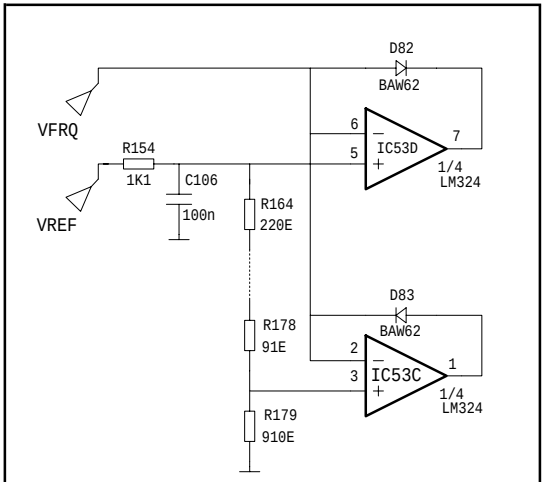


Fig. 4 Voltage clamps.

To prevent the horizontal power output stage from running at either too low, or too high, a frequency, the drive voltage for the current source is limited. IC53C limits the lower voltage and IC53D the upper voltage, see Fig.4. The frequency range of the TDA4851 is now limited to 30 kHz minimum and 66 kHz maximum.

Reference for the comparators IC53C/D is a voltage divider network, driven by IC53B. The input voltage for IC53B is the temperature compensated reference voltage at pin 15 of the TDA4851.

3.3 Horizontal scan control driver

In order to keep the picture width constant, independent of the horizontal scan frequency, the scan voltage is continuously adapted. The relation:

$$V_{scan} = L \times I \times f_H$$

is valid. From this equation, it can be seen that with increasing scan frequency, the supply voltage must also increase proportionally.

Realisation of this demand is in fact quite simple. The horizontal drive pulse from the TDA4851 triggers one-shot IC54. The output pulse width of this one-shot is constant, independent of the trigger frequency. Therefore, the duty-cycle increases with increasing frequency. Via buffer stage T62/63, FET switch T64 is controlled. In this way, the scan voltage for the horizontal deflection output stage is controlled, according to the previously stated relation.

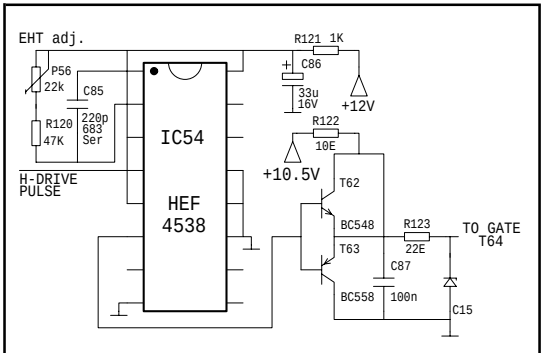


Fig. 5 Horizontal Scan Control Driver.

IC54 is a retriggerable one-shot, see Fig. 5, which is important at higher scan frequencies (above 66 kHz), where the duty-cycle becomes 1.0. In case of a non-retriggerable one- shot, the duty-cycle would suddenly drop to 0.5. This would not only result in half the deflection amplitude, but also in a drop of the EHT.

One other important item is the phase relation between the drive pulses of T53 and T64. When the horizontal output stage is in the flyback part, T64 must always conduct (in order to keep the EHT constant). This is realised by choosing the appropriate trigger edge (positive edge of the horizontal drive pulse) and by a lower limit of the adjustment range of the pulse width, to ensure T64 is conducting all through the flyback period of the horizontal deflection stage.

3.4 S-correction capacitor selection

The necessary value of the S-correction capacitor varies with the horizontal frequency, given a certain deflection coil impedance and screen radius. The correct capacitor value is chosen from eight different values through a combination of one fixed and a choice of three capacitors.

The voltage VFRQ, representing the horizontal scan frequency, is connected to the inverting inputs of seven comparators IC56/57. Each non-inverting input of these comparators is connected to a different output of a resistor ladder R154/164-170/178/179. This resistor ladder is fed by a voltage VREF.

At pin 15 of IC52 a temperature compensated voltage of, typically, 3.0V is available for setting the vertical oscillator current (R89). To avoid extra loading of this pin, a voltage follower with high input impedance IC53b is used. The output of op. amp. IC53b is a stable dc voltage with very low output impedance: VREF.

Resistors R171 to R177 provide each comparator with some hysteresis to prevent parasitic oscillations on the switch-over points.

The comparator outputs are connected to an 8-3 multiplexer IC58. The outputs of IC58 drive transistors T73/74/75. These transistors can withstand the possible high voltages (max. 150V) that drive the S-correction capacitor switches.

D79/80/81 are added to prevent T73/74/75 from break down during line flyback. In this way, the selection of the resistors sets the frequencies when the circuit switches to another S-correction capacitor value.

3.5 Picture width driver

Since pin-cushion distortion is a fixed percentage of the scan voltage, the peak to peak parabola voltage, correcting the pin-cushion distortion, must be adapted to the actual scan frequency. This multiplication is achieved in the same manner as the scan voltage for horizontal deflection is adapted.

One-shot IC55, see Fig. 7, is triggered with pulses having the same frequency as the horizontal scan frequency. But now, also the parabola voltage modulates the width of the output pulse. This output pulse is integrated through R138/C98; the voltage drives a common base stage T69.

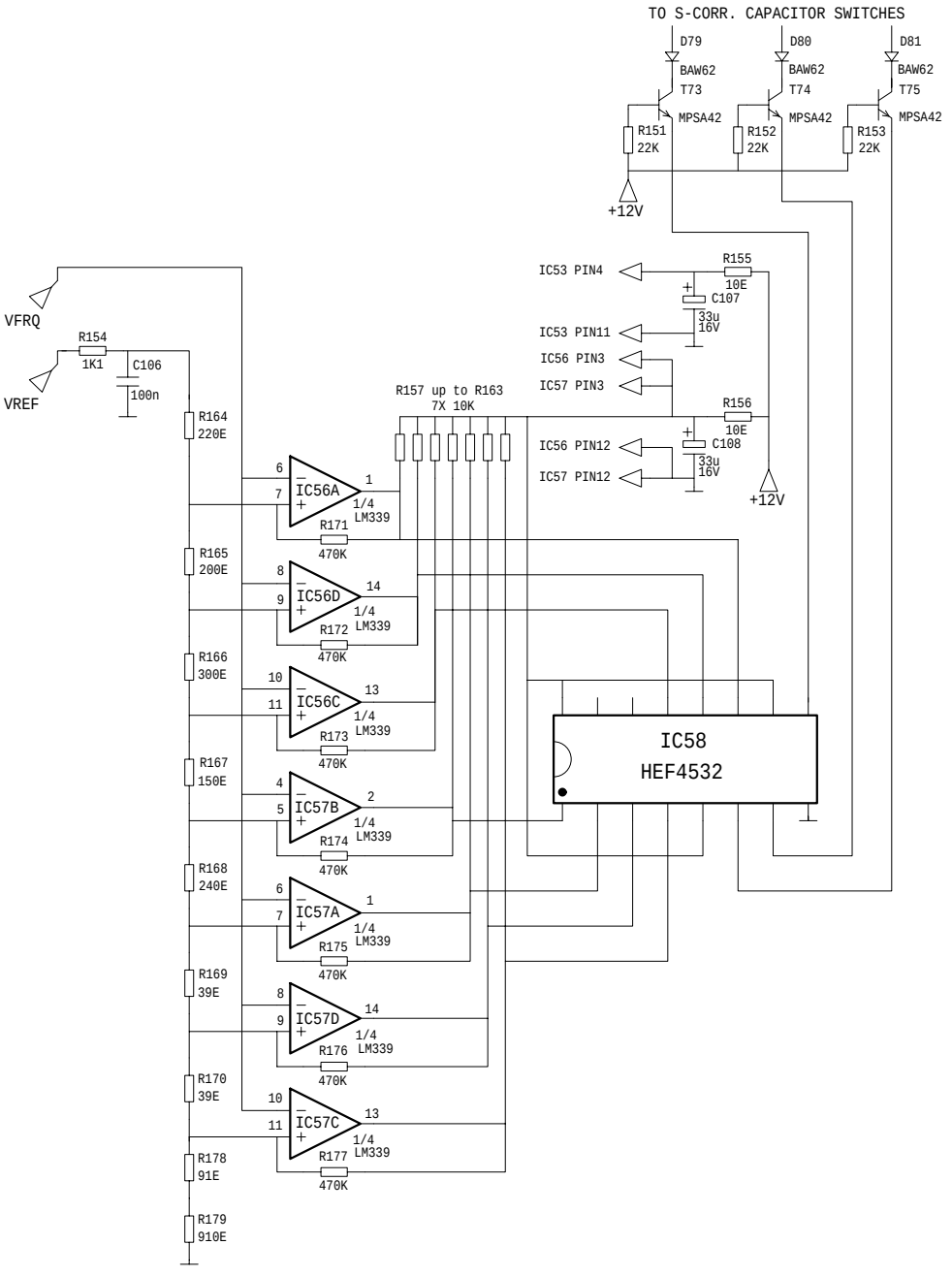


Fig. 6 S-Correction Capacitor Selection Circuit.

In this way, the modulation is converted to the collector current of T69 (IEW), simplifying the interface to the east-west power stage, which is connected to the +155V supply.

Two other functions are also incorporated in this part of the circuit:

- User control of the picture width via P58; and
- Compensation for variation of the EHT; achieved through R136 - the information is supplied by the EHT compensation circuit.

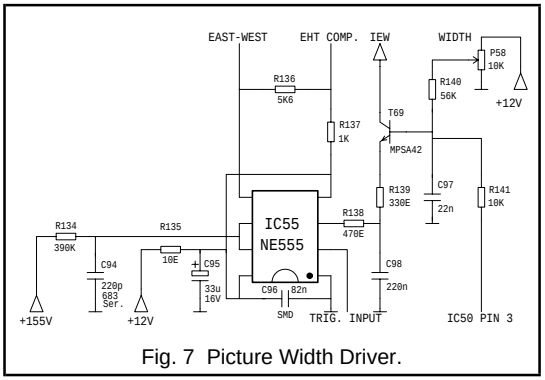


Fig. 7 Picture Width Driver.

3.6 Horizontal deflection output stage

To allow a frequency range of 30 to 64 kHz, additional measures have to be taken to keep the deflection current and the EHT constant. This is realised by continuously adapting the scan voltage to the horizontal frequency by means of the horizontal scan control. The scan control switch T64 is connected to ground, resulting in simple gate drive. The horizontal deflection output transistor T55 is connected to the supply rail because the driver transformer L50 already provides isolation. The primary winding of the Line Output Transformer L54 is used as a choke.

This set-up of horizontal deflection has two disadvantages:

1. The pincushion correction stage is either floating or connected to the same supply rail as the line output transistor, T55. In this concept, connection to the supply rail is chosen, and driving it with a current IEW from the small-signal circuit.
2. The S-correction capacitor switches are floating, which makes it less simple to drive them.

The biggest advantage of this deflection stage is that a minimum of wire wound components has been used.

3.6.1 Line driver stage

The circuit is shown in Fig. 8. As driver device T53 a small MOSFET (BSN274) is chosen. Its advantages over a bipolar device on this particular application are: less power dissipation (enabling smaller encapsulation), less drive power required, better switching behaviour and no storage time (so no additional stress on the Φ_2 loop). To protect the gate the standard precautions (zener diode and series resistor) are taken.

The driver transformer is equipped with a damper network at the primary side (C71/R98) to damp excessive ringing. On the secondary side a damper (C76/R107) is present between the base and emitter of the deflection transistor T55.

In order to achieve sufficient negative drive voltage during flyback, resistor R106 and diode D58 are added. Proper $-dI_b/dT$ is achieved by the leakage inductance of L50.

When the X-ray protection is activated, the inverting driver stage will be turned on continuously. This will switch off T55, but also cause a low frequency swing in the driver transformer. To prevent voltage inversion across the primary winding of driver transformer L50, which would turn on the deflection transistor T55 for a relatively long time, D55 is added. A second measure, that must be implemented when X-ray protection is installed, is increasing the power rating of the current source resistor R97 to 16W (!) or using an electronic resistor with a current fold back characteristic.

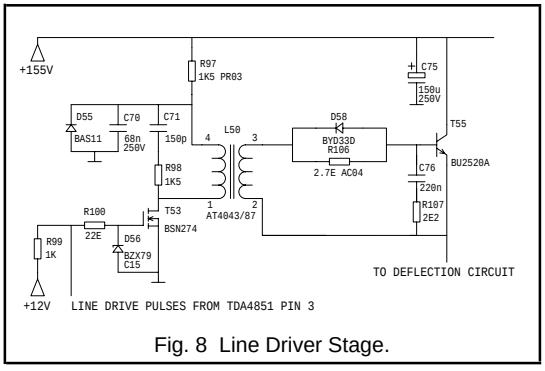


Fig. 8 Line Driver Stage.

3.6.2 Horizontal scan control output stage

At double the line frequency, the scan voltage must be doubled as well to have the same picture width on the screen. Furthermore, the supply voltage to the line output transformer must be proportional to the horizontal line frequency to have constant EHT over the whole frequency range. To achieve this, a synchronous switching series regulator is added. This series regulator operates with a constant T-on time.

In Fig. 9 the basic circuit diagram and in Fig. 10 the relevant waveforms are given.

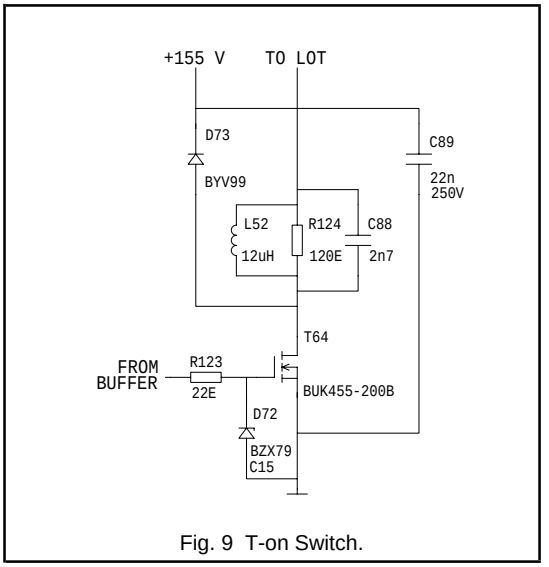


Fig. 9 T-on Switch.

Transistor T64 controls the horizontal supply voltage and, hence, the peak value of the flyback pulse which is directly related to the horizontal amplitude and EHT (flyback time is fixed, independent of frequency).

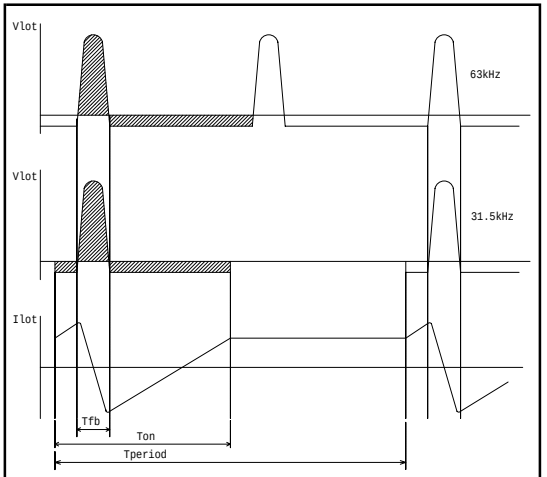


Fig. 10 Horizontal Scan Control Waveforms.

The average voltage across a coil must be equal to zero. With T-on = 100% the area under the flyback pulse must be equal to the scan amount. At half frequency, for equal EHT with fixed flyback time, half scan amount will be sufficient. This is indicated in Fig. 10. During T-off the current will flywheel in D73.

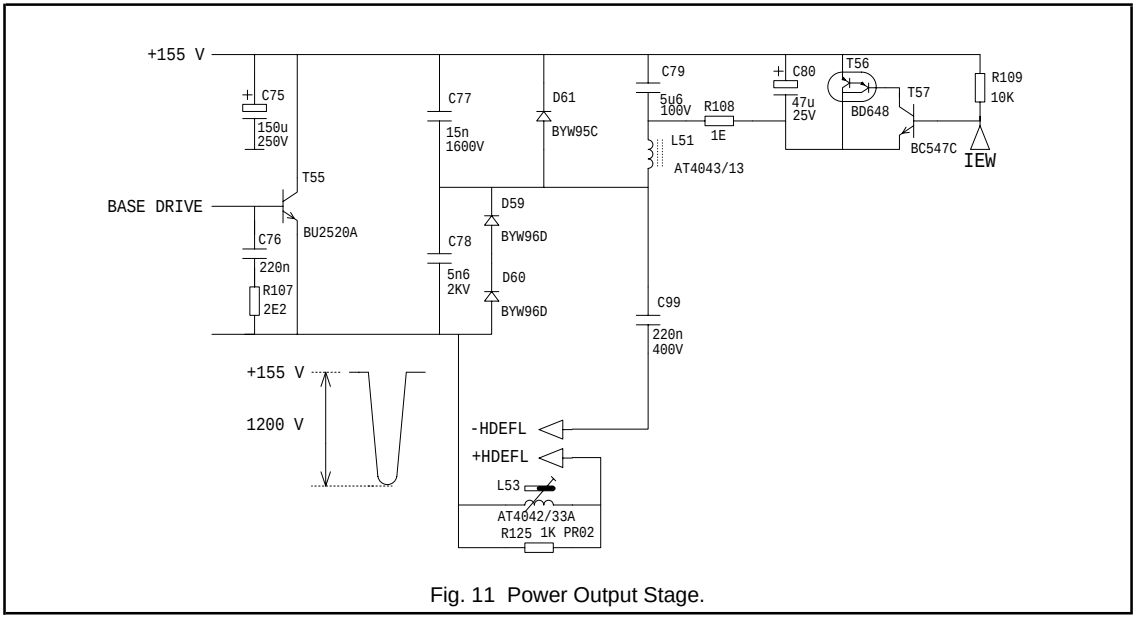


Fig. 11 Power Output Stage.

3.6.3 Power output stage

The power output stage, see Fig. 11, is a conventional one with a diode modulator.

Because this stage is connected to the supply rail, the flyback pulse has negative polarity. This makes the use of T54, see Fig. 2, necessary because the deflection controller IC52 expects a positive flyback pulse.

As lower damper diodes two low voltage diodes BYW96D in series are chosen because they switch faster than one single high voltage device.

As deflection transistor, the BU2520A is chosen. This device performs remarkably well over the frequency range of 30 to 64 kHz.

The value of flyback capacitor C78 depends on the impedance of the line deflection coils and the desired flyback time. With 180µH deflection coil impedance, C78 should be 5n6/2kV, with 220µH impedance, C78 should be 4n7/2kV.

3.6.4 East-west power stage

To drive the diode modulator, the drive current "IEW" must be converted to a voltage by means of R109. A power buffer T56/57, see Fig. 12, drives the diode modulator. To prevent high ac currents from flowing through T56, an additional filter R108/C80 is added.

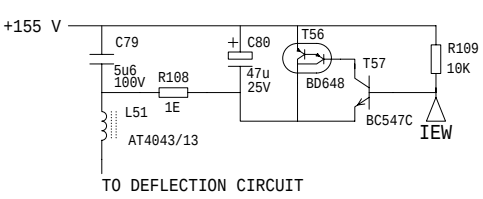


Fig. 12 EW Power Stage.

3.6.5 S-correction capacitor switches

The curvature of the screen determines the percentage S-correction. This percentage is constant and independent of frequency. Since the scan voltage is adapted according to the horizontal frequency, the S-correction voltage also has to be adapted, according to the frequency. The value of the S-correction capacitor is determined with the following equation:

$$C_s = T_p^2 / (8 \times \sigma \times L_h)$$

where:

T_p = the visible line period time;
σ = the percentage of S-correction;
L_h = the impedance of the deflection coil.

With a constant flyback time of 3µs, this gives the results as shown in Fig. 14. These values are realised in the circuit shown in Fig. 13.

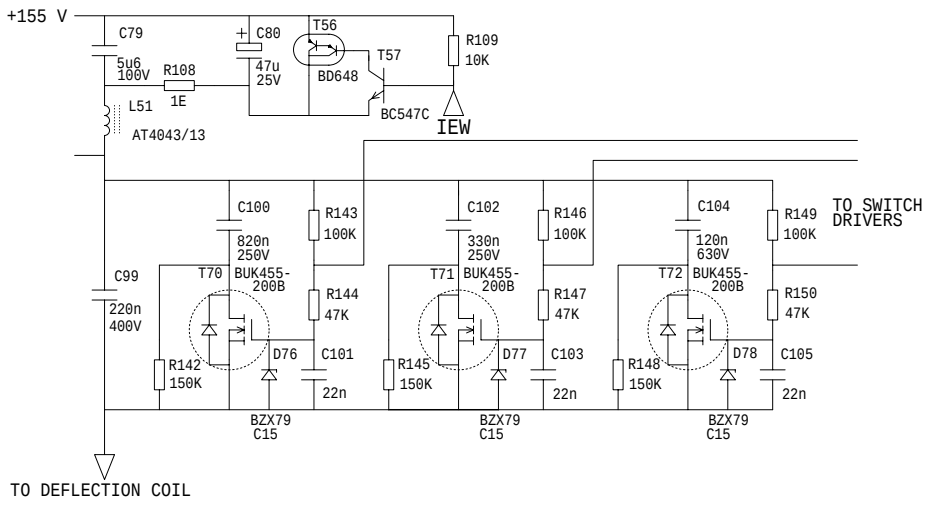


Fig. 13 S-correction Capacitor Switches.

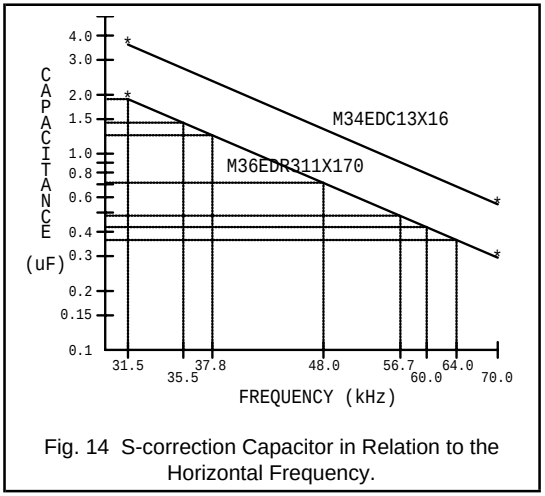


Fig. 14 S-correction Capacitor in Relation to the Horizontal Frequency.

Each switch contains a MOSFET with built-in anti parallel diode, see Fig. 14. When, for instance, T75, see Fig. 5, is not conducting, C101 will be charged via R143/144 and T70 will conduct. D76 prevents the gate from too high voltages. When T75 conducts, the voltage at C101 will be zero and T70 will block. Such a switch can also be build with a bipolar device, however that would require a higher drive current, resulting in high losses because of the ac and dc voltage difference between drive and switch.

The switch itself functions as follows. During the first part of scan the current is conducted by the MOSFET; the S-correction capacitor will be charged. During the second part of scan the current will be conducted by the anti parallel diode. In case the MOSFET is not conducting, the S-correction capacitor will not be charged during first part of scan, except from a very small current through the resistors parallel to the MOSFET switches. So, during the second part of the scan the V_{DS} will remain positive and the anti-parallel diode will not conduct.

3.6.6 EHT, Focus and Vg2

The EHT, focus and Vg2 are generated by the Line Output Transformer (LOT) AT2090/01. This transformer can be used up to 85 kHz and has a built-in bleeder (with focus and Vg2 potentiometers) and an EHT smoothing capacitor of 3nF. Not only the flyback but also the scan voltages are frequency independent. So, auxiliary voltages can be extracted from the LOT in the ordinary way. There is one exception: often the heater voltage for the CRT is taken from an unrectified winding of the line output transformer. Since due to T-on the RMS value is not frequency independent, the CRT heater must be supplied from a rectified winding. For practical reasons in this design an SMPS voltage was more suited (-10.5V).

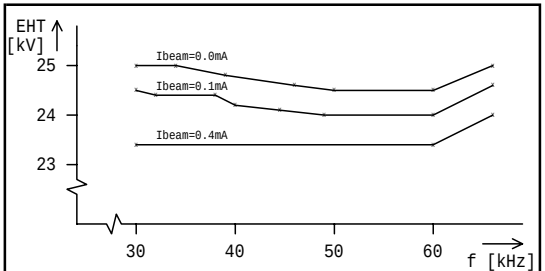


Fig. 15 EHT vs. Frequency.

3.7 Vertical deflection

The vertical deflection output stage used in this design is the TDA4861 (IC51), see Fig.16. This vertical output stage can be considered as a power operational amplifier with an extra flyback generator and guard circuit.

The inputs are driven by the balanced outputs of the TDA4851. The TDA4851 supplies complementary drive currents, which can be directly connected to the input pins of the output stage.

To determine the values of resistors R71/75, conventional operational amplifier theory is applicable. This theory says that, in practical cases, the differential input voltage of an operational amplifier always equals zero:

$$V_2 = V_3$$

$$I_{out} \times R_{72} - I_{drive} \times R_{71} = I_{drive} \times R_{75}$$

For simplicity of design, R71 and R75 have the same value Ri:

$$R_i = I_{out} \times R_{72} / (2 \times I_{drive})$$

The peak output current is the peak current for the deflection coil used in the design (here peak Iout = 0.75A), Idrive is the drive current from the TDA4851: 250µA. The value of resistor R72 can be chosen freely within certain limits:

1. The power dissipation in the resistor may not exceed the power rating of the resistor used;
2. The voltage drop across R72 is subtracted from the total available peak to peak coil drive voltage;
3. The minimum resistance is limited by the ground plane, which introduces a tolerance that has to be minimised with respect to the resistor value.

A good choice for R72 is 1Ω, the lowest available resistor value in the normal range. This leads to the following result:

$$R_i = 0.75 \times 1 / (2 \times 250 \times 10^{-6})$$

$$R_i = 1500\ \Omega$$

Amplitude control is realised by adjustment of the output of the TDA4851.

Vertical shift, a user control, is possible by P52. Injecting a dc current in one of the summation points, results in a dc current through the deflection coil. The 0 to +12V from the potmeter P52 is translated into a dc current in R71 by means of resistors R73/74. Design considerations for these two resistors are: a potmeter in middle position (the dc current in the coil should be zero) and the maximum shift range.

The resistors values in the circuit diagram allow a shift range of ±15 mm.

The output of the TDA4861 is DC coupled with the deflection coil, resulting in a bounce-free behaviour. Together with the fast response of the TDA4851 after a frequency change, this combination offers a stable picture within two frames.

For stability reasons, the combination R70/C56 is added between the output and the most negative supply voltage. If no damping resistor is present on the deflection coil, R69 should be added. Its value has to be determined experimentally.

The supply voltages for the TDA4861 are ± 10.5V, allowing simple dc coupling of the deflection coil. For flyback, an extra supply voltage of +30V is connected to pin 8. This results in a fast flyback of 300µs.

The vertical guard pulse, available on pin 9, is connected to the Vg1 circuit to provide vertical blanking and protection in case no deflection coil is connected.

Diode D52 protects the TDA4861 in case the flyback voltage is missing or drops faster than the +10.5V at switching off of the circuit.

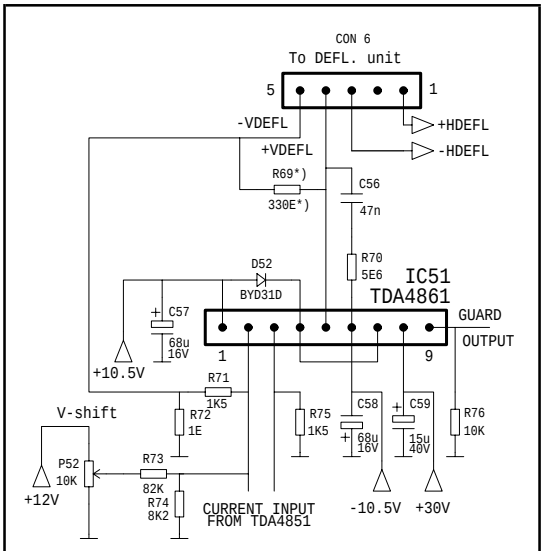


Fig. 16 Vertical Deflection Output Stage.

3.8 Miscellaneous II

3.8.1 EHT compensation

With the aid of the built-in EHT capacitor and focus / Vg2 divider in the LOT, the EHT voltage can be monitored in a very easy way. When the time constant of these built-in components is equal to the time constant of (R128+P57)/C92, then at LOT pin 12 an exact (divided) copy of the EHT can be found. This signal is buffered by T66 and inverted by T67, see Fig. 17.

Due to the tolerance on the Focus / Vg2 bleeder an adjustment is required (P57).

The EHT information signal goes to T68, the inverted signal modulates the picture width driver, in order to compensate the horizontal deflection for EHT variations. The non-inverted output of T68 is fed to the vertical amplitude control pin of the TDA4851 to compensate the vertical deflection for EHT variations.

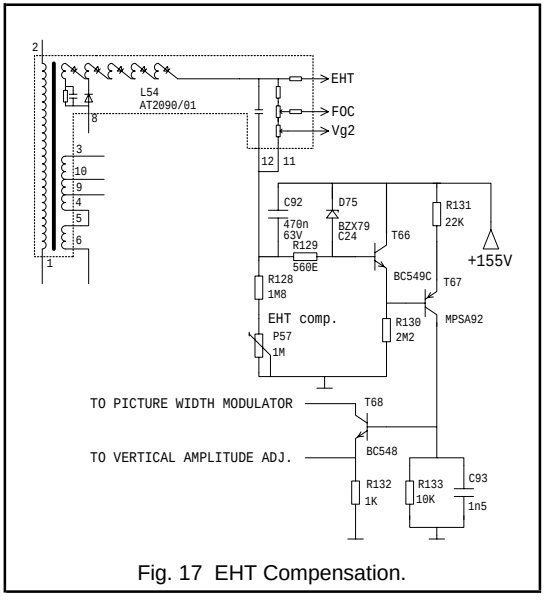


Fig. 17 EHT Compensation.

3.8.2 Beam current limiting

The long-term average anode current for the given tube is 700µA. This current is measured at the lower side of the EHT winding of the LOT, L54. The anode current flows through resistor R126, connected to the +12V rail. When the voltage across this resistor increases (with increasing anode current), the base voltage of T65 drops. With a high contrast setting, 6V dc on pin 9 of connector 2, the beam current limiter (BCL) will be activated at an average anode current of:

$$I_a = \{ +U_v - U_{contrast} + U_{be}(T65) + U(D74) \} / R126 - I_{bleeder}$$

$$I_a = \{ (12 - 6 + 0.65 + 0.5) / 15{,}000 \} - \{ 25{,}000 / (300 \times 10^6) \}$$

$$I_a = 394\ \mu A$$

3.8.3 Vg1 supply

This monitor is equipped with an ac coupled video output stage, using a supply voltage of 65V. After dc restoration, the highest black level is approximately 45V, with respect to ground. This implies that, with a tube requiring a cut-off of 125V, Vg1 must be -80V.

At C84 a negative flyback pulse is rectified (-130V). During normal operation T58 is saturated and Vg1 will be -80V. If T58 is not conducting, Vg1 will be -130V which will cut-off the tube completely. This will be the case in the following conditions:

vertical guard (failure in the vertical output stage;
absence of vertical supply (+10.5V); and
absence of horizontal deflection (e.g. power switch off).

Vertical guard. When the vertical output stage generates a vertical guard pulse, via D64 the base of T58 will become high, which will turn off this transistor. Vg1 will be -130V.

Absence of vertical supply. When there is no vertical supply, the vertical output stage can not generate a guard pulse either. Therefore, the Vg1 circuit is connected to the vertical supply rail. When the +10.5V supply is missing, T58 cannot conduct, resulting in Vg1 = -130V.

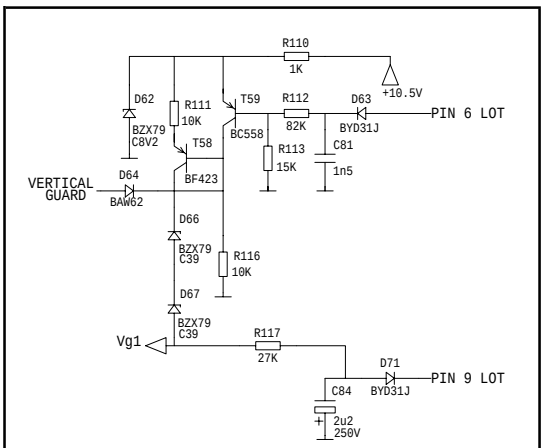


Fig. 18 Vg1 Supply.

Absence of horizontal deflection. When there is no horizontal deflection the line flyback pulse will be small or not present at all. This line flyback pulse is peak-peak rectified at C81 and thus keeping T59 blocked. When flyback pulses disappear, caused by a failure in the Line Output Stage or at switch-off, T59 will conduct, causing T58 to be blocked, and Vg1 will be -130V (C84 is large enough to hold Vg1 on -130 Volts until the EHT is discharged).

3.8.4 Blanking for TDA4881

Horizontal blanking pulses are derived from the line flyback pulses as delivered by the circuit around T54, see Fig. 2. The cathode of D51 is connected to the collector of T54. To limit the amplitude of the blanking pulses, D50 is added, see Fig. 19.

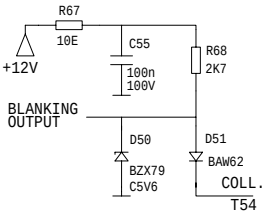


Fig. 19 Blanking Pulse Generator.

3.8.5 Video supply

The ac coupled video output amplifiers require a supply voltage of:

$$V_s = V_{swing} + V_{min} + (V_s - V_{max})$$

$$V_s = 50 + 10 + 5\ V$$

$$V_s = 65\ V$$

The secondary windings 3-4 and 5-6 of the LOT, L54, are connected in series and stacked on the +10.5V supply. The output voltage of rectifier diode D65 and capacitor C83 is 66V.

3.8.6 X-ray protection

A failure in the horizontal scan control section, could cause a dangerous situation: the EHT might rise to an unacceptable high level. The thyristor, consisting of T60/61, see Fig. 20, is fired when the flyback voltage rises to an unacceptable level. The flyback input pin 2 of the TDA4851 is forced high. This causes the horizontal drive output pin 3 of the TDA4851 to be turned off (output voltage is high). The line driver will be turned on, turning off the line output transistor. The T-on driver will not be triggered any more. The result is that the complete line output stage stops working, so that the EHT will drop automatically.

Blanking is achieved, through the normal blanking circuit. Furthermore, the Vg1 voltage will also drop, in order to cut-off the tube.

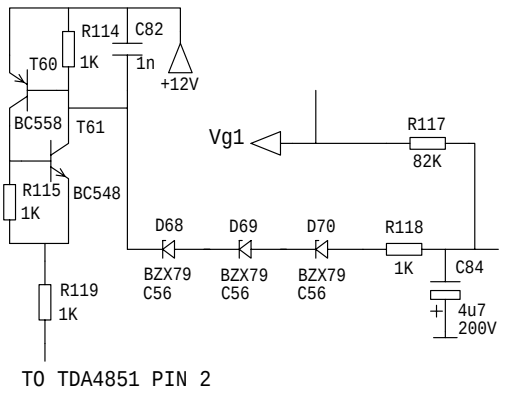


Fig. 20 X-ray Protection.

4. Oscillograms

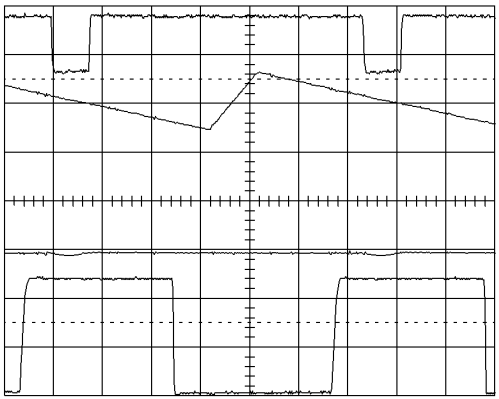
The oscillograms given are meant as a guide-line in debugging and aligning the circuit and together with the above text it can also be of help in understanding the circuit.

All oscillograms concerning the horizontal sync processing and deflection are given at two frequencies (31.5 & 56.7 kHz).

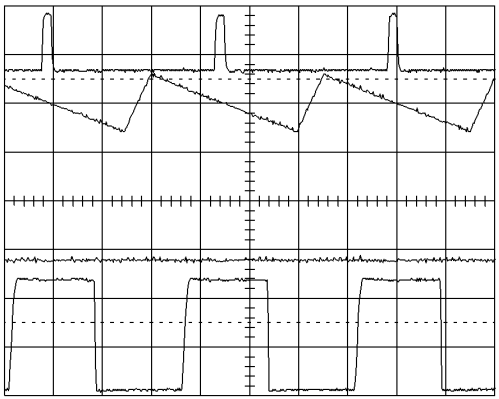
The relative position of the traces in the oscillograms with respect to ground is not given. It is assumed that the reader has enough knowledge of the circuits to understand them without this indication.

In all the following figures trace 1 is at the top leading to trace 4 at the bottom of each oscillogram.

31.5 kHz



56.7 kHz

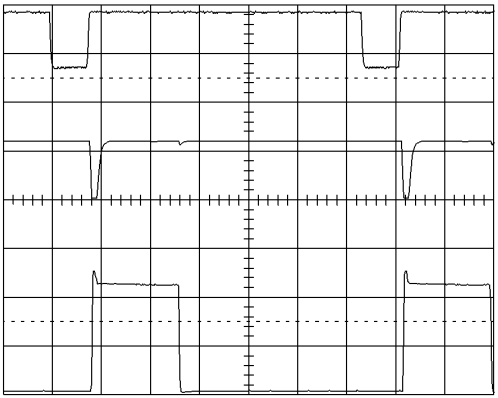


Figs. 21 & 22 Horizontal Oscillator

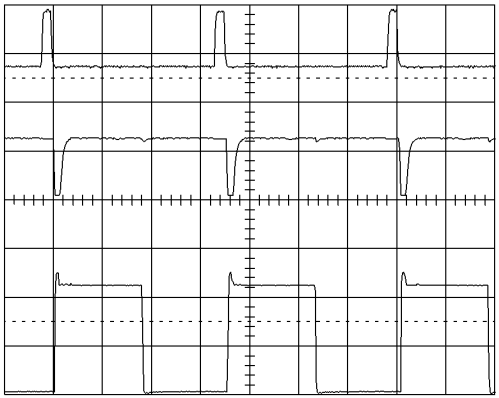
Trace 1: H-sync pulse at pin 9 of TDA4851 (2V/div).
Trace 2: Sawtooth voltage at pin 19 of TDA4851 (2V/div).
Trace 3: Φ1 voltage at pin 17 of TDA4851 (5V/div).
Trace 4: Drive voltage at pin 3 of TDA4851 (2V/div).
Horizontal: 5µs/div.

Remark: When the sensitivity of trace 3 is enlarged small triangles can be seen (100 - 150mV) pointing downwards. These triangles coincide with the horizontal sync pulse. So a wider sync pulse gives wider (and larger) triangles.

31.5 kHz



56.7 kHz

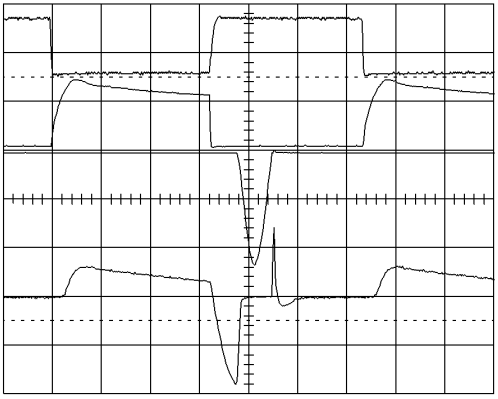


Figs. 23 & 24 Frequency to Voltage Converter

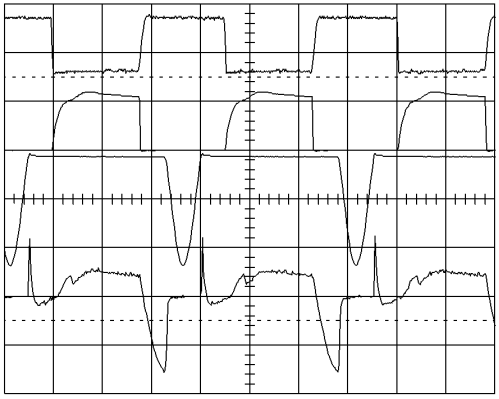
Trace 1: H-sync pulse at pin 9 of TDA4851 (2V/div).
Trace 2: Voltage at pin 2 of IC50 (5V/div).
Trace 3: Output voltage at pin 3 of IC50 (5V/div).
Horizontal: 5µs/div.

Remark: The output voltage of pin 3 is integrated and is used for driving the horizontal oscillator and S-correction switches.

31.5 kHz



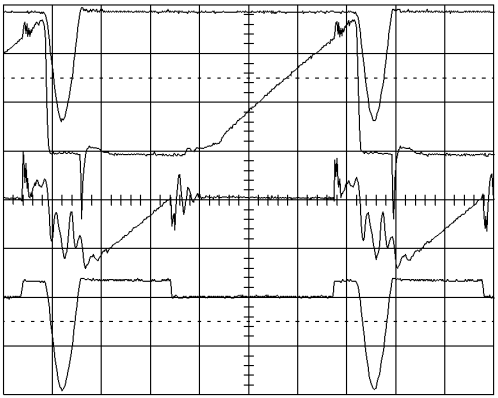
56.7 kHz



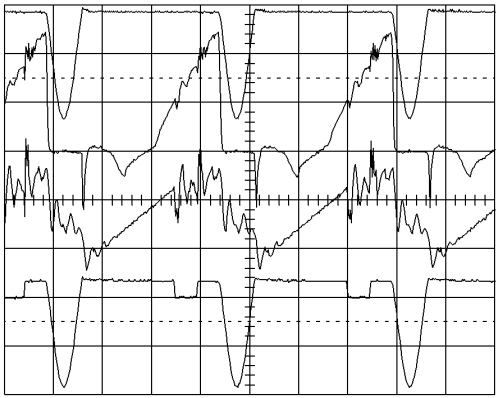
Figs. 25 & 26 Horizontal Driver

Trace 1: H drive pulse at pin 3 of TDA4851 (5V/div).
Trace 2: Drain voltage at the driver MOSFET BSN274 (200V/div).
Trace 3: Emitter voltage of the deflection transistor (500V/div).
Trace 4: Current in the base of the deflection transistor (2A/div).
Horizontal: 5µs/div.

31.5 kHz



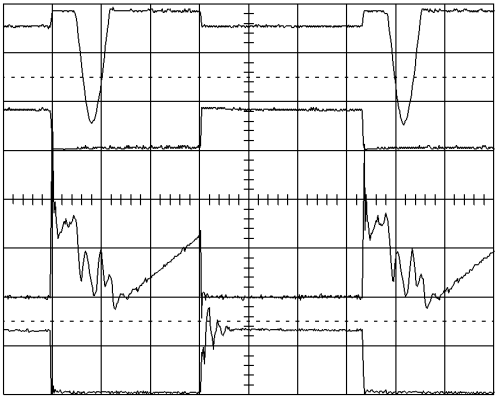
56.7 kHz



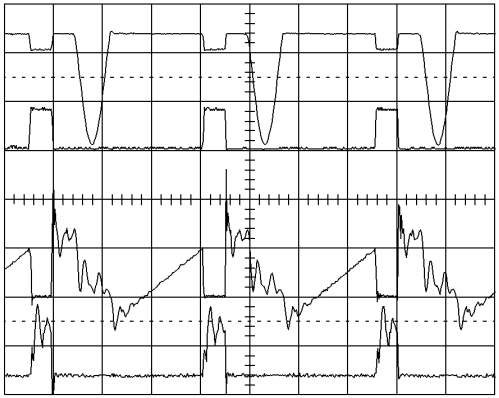
Figs. 27 & 28 LOT & Deflection Transistor

Trace 1: Emitter voltage of the deflection transistor (500V/div).
Trace 2: Collector current of the deflection transistor (2A/div).
Trace 3: Primary current in the LOT (0.5A/div).
Trace 4: Primary voltage of the LOT (500V/div).
Horizontal: 5µs/div.
Remark: The switching of T64 causes ringing in the LOT. This ringing is suppressed by the damping network in series with the LOT (R124, C88, L52). Some small ringing remains and is visible in the oscillograms.

31.5 kHz



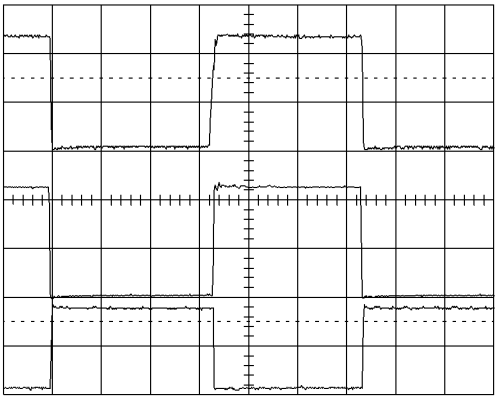
56.7 kHz



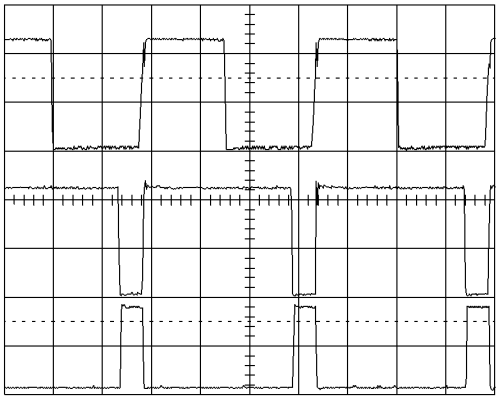
Figs. 29 & 30 T_{on} Switch

Trace 1: Primary voltage LOT (500V/div).
Trace 2: Drain voltage T-on switch T64 (200V/div).
Trace 3: Drain current T-on switch T64 (0.5A/div).
Trace 4: Current in D73 (0.5A/div).
Horizontal: 5µs/div.

31.5 kHz



56.7 kHz

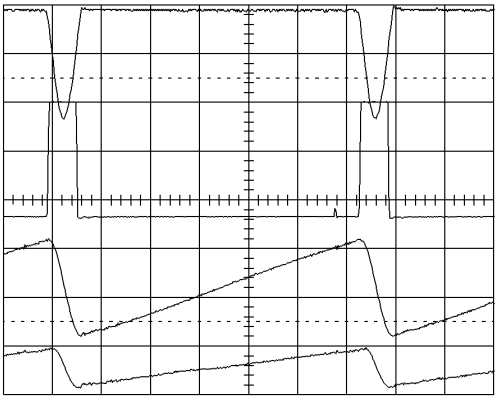


Figs. 31 & 32 Drive T_{on} Switch

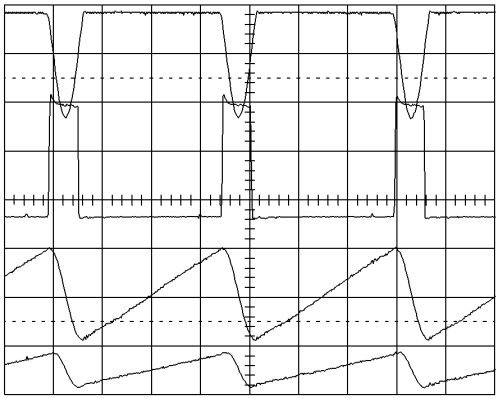
Trace 1: Pin 4 IC54 (5V/div).
Trace 2: Pin 6 IC54 (5V/div).
Trace 3: Drain T64 (100V/div).
Horizontal: 5µs/div.

Remark: At the negative edge of the drive pulse IC50 is triggered. The output will give a fixed T-on (high) output. To prevent this one shot working at half frequency ($f_{drive} > 1/T_{on}$), this one shot must be retriggerable.

31.5 kHz



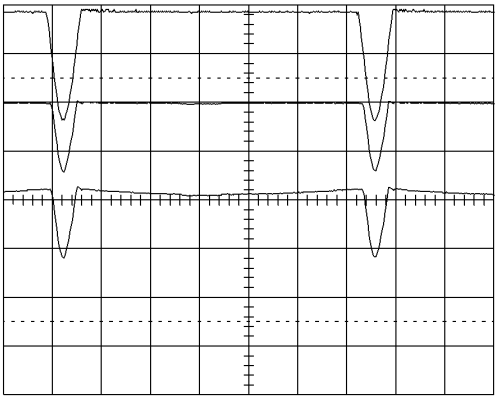
56.7 kHz



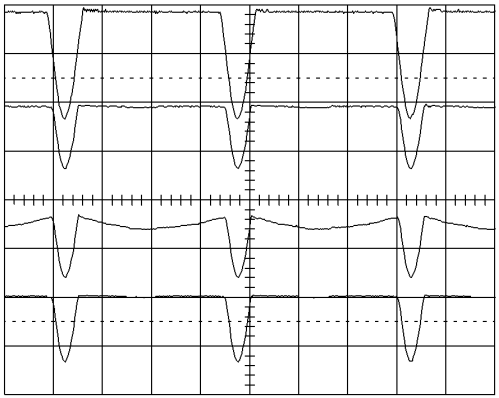
Figs. 33 & 34 Deflection Stage

Trace 1: Emitter voltage T55 (500V/div)/
Trace 2: Voltage at pin 2 TDA4851 (2V/div).
Trace 3: Deflection current (5A/div).
Trace 4: Current in bridge coil L51 (5A/div).
Horizontal: 5µs/div).

31.5 kHz



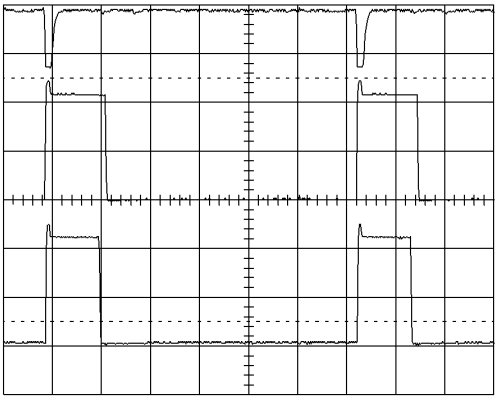
56.7 kHz



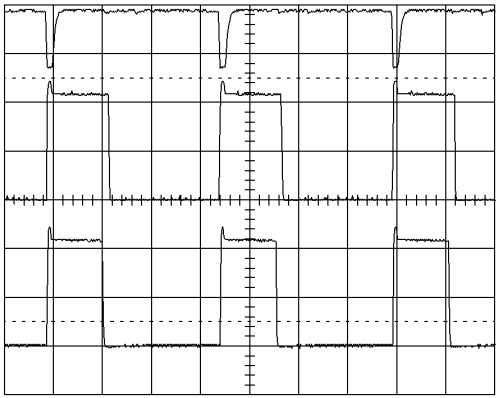
Figs. 35 & 36 S-correction switches

Trace 1: Emitter voltage T55 (500V/div).
Trace 2: Anode voltage D61 (100V/div).
Trace 3: Drain voltage S-correction switch T70/71/72 when on (100V/div).
Trace 4: Drain voltage S-correction switch T70/71/72 when off (100V/div).
Horizontal: 5µs/div.
Remark: At 31.5 kHz all S-correction switches are conducting so in Fig. 35 trace 4 is missing.

31.5 kHz

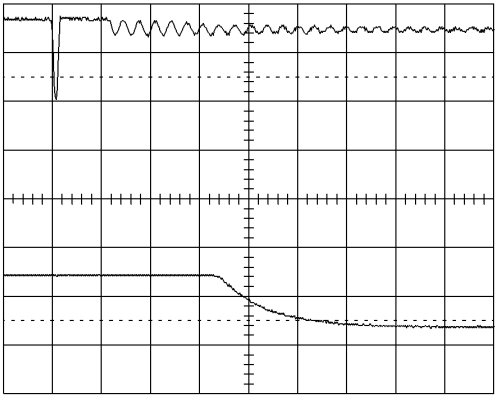


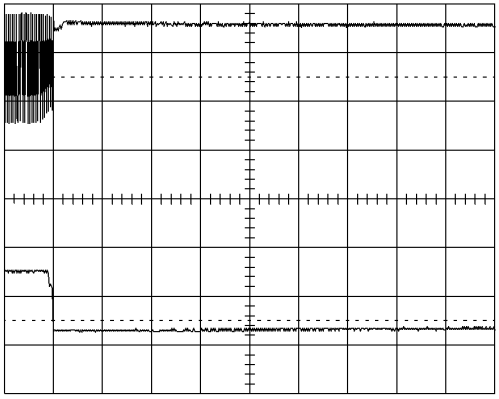
56.7 kHz



Figs. 37 & 38 EW One Shot

Trace 1: Voltage at pin 2 IC55 (5V/div).
Trace 2: Voltage at pin 6 IC55 with max. pulse width (5V/div).
Trace 3: Voltage at pin 6 IC55 with min. pulse width (5V/div).
Horizontal: 5µs/div.
Remark: Pin 5 of IC55 is modulated with the EW parabola, see Fig. 43. The output pulse width is thus EW modulated with the min/max pulse width given in traces 2 and 3.





Figs. 39 & 40 Vg1 Switch Off

Trace 1: Emitter voltage T55 (500V/div).
Trace 2: Vg1 (50V/div).
Horizontal left: 20µs/div.
Horizontal right: 1s/div.

Remark: The time constant of the picture tube and EHT capacitor/bleeder is about 1.6s, so Vg1 is still -130V as the picture tube is fully discharged. Vg1 will also blank the screen in case of vertical guard and failure of the +10.5V supply.

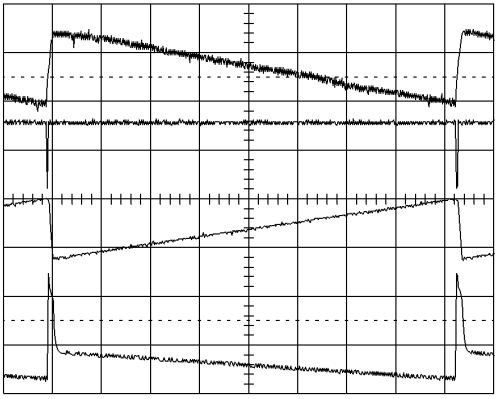
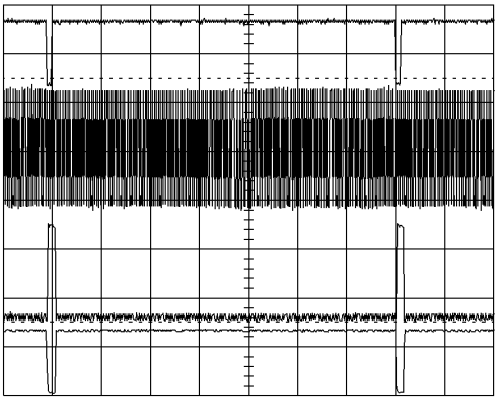


Fig. 41 Vertical Deflection

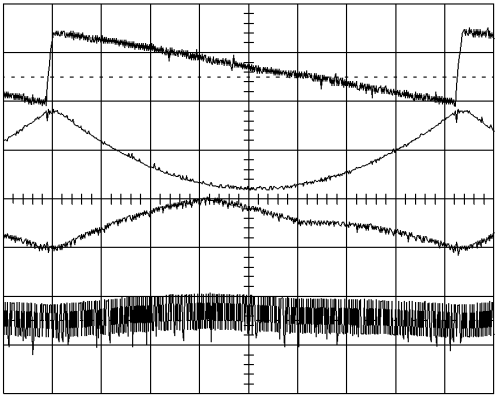
Trace 1: Vertical deflection current (1A/div).
Trace 2: Sync pulse at pin 10 TDA4851 (2V/div).
Trace 3: Vertical oscillator voltage pin 16 TDA4851 (2V/div).
Trace 4: Output voltage at pin 5 TDA4861 (20V/div).
Horizontal: 2ms/div.

Remark: During vertical sync pin 8 will be 2V (not visible in this oscillogram due to sampling effect of the DSO used).



Trace 1: Vertical sync pulse at pin 10 TDA4851 (2V/div).
Trace 2: Voltage at pin 8 TDA4851 (2V/div).
Trace 3: Guard voltage at pin 9 TDA4861 (5V/div).
Trace 4: Vg1 (50V/div).
Horizontal: 2ms/div.

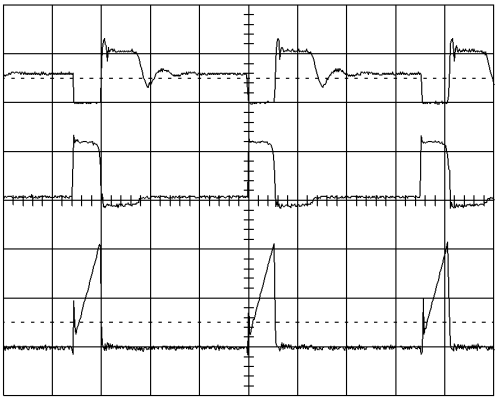
Fig. 42 Blanking and Guard



Trace 1: Vertical deflection current (1A/div).
Trace 2: EW output (pin 11) of TDA4851 (1V/div).
Trace 3: Pin 5 IC55 (1V/div).
Trace 4: Filtered voltage of pin 3 IC55 (0.5V/div).
Horizontal: 2ms/div.

Remark: In the middle of the picture tube a white bar with high intensity was displayed. At trace 3 the superimposed EHT compensation signal for picture width correction can be seen. At trace 4 some line ripple is visible, see Figs. 37&38.

Fig. 43 EW waveforms



Trace 1: V_{CE} of the SMPS transistor (500V/div).
Trace 2: V_{BE} of SMPS transistor (5V/div).
Trace 3: I_C of SMPS transistor (1A/div).
Horizontal: 10µs/div.

Fig. 44 Power supply

5. Component Placement

The following recommendations are given for the design of the PCB (see also reference).

1. Keep loop areas with high currents and sensitive loop areas as small as possible.
2. Keep tracks that carry high voltage components and sensitive tracks as short as possible.
3. Do not locate the asynchronous SMPS transformer close to the TDA4850.
4. Use a star ground without ground loops!
5. Implement local supply filtering for an IC. On the ground only peripheral components of this particular IC may be grounded.
6. Try to ground sensitive components as close as possible to the ground pin of its IC using a separate ground track; for example, components of oscillator, Φ1 and Φ2.
7. Especially critical in this circuit are the components around the TDA4851 (IC52), belonging to the horizontal part. Where possible, SMD types should be used. In all other cases, connecting tracks should be kept as short as possible.

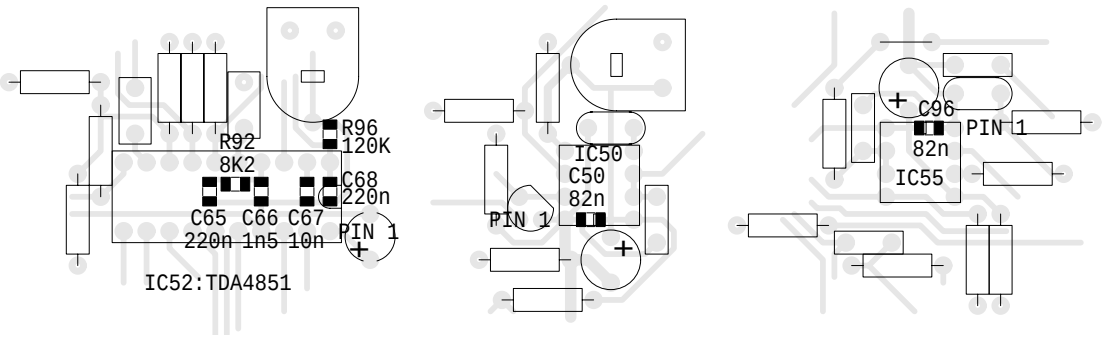


Fig. 45 Examples of SMD component placement

8. IC50 and IC55, both NE555 timers, should be fitted with an SMD supply bypass capacitor connected directly across the supply pins. The reason for this is, to keep the current transient at switch-over of the output as small as possible.
9. The pulses from the F/V converter, IC50 in Fig. 3, and the picture width driver, IC55 in Fig. 7, must not interfere with the sawtooth voltage of the horizontal oscillator, IC52 in Fig. 1.

Examples of good layout solutions with SMD components are shown in Fig. 45.

6. References

The information in this section has been extracted from the following report:

A Versatile 30 - 64 kHz Autosync Monitor

Author: H.Misdom / H.Verhees
Report no.: ETV92003
12NC:

For a complete understanding of this application leading to actual implementation of this design the above report should be consulted. Other essential reference sources are as follows:

Improvements on the 30 - 64 kHz Autosync Monitor

Author: H.Verhees
Report no.: ETV92008
12NC:

Full Mains Range 150W SMPS for TV and Monitors

Author: H.Simons
Report no.: ETV/AN92011
12NC.:

Advanced Monitor Deflection Controllers TDA4851 and TDA4852

Author: H.Verhees
Report no.: ETV93003
12NC:

Integrated SMPS Control Circuit TDA8380

Author:
Report no.:
12NC: 9398 358 40011

Specification of Bus Controlled Monitor

Author: J.Shy, T.H.Wu and J.Chiou
Report no.: Taiwan/AN9101
12NC:

Improvements on the 30 to 64 kHz Autosync Monitor

Author: H.Verhees
Report no.: ETV92008
12NC:

Electromagnetic Compatibility and PCB Constraints

Author: M.J.Coenen
Report no.: ESG89001
12NC: 9398 067 20011

Acknowledgments

We are grateful for all the contributions from our colleagues within Philips and to the Application Laboratories in Eindhoven and Hamburg.

We would also like to thank Dr.P.H.Mellor of the University of Sheffield for contributing the application note of section 3.1.5.

The authors thank Mrs.R.Hayes for her considerable help in the preparation of this book.

The authors also thank Mr.D.F.Haslam for his assistance in the formatting and printing of the manuscripts.

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Preface

This book was prepared by the Power Semiconductor Applications Laboratory of the Philips Semiconductors product division, Hazel Grove. The book is intended as a guide to using power semiconductors both efficiently and reliably in power conversion applications. It is made up of eight main chapters each of which contains a number of application notes aimed at making it easier to select and use power semiconductors.

CHAPTER 1 forms an introduction to power semiconductors concentrating particularly on the two major power transistor technologies, Power MOSFETs and High Voltage Bipolar Transistors.

CHAPTER 2 is devoted to Switched Mode Power Supplies. It begins with a basic description of the most commonly used topologies and discusses the major issues surrounding the use of power semiconductors including rectifiers. Specific design examples are given as well as a look at designing the magnetic components. The end of this chapter describes resonant power supply technology.

CHAPTER 3 describes motion control in terms of ac, dc and stepper motor operation and control. This chapter looks only at transistor controls, phase control using thyristors and triacs is discussed separately in chapter 6.

CHAPTER 4 looks at television and monitor applications. A description of the operation of horizontal deflection circuits is given followed by transistor selection guides for both deflection and power supply applications. Deflection and power supply circuit examples are also given based on circuits designed by the Product Concept and Application Laboratories (Eindhoven).

CHAPTER 5 concentrates on automotive electronics looking in detail at the requirements for the electronic switches taking into consideration the harsh environment in which they must operate.

CHAPTER 6 reviews thyristor and triac applications from the basics of device technology and operation to the simple design rules which should be followed to achieve maximum reliability. Specific examples are given in this chapter for a number of the common applications.

CHAPTER 7 looks at the thermal considerations for power semiconductors in terms of power dissipation and junction temperature limits. Part of this chapter is devoted to worked examples showing how junction temperatures can be calculated to ensure the limits are not exceeded. Heatsink requirements and designs are also discussed in the second half of this chapter.

CHAPTER 8 is an introduction to the use of high voltage bipolar transistors in electronic lighting ballasts. Many of the possible topologies are described.

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