Chapter V
Transceiver Design

In this chapter we will explain the available transceiver architectures and will discus their specification, to find the best architecture to be used in wireless sensor network (WSN). WSNs are inherently low-power network with short range communication capability. Most of WSNs are very dense networks and hence low cost of its nodes is an important requirement. RF transceivers are the most power consuming and high cost part of a sensor node in WSNS. Consequently its low power and low cost requirements, demands new design strategies. Prior to define a design strategy it is necessary to define some parts of the networks communication protocol. Communication protocol and the radio link specifications insert limitations or offers freedoms on the transceiver characteristics. The most important characteristics of a receiver are:

- Dynamic range
- Sensitivity
- Linearity
- Noise figure
- Phase noise
- Working frequency and band width
- Channel selectivity
- Power consumption
- Spurious frequencies effect
- Leakage effects
- Image band rejection

Definition of dynamic range depends on the specific application. This parameter is generally a function of the transceiver parameters and the system requirement, like BER[1], VER[2], of false alarm rate, in detection systems. Dynamic range, linearity and phase noise are not so important in low performance transceivers, like the ones is required in WSN applications. The important specifications of a transmitter are as follows:

- Power efficiency
- Power control capability
- Transmitted signal power
- Working frequency and band width
- Out-of-band emission (ACI[3], ACPR[4])
- Inter Modulation products (IMP)

Transceiver requirements force the designer toward specific class of transceiver. Then the transceiver architecture and its configuration is selected or designed based on the specific application and the designer's experience. Among various specifications of the radio link, modulation scheme greatly influence the transceiver architecture. Simple modulations make possible to use very simple transceiver architectures, in expense of lower data rate, lower signal quality and lower spectral efficiency. After selecting the transceiver architecture and configuration, the required circuits and sub-blocks will be presented and finally the performance of the transceiver will be analyzed and optimized.

[1] Bit Error Rate
[2] Vector Error rate
[3] Adjacent Channel Interference
[4] Adjacent Channel Power Ratio

V.1 Transceiver Review

Three architectures are classically used for transceivers in a radio link: Heterodyne, Low-IF and Zero-IF or Direct Conversion (DCR[1] and DCT[2]). Each of these architectures has some advantages and some drawbacks, and hence designer chooses the proper architecture depending on the requirements of the application. Another transceiver technology, developed for short range low power UWB applications is UWB impulse radio. In this technology very short, un-modulated pulses are directly transmitted from antenna [1], [2], [3]. This architecture is not suitable for simple narrow-band transceivers. LNA-less receiver is another very simple architecture that may be used in wireless sensors networks as wakeup receiver [4], [5].

V.1.1 Heterodyne Architecture

Heterodyne architecture has been used in more than 98% of radio frequency applications until 1995 [6]. Block diagram of heterodyne receiver has been shown in Fig. V-1. Image-reject filter is placed after LNA and attenuates the image signal in the mixer input. Image signal has at f_{IF} distance from the local oscillator frequency, in counter side of the massage signal. To day this architecture is widely used in optical and electro-optical systems [7], astronomy and space science [8],high frequency imaging [9], and accurate and standard frequency measurement and spectral analysis [10], [11], medical analysis [12], and in mm-wave wireless communications [13], [14], [15]. This architecture has been noticed in modern CMOS technologies for WSN applications [16].

The image signal problem is the bottleneck of heterodyne receiver, in sense of fully integrated design [17], [18]. Special techniques have been proposed this problem [19]. Image signal will be described in the next section. In general the image signal power can be even very higher than the massage signal [20]. So image rejection is the most problem of heterodyne receiver in radio communication applications. Choosing higher IF frequency eases the image rejection, however the IF signal processing and adjacent channel rejection will be more difficult [21], [22]. In the next section, the low-IF receiver that is a solution to reject the image signal is described. New architecture has been proposed for heterodyne receiver in [23] and claimed that the new architecture has many advantages over direct-conversion receivers and relaxes the performance of the receiver building blocks and eases the overall system floor planning.

Heterodyne receiver can be designed as single or double IF stage. In classic heterodyne receiver channel selection is done by the RF local oscillator and hence the IF filter bandwidth is equal to the channel band width. In some other types the IF filter is wide and covers all the

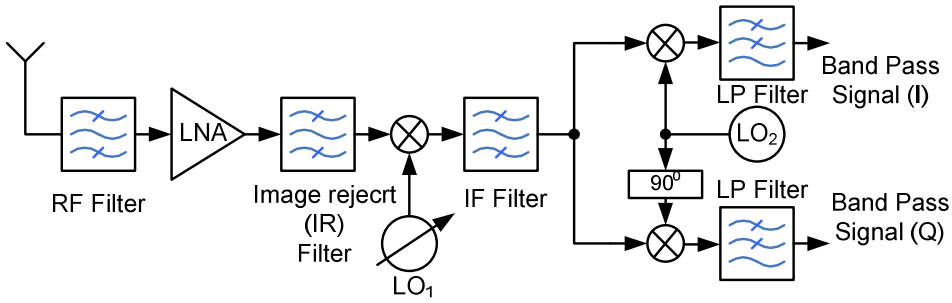


Fig. V-1. Basic block diagram of a heterodyne receiver

[1] Direct Conversion Receiver
[2] Direct Conversion Transmitter

receiver operation band and channel selection is done in IF band [24]. This configuration, named Wide IF heterodyne, has the benefit of more accurate channel selection, in expense of increased noise band width of the receiver. Main advantages of heterodyne receiver are [6]:

- High selectivity (good channel selecting in communication application and high spectral resolution in spectroscopy and spectral measurements [8])
- High sensitivity
- High dynamic range (AGC[1] easily be added to the IF amplifier)
- Less sensitive to DC offset of the mixer, spurious frequencies, high frequency leakages and even-order inter-modulation terms
- Less sensitivity to flicker noise

Main drawbacks of heterodyne architectures are [17], [25], [22]:

- Image reject filter problem in fully integrated design. In many applications, this filter should be implemented using SAW filters or other technologies that can not be integrated in bulk CMOS technology.
- Inherently complicated (needs two VCO and some mixers)
- High DC power consumption
- IF filter problem in fully integrated design
- The LNA must drive 50Ω load (the off-chip image reject filter) and this adds to the power dissipation, gain and noise problems.

V.1.2 Low-IF Architecture

To benefit the advantages of the heterodyne receiver, meanwhile making it suitable for fully integrated receiver and System-on-Chip integration, low-IF receiver architectures were developed [25], [17]. In these receivers the image signal is suppressed using complex signal processing and without need for sharp passive filters, as in heterodyne receivers. This architecture is widely used in recent communication and wireless applications [26], [27] ,[28].

The low-IF receiver rejects the image signals, like an Image-Reject Mixer (IRM), that its idea is based on the SSB[2] signal transmission theory, developed by Hartley in 1928 [29], and Weaver in 1956 [30]. Actually rejection of the image signal is due to the fact that the desire signal and the image signal appear in the IF band with different phase, as depicted in Fig. V-2 [31].

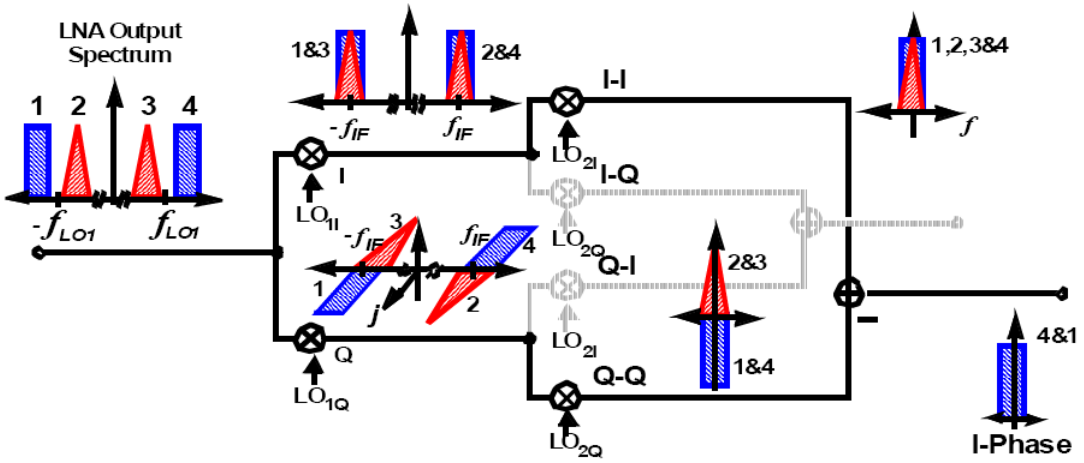


Fig. V-2. Representation of image rejection in a low-IF architecture, in frequency domain [31].

[1] Automatic gain Control
[2] Single Side Band Transmitters

This receiver is implemented in two approaches [6], [19]. One is based on the Weaver method and the other is based on the Hartley method. The former also is known as phasing method. Two different implementation of low IF receiver architectures based on the Hartley method, have been shown in Fig. V-3 [32], [33]. Both of these use 90^0 phase shifter in the signal path, that introduces the limitation in the signal bandwidth, since the phase shifter is inherently narrow band. Weaver architecture has been shown in Fig. V-4 [25]. This architecture replaces the phase shifters in the signal path, with the phase shifters in the local oscillator path and consequently does not suffers from the signal bandwidth. Analysis of this architecture has been presented in [17]. Weaver architecture is suitable for digital implementation and has been widely used in recent years in CMOS technology [26], [27], [28].Mathematical interpretation of image rejection process in Weaver architecture has been given in Appendix E.

Poly-phase filters [34], are widely used in low-IF receivers to improve the performance of low-IF receiver [17], [35]. Image reject performance of low-IF receiver is highly degraded in presence of the phase and gain imbalance in the mixer branches [6], [25]. In early CMOS technologies the typical phase mismatch of 3^0 was restricted the image rejection to 26 dB , but using special techniques 46 dB image rejection was possible [25]. In more recent technologies 35 dB image rejection is achievable with the standard low-IF architectures, for below 10 GHz [19]. Some adaptive techniques have been used to improve the signal path mismatch in a low-IF receiver [36], [37]. However these techniques are complicated and not suitable for low power applications, like WSN. A simple way to improve the image rejection of a low-IF receiver is using selective LNA. Using this method, in [38] 57dB image rejection at 2GHz has been reported and in [18] additional 12dB improvement has been achieved.

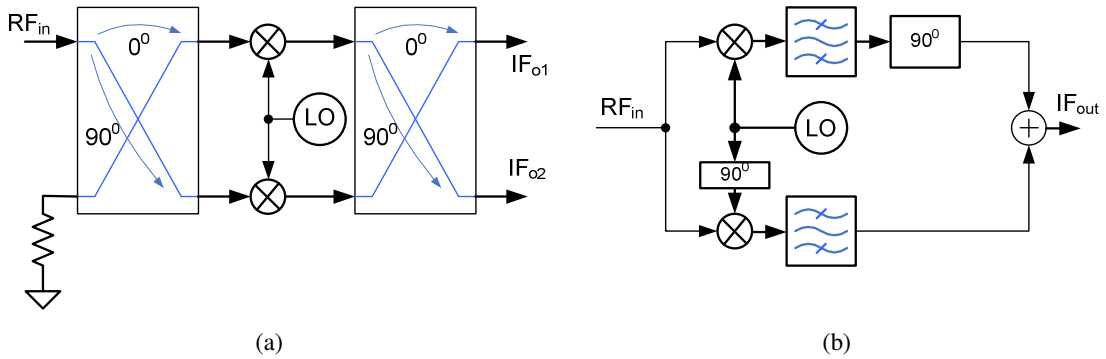


Fig. V-3. Two different implementation of Hartley low IF receiver: a) two phase-shifters with simple LO and [33] b) one phase-shifter with quadrature mixer [32].

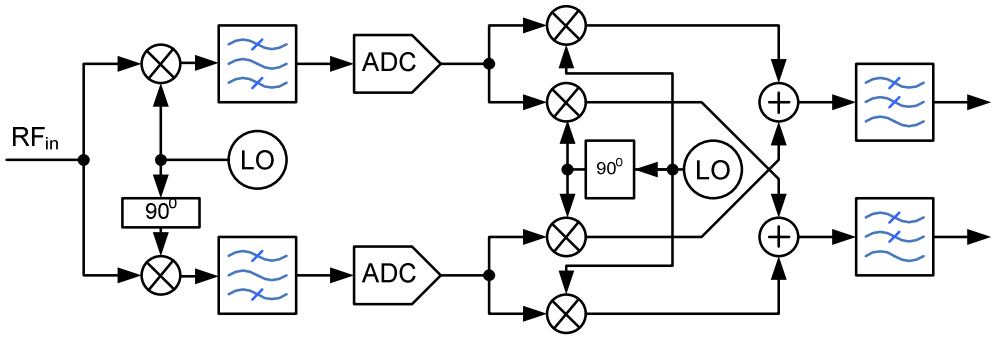


Fig. V-4. Architecture of Weaver low-IF receiver [25].

Weaver low-IF architecture is a good choice for WSN application, since it can be realized mainly in digital sections and hence yields a low-power receiver. Nevertheless, this is not the case for millimeter wave applications, in which high value of mismatch occurs between the I and Q signal passes. As an example, Razavi has reported 1.6dB/6.5^0 mismatch in 60GHz band for 90nm CMOS technology [13]. Using a simple analytic equation one can obtain an approximate value of image rejection [22]:

$$IRR = -10\log\left(\frac{1-2(1+\delta A)\cos\theta+(1+\delta A)^2}{1+2(1+\delta A)\cos\theta+(1+\delta A)^2}\right) \quad \text{(V-1)}$$

In which ΔA and θ are the gain and phase imbalance for two signal paths. Inserting the above values in this equation we obtain 19.3dB image rejection that is very low for practical applications. On the other hand in mm-wave band some other crucial problems arise that corrupts the advantages of the low-IF architecture [13].

V.1.3 Direct Conversion Architecture

Direct conversion receiver architecture (also recognized as zero-IF or Homodyne architecture) was considered as early as 1924, but as a crude receivers requiring only. In 1947 homodyne receiver was used in full effect for carrier based telephony [39]. However superior performance of heterodyne receivers pushed it out in the radio communication systems. Emerging the RF-CMOS and trends toward fully integrated transceiver, the zero-IF architecture was considered again. The first application of zero-IF technique in digital receivers was in 1980, in the FM paging receivers, firstly in ITT Standard Telecommunication Laboratories, and then in NEC and Philips paging receivers [39], [6]. In recent years many researches have been turned to the direct conversion transceivers [40], [41], [42].

The architecture of zero-IF receiver and transmitter has been shown in Fig. V-5. In the receiver, the RF signal amplified by a LNA then applied to a quadrature mixer. The local oscillator frequency is equal to the carrier frequency. Consequently the mixer translates the signal in the RF band, directly into the base-band. In the transmitter a band pass filter can be used before the power amplifier, to suppress the excess interference and noise in the transmitted signal [43]. If power control is required in a DCT, the power amplifier should handle variable output power.

The most important advantage of the direct conversion receiver is solving the image signal problem, and hence the image reject filter [22]. On the other hand, in direct conversion receivers, the channel filtering takes place at base band, this has an advantage with respect to both integration as well as potential use in multi-standard and SDR[1] applications [44]. With the desired channel modulated to base band, this enables the implementation of integrated, high-Q filter architectures capable of providing sufficient rejection of alternate channel energy before being digitized. Because the carrier is directly modulated to base band, there exists the possibility of integrating programmable base band signal processing either in the form of programmable filters or high-dynamic range ADCs followed by programmable digital channel filters to address variable bandwidth and frequency response requirements associated with different standards. In comparison with low-IF transceiver, base band signal in a direct conversion transceiver has less band width than low-IF architecture. Consequently the filtering in direct conversion architecture is less power consuming and ADC conversion can be done with half rate of low-IF architecture and hence with lower DC power consumption [45].

[1] Software Defined Radio

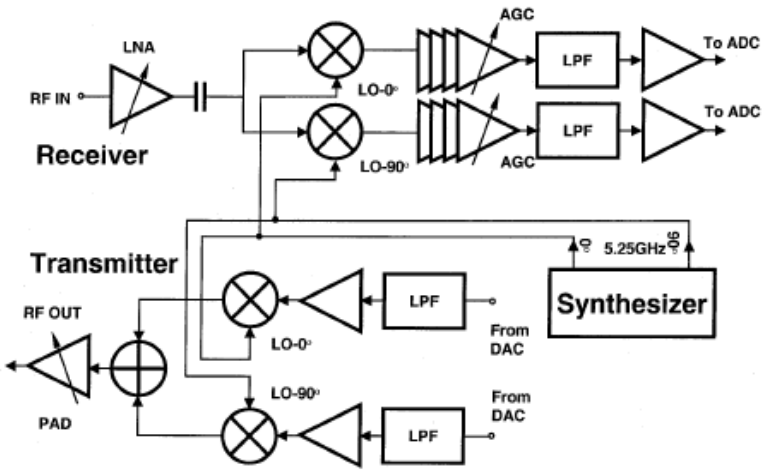


Fig. V-5. Architecture of direct conversion transceiver [45].

V.1.3.1 Problems with Direct Converter Receivers

The most important problem is the DC offset. The DC offset may have static or dynamic nature [46], [47], [48], [6], [22]. There are three main sources for dynamic DC offset:

First is the unsuppressed carrier in the received signal that is directly converted to the DC signal in the mixer output. Carrier signal in the received signal is due to the weak SSB forming and/or receiver back emission. The receiver back emission is due to the LO signal leakage to the receiver antenna and propagation to other receivers. This effect is more crucial in direct conversion receivers, because LO frequency is exactly at the center of the LNA and antenna band [49]. On the other hand the LO leakage into the power amplifier in SSB transmitter causes the weak carrier suppression. This problem may be reduced using heterodyne transmitters [50], however in heterodyne system the noise in the transmitted signal due to the phase noise of LO, that is added to the transmitted signal (known as *reciprocal mixing*), is more than the direct conversion transmitter, in which only one LO is used.

The second contributor to the dynamic DC offset is the various leakage signals, inside the receiver, as well as the unwanted RF signals input from antenna [6]. Fig. V-6 shows the various leakage signals. Self mixing of LO signal and the input signal with their leakages can be reduced with proper placing of mixer and LNA in the receiver layout.

The third contribution is the second order nonlinearity that leads to the detection of amplitude variations of the received signal [51], [49], [42]. If the received signal is strong desired signal, this effect increases the BER and hence degrades the dynamic range. If the strong received signal is not the desired signal (Interferer signal), then this effect degrades the receiver sensitivity. An efficient way to overcome this problem is using balanced circuits in the RF front-end.

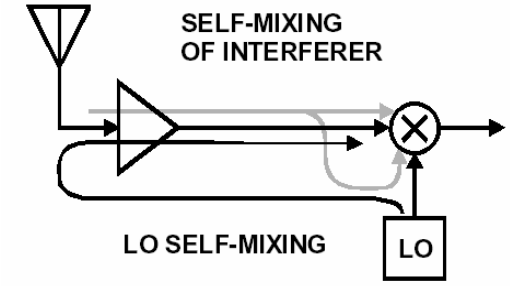


Fig. V-6. Self mixing of LO signal and the input signal with their leakages in a direct conversion receiver [6]

Static DC offset is mainly due to the transistor mismatch in the base band parts, after the mixer. Since the base band amplifiers in the direct conversion receiver have very high gain, even very small mismatch leads to a noticeable DC offset in the signal at the input of detector. In frequency domain, this offset appears in the middle of the down-converted signal spectrum and may be larger than the signal and much larger than the thermal and flicker noise. In the time domain the DC offset shifts the signal constellation and increases the bit error rate.

Most efficient way to reduce the DC offset is using the modulation schemes by which the modulated signal has very low energy in the frequency band around DC. By this way one can simply reject the DC offset by a notch filter in DC [52]. As an example, wide-band FSK[1] is not spectrally efficient, but it has been widely used in low data rate systems, like pagers [6]. FSK is a proper choice for wireless sensor networks, since it can be detected using very simple detectors [53], [54]. For many applications, e.g. digital cellular mobile communications, complicated spectrally-efficient modulations are needed. CDMA and WCDMA signals have very small energy in vicinity of DC, but for GMSK modulation, used in GSM mobile system, the spectra has its peak at DC [52]. Spectra of some modulations have been shown in Fig. V-7.

The other way to reduce the DC offset is using adaptive compensations [55], [56], [57]. In TDMA systems, the DC offset can be measured in unused time slots and then the results can be used for DC offset compensation. However this method is useful only in the case of static DC offset. Burst-to-burst DC offset estimation, special feed back techniques and DC offset estimation are some techniques used for DC offset cancellation [58], [59], [60], [61]. In term of circuit design, Even Harmonic Mixers (EHM) can be used to reduce the LO leakages [57], [62].

After solving the DC offset, the flicker noise problem arises. Again the easiest solution is using signal spectral shaping, so that the signal energy distributed in the frequency band out of the region in which the flicker noise is trouble. The other way is to use technologies with low *flicker noise corner*. For example, the flicker noise corner for CMOS is about 1 MHz and for Bipolar is about few kilo hertz [52], [63], [22]. Flicker noise reduction in a direct conversion receiver has been widely studied in recent years and mixers with flicker noise corner as low as few tens of kilo hertz have been reported [42], [64], [65]. One useful, but complicate technique to rune away the flicker noise is dynamic matching mixer, in which using two extra mixing (down-conversion and then up-conversion) the flicker noise spectral is separated from the signal spectra [66].

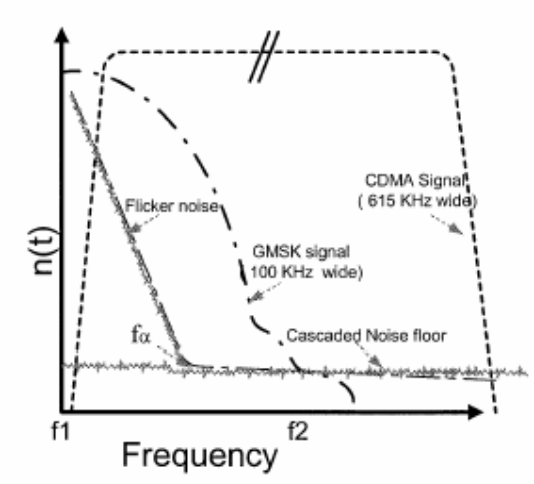


Fig. V-7. Power spectral density for GMSK and CDMA modulations [52].

[1] Frequency Shift Keying

Carrier adjustment and frequency dependent effects are other important problems in direct conversion receivers that can make the DC cancellation techniques ineffective. [67], [68], [6]. Even a small difference between the receiver LO and the received signal carrier frequencies can shift the signal spectra, so that the signal energy falls into the frequency bands in which DC offset or flicker noise is damaging. One solution is transmitting pseudo-random data in some unused or dedicated time slots and averaging the received signal to correct the receiver LO frequency [6].

V.1.3.2 Problems with Direct Converter Transmitters

The most crucial problem in a direct conversion transmitter is VCO pulling [45], [68]. The most effective technique to reduce the unwanted effects on VCO in a direct conversion transmitter, is using VCO in two-thirds of the LO frequency. Then the VCO output is applied to a divide by two circuit and finally the VCO output and the divider output are mixed to generate the desired LO signal [69]. However this technique produces unwanted terms in the output. In [45] another scheme has been proposed to obtain pure signal in the synthesizer output. These techniques have been depicted in Fig. V-8. In high performance transmitters, Low-IF technique is used to overcome this problem [68].

The second problem with direct conversion transmitter is generating quadrature LO signal. In spite of heterodyne architecture, in which quadrature LO signals are required in low frequency (in IF stage), the direct conversion receiver and transmitter needs the quadrature LO at RF frequency, in which the phase control is more complicated. Different techniques have been reported to generate the quadrature LO signal. Choosing the proper one is trade of between higher performance and lower power consumption [62], [70].

V.1.4 Transceiver Architecture for WSN

Requirements of WSN, i.e. very low power and moderate performance has been forced the WSN transceiver designers toward very simple transceiver structures. Fig. V-9 shows some the transceiver architectures developed for WSN applications. Simple receiver structure of Fig. V-9(a) detects the envelope of 916MHz RF signal without converting it to IF band [71]. In this figure the transmitter is simply composed of an oscillator whose output is connected to the power amplifier input via a on/off switch (direct modulation). The transceiver shown in Fig. V-9(b) is another simple transceiver that uses super regenerative sampling oscillator to directly sample the 1.9GHz RF signal. Both of the receivers in Fig. V-9 do not need to local oscillator. The transmitter in Fig. V-9(b) is a very low power BAW[1] resonator oscillator and a simple single stage power amplifier.

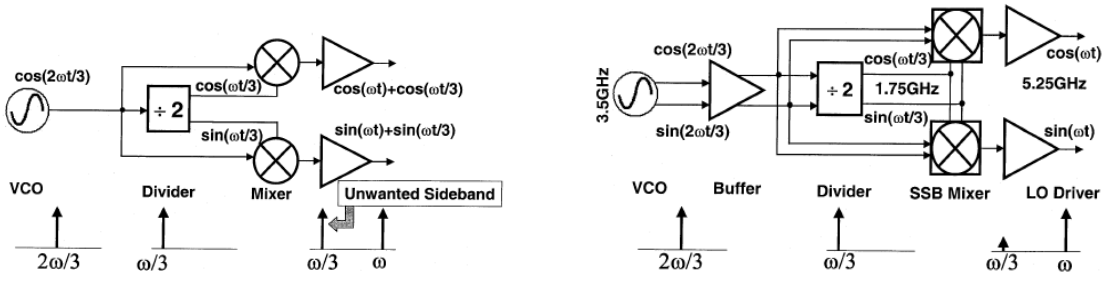


Fig. V-8. Frequency synthesize techniques to avoid VCO pulling in a direct conversion transceiver. The circuit in (a) produces unwanted harmonic in the output [69]. The circuit in (b) solves this problem in expense of more complexity [45].

[1] Bulk Acoustic Wave

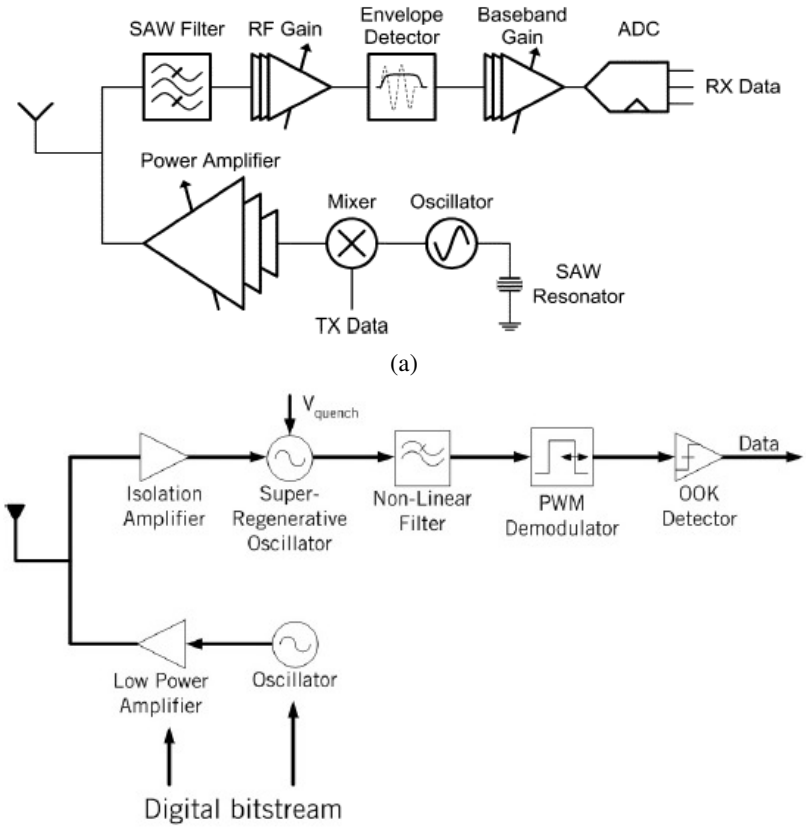


Fig. V-9. Simple transceiver structure developed for WSN applications, with direct detection of RF signal using (a) envelope detector [71] and (b) regenerative sampling [72]

Rabaey et *al*. have reported power oscillator based transmitter in which the oscillator is used instead of power amplifier. They have used an accurate 90uW FBAR[1] reference oscillator to luck the power oscillator by injection process (injection locked) [73]. Automatic Gain Control (AGC) is conventionally used in most of high performance receivers to increase the receiver's dynamic range. However AGC increases the complexity and power consumption and hence logarithmic amplifier or RF limiter is used as inherit AGC in low performance receivers. In [72] a logarithmic amplifier has been used and in [71] multi channel base band structure has been developed to increase the dynamic range, mean while keep the receivers performance, without any power budget. Many other techniques may be used to simplify the transceiver structure. Direct connection of LNA to antenna is a simple technique to simplify the receiver structure [74]. Envelope detectors have been used widely in WSN receivers, not only as amplitude detectors, but also as nonlinear low pass filter to discriminate the FSK signals [75]. To address the problems related to VCO in direct conversion transceivers, VCO in half of the local oscillator frequency has been used in [76]. This technique also reduces the VCO power consumption.

W.2 Transceiver Design in Our Work

Prior to design RF transceiver, some specifications and parameters of the WSN should be given. In our work, such data are not available and hence we will investigate the reported low power WSN transceivers to calculate some of the required parameters. A summary of

[1] Film (thin) Bulk Acoustic wave Resonator

reported WSN transmitters and receivers have been tabulated in Table V-1 and Table V-2, respectively.

V.2.1 Radio Link Design

Since the radio link has not been defined for our work, we should determine and design the items of radio like that are required in transceiver design.

A) Carrier and IF Frequency

Regarding the reported WSN transceivers in Table V-1 and V-2, all of the recently reported works have used carrier frequencies below 3GHz. However, higher carrier frequencies have the main advantages of higher immunity and antenna integration possibility. These advantages motivated us to try mm-wave band in our work. In recent years, mm-wave band has been considered as a candidate for low power short range high data rate

TABLE V-1
Summary of Reported WSN Transmitters

Reference	[73]	[72]	[75]	[77]	[78]	[71]	[79]
Year	2005	2006	2004	2004	2006	2007	2007
Technology	130nm CMOS	130nm CMOS	130nm CMOS	250nm CMOS	130nm CMOS	180nm CMOS	180nm CMOS
Frequency (GHz)	1.9	1.9	1.9	0.9	1.9	0.916	0.44
RF Power (dBm)*	-6	0	1.6	-6	0.8	-11.4 -2.2	0
DC Power (mW)**	1.8	1.6 1.8	3.6	1.3	1.35	3.8 9.1	2.58
Modulation	OOK	OOK	OOK BFSK	BFSK	OOK	OOK	OOK
Data Rate (kb/s)	5	50 156	40	20	330	1000	40000
Efficiency (%)	25	32 28	16.5	19	46	NA	NA

* Radiated power, when TX is on
** Average DC power, when TX is on

TABLE V-2
Summary of Reported WSN Receivers

Reference	[72]	[75]	[77]	[76]	[80]	[74]	[71]	[81]	[82]
Year	2005	2004	2004	2007	2007	2007	2007	2006	2005
Technology	130nm CMOS	130nm CMOS	250nm CMOS	180nm	130nm CMOS	130nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS
Receiver	Non-coherent	Non-coherent	Non-coherent	Non-coherent	Non-coherent	Non-coherent	Non-coherent	Non-coherent	Non-coherent
Frequency (GHz)	1.9	1.9	0.9	2.4	2.45	2.2	0.916	2.4	0.433
Sensitivity (dBm)	-100.5	-78	-94	-90	-90	-53	-37 -65	-90	-50
DC Power (mW)*	0.45	3.6	1.3	1	0.6	2	0.5 2.6	1	3.1
Modulation	OOK	OOK BFSK	BFSK	BFSK	BFSK	OOK	OOK	BFSK	OOK
Data Rate (kb/s)	5	40	20	100	NA	3000	1000	100	2000
BER	1e-3	NA	NA	1e-3	1e-3	NA	1e-3	1e-3	NA

*Average DC power, when RX is on

communications, such as WLAN[1] and WPAN[2] [83], [13], [84]. Higher carrier frequency allows small and antenna, but increases the DC power drastically [85].

Obviously increasing the carrier frequency increases the path loss and hence more transmitter power is required. Mathematically, the path loss can be calculated as [81], [86], [87]:

$$L_{path}(d) = 10\log\frac{(4\pi)^2 d^n}{\lambda^n} + L_{atten} \quad \text{(V-2)}$$

Where d is the distance of two nodes, λ is wave length and L_{atten} is the attenuation in the path. Although increased path loss forces the low power WSN designers toward lower carrier frequencies, the network reliability and interference and jamming immunity is an important motivation for higher carrier frequencies. Another important issue is the energy-per-bit value. Energy-per-bit is measure of comparing the energy efficiency of low power transceivers [71], [88], [89] and is calculated as:

$$E_b = T_b \times P_{DC} \quad \text{(V-3)}$$

Where P_{DC} is the average DC power and T_b is time duration of single bit. This equation implies that for a given DC power, increasing data rate decreases the energy-per-bit, and this means more energy efficient transceiver. As mentioned, wider IF band is possible if higher carrier frequency is used. Consequently, higher data rate is achievable and regarding (V-3), this means that energy efficient transceiver is achievable with higher carrier frequencies. However when data rate increased, the receiver bandwidth should be increased and regarding the receiver sensitivity equation [71]:

$$Sensitivity(dBm) = -174dBm/Hz + 10\log(Bandwidth) + SNR + NF \quad \text{(V-4)}$$

the receiver sensitivity is reduced. This directly translates to the higher transmitted power and consequently increasing DC power consumption. We have chosen the 30GHz carrier frequency in our design to evaluate mm-wave band ability in WSNs.

Selecting IF frequency is a compromise between the image reject capability in one side, and the IF stages power budget and the detector performance, in the other side. Better image signal rejection is achieved in higher IF and better detection and more low power and flexible IF stage is obtained in lower IF frequency. We found 2GHz frequency as a good compromise.

B) Transmitter Power

Regarding Table V-1, transmitter's radiated power is about few milliwatts in reported WSNs. This ensures that the transmitter power consumption be in order of power consumption of other circuits of WSN node. In our work the power consumption of receiver blocks is predicted to be about 10mW. Consequently assuming about 25% efficiency for the transmitter, we chose 5mW as the radiated power of transmitter. Regarding Table V-1, 25% efficiency in mm-wave seems difficult, but we have achieved it using power oscillator transmitter.

C) Modulation Scheme

To overcome the band-width limitations, traditional cellular and wireless local area network (WLAN) standards have grate emphasis on spectrally efficient modulation schemes, such as Gaussian Minimum-Shift Keying (GMSK) or Quadrature Amplitude Modulation (QAM). In addition, coherent receivers are mandatory to increase the channel capacity for a given bandwidth. However, these transceivers consume too much energy for sensor network applications. To address this problem, in 2003 the IEEE approved the 802.15.4 standard for

[1] Wireless Local Area Network
[2] Wireless Personal Area Network

low-power wireless personal area networks (WPANs). 802.15.4 supports both Binary Phase-Shift Keying (BPSK) and Offset Quadrature Phase-Sshift Keying (O-QPSK) modulation at a maximum data rate of 250 kb/s. Current 802.15.4 transceivers consume tens of milliwatts and have approximate energy per bit values of 100 nJ/bit, which is less than cellular systems but still too high for sensor network applications [71], [71].

To achieve very low energy-per-bit, very simple modulations, in conjunction with non-coherent receiver structure have been used in WSNs (See Table V-2). In a non-coherent receiver, in contrast with coherent receiver architecture, no oscillator is required for phase synchronization and the receiver can turn on quickly. Furthermore, when received power levels are large, the power consumption can be dramatically decreased as little RF gain is required and no RF oscillation must be sustained.

Two modulation schemes, i.e. On-Off Keying (OOK) and Binary Frequency Shift Keying (BFSK) have been widely used in WSN applications (See Table V-1 and V-2). Fig. V-10 shows simple implementation of these modulations. Both of these modulations are constant-envelop and hence non-linear power amplifiers can be used. Actually theses modulations are not band-width efficient, but are energy efficient [74]. In comparison with OOK, FSK needs more complicated transceiver. FSK needs complicated VCO and in some cases two VCO is used [73], [90]. Detection of FSK is more complicated than OOK. OOK receiver enables the use of an envelope detection based receiver [71]. In [75] receiver has two branches and can operate as FSK or two OOK branch and noted that OOK is more preferable for dense WSN. In [87] PPM[1] and OOK have been compared and using analysis of battery life time, it has been deduced that for dense WSN OOK modulation is more energy efficient, but for spars WSN PPM is better choice. UWB[2] signaling was defined by FCC[3] in Feb. 2002, is a good candidate for low-power short range communications and has some advantages in WSN applications [91], [1]. However this technique needs complicated transceiver structure. We have chosen OOK in our design and will analyze it in detail in the next sections.

D) Receiver Sensitivity

Receiver sensitivity is defined as the minimum receiver input power, by which the minimum performance of the communication system is achieved. Bit Error Rate (BER) is used as the performance measure in many communication systems and specially in WSN (See Table V-2). As deduce from Table V-2, maximum BER value of 1e-3 has been accepted as standard value in WSN applications. So the objective in our work is to obtain BER less than 1e-3.

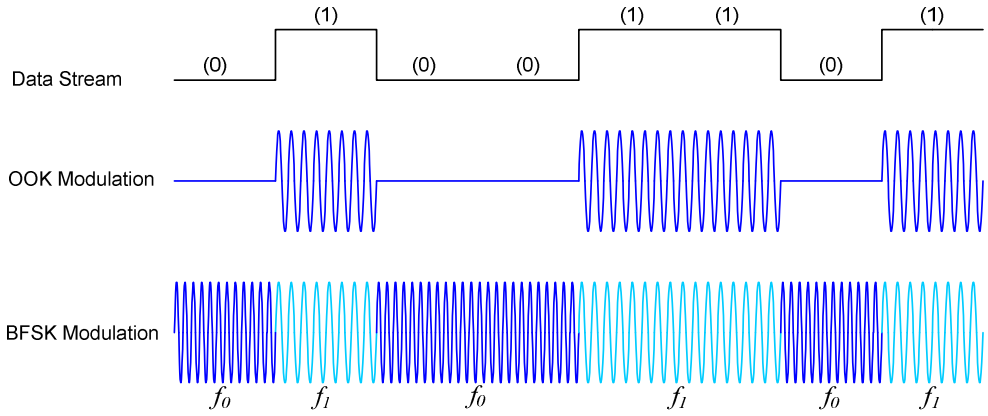


Fig. V-10. Principle of OOK and BFSK modulations

[1] Pulse Position Modulation
[2] Ultra Wide Band
[3] Federal Communication Commission

For a given modulation scheme, BER is a function of SNR. Theoretical value of required SNR to achieve BER of 1e-3 with OOK modulation is 16dB [71]. In a dense WSN maximum range (distance between two communicating nodes) is about few tens of meters. For example, Rabaey et *al.* (Frontiers of WSN in Berkeley wireless research center) have designed their WSN node for less than 10 meters [73], [78]. Similarly, in [71] less than 10 meters range has been considered. In [77] sensor node has been designed for 16 meters range. In [80] 10-20 meters range has been considered and in some other works the sensor nodes have been designed for 20 and 30 meters range [76]. Regarding this suggestion, we have considered the maximum nodes distance equal to 10 meters in our work.

After determining the transmitter radiation power and range, the receiver sensitivity can be calculated using Friis wave propagation equation [92]. It must be noted that accurate calculation of the path loss, specially for indoor applications is very complicated and Friis equation calculated the path loss for a point-to-point communication. However this equation can be used as a primary design guideline in WSN applications [71]. Friis equation calculates the ratio of received power to transmitted power:

$$\frac{P_r}{P_t} = \left(\frac{\lambda}{4\pi d}\right)^2 G_r G_t \qquad \text{(V-5)}$$

Where P_r and P_t are received and transmitted powers, respectively, λ is wave length and d is the nodes distance. G_r and G_t are the receiver and transmitter antennas gain, respectively.

Integration of antenna on chip is possible in mm-wave band and half- wavelength dipole antenna is a good choice for this purpose [93]. Maximum directivity of half-wavelength dipole is 1.64 and hence for an antenna with 100% radiation efficiency, the gain of 2.15dB is expected [94]. However, integrated antenna in CMOS technologies suffers from high substrate loss and hence the antenna gain is considerably reduced. Half- wavelength dipole antenna has been designed and measured in [93], in bulk CMOS and HR[1]-SOI CMOS technologies in K_a band. In bulk CMOS, gain of -8dB has been measured at 36GHz and in SOI CMOS the measured gain is -2dB at 40 GHz. We consider half- wavelength dipole in our design and the antenna gain is assumed to be -8dB for both of receiver and transmitter. We assume -7dB gain for both of receiver and transmitter antennas at 30GHz.

Now, for given carrier frequency of 30GHz, node distance of 10 meter, transmitted power of 5dBm and antenna gain of -7dB, we can calculate the required receiver sensitivity from (V-5). The calculated required sensitivity is equal to -90.5dBm.

E) Data Rate and Receiver Band Width

In the preceding section we calculated the minimum SNR and the receiver sensitivity equal to 16dB and -90.5dB, respectively. To calculate the receiver band width we use (V-4). For this purpose the receiver noise figure must be determined. Based on our experience NF 8dB is achievable in our work. This is not strange, considering the reported values of NF in mm-wave band and 90nm CMOS technology [13], [14]. Now using (V-4) the receiver band width is calculated:

$$BW = 10^{\left(\frac{Sensitiviyt+174-SNR-NF}{10}\right)} = 890KHz \qquad \text{(V-6)}$$

This is the maximum bandwidth of the receiver. We can choose the bandwidth less than 890KHz to gain better sensitivity or to relax the noise figure requirement. The receiver data rate (bit-per-second) is chosen equal to the receiver bandwidth.

[1] High Resistivity

V.2.2 Transceiver Architecture

The specifications of the developed radio link have been listed in Table V-3. Based on the features of this radio link we propose the transceiver structure for our work. The transceiver architecture in our work has been shown in Fig. V-11. To relax the isolation between transmitter and receiver, we have used TR switch, instead of duplexer. This is necessary, since in our design receiver and transmitter are in the same frequency band. Remind that in networks for which the receivers communicate with a single base station, such as mobile phone cellular networks, TX and RX can be in different frequency. However in WSN applications all of the sensor nodes must have the ability to communicate with each other and hence the RX and TX must be at same frequency. All blocks of the receiver and transmitter can be switched to idle or active states to save the battery energy.

In receiver branch, the Image Reject Filter (IRF) has been placed prior to LNA to reject the input signals in the image band. Even-harmonic mixer has been adopted for lowering the VCO[1] power consumption and to increase the VCO signal quality [95], [96], [97], [98]. As will be explained later, in the even harmonic mixer the VCO frequency is half of the required LO frequency in conventional mixer. This eliminates the frequency pulling due to the leakage signals with frequency close to the VCO frequency [73]. In addition, VCO power consumption decreases drastically with decreasing the frequency [76]. Multi-slice IF amplifier and limiter, proposed in [71], has been used for increasing the receiver's dynamic range and improving the receiver performance, without any power budget. In each slice, the last IF amplifier acts as a limiter. At any time instance, only one slice is active, depending on the received signal strength. IF slice (IF gain) selection is performed by the RSSI[2] unit that measures the input signal strength [99]. The signal amplitude is extracted by an envelope detector. Then a comparator is used for decide that the input data is "1" or "0". Demodulation of OOK signal is performed by envelope detection and simple comparison with a threshold voltage.

Transmitter is composed of a simple power VCO. Although OOK modulations permit the use of non-linear high efficiency class E power amplifiers, we encountered with some problems in drive stage of class E power amplifier in 30GHz band.

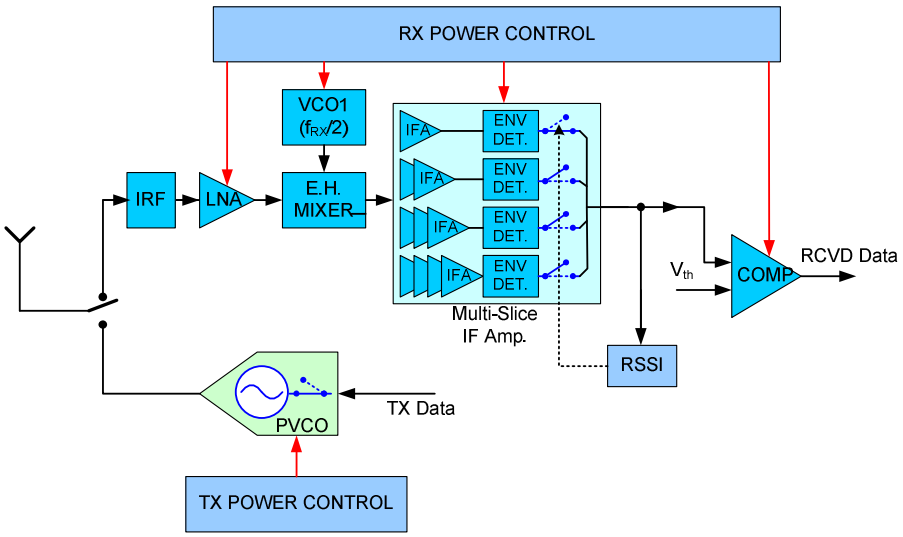


Fig. V-11. Proposed transceiver architecture with multi-slice IF amplifier and EHM in the receiver and power oscillator (PVCO) in the transmitter

[1] Voltage Controlled Oscillator
[2] Received Signal Strength Indicator

Table V-3
Features of the Designed Radio Link

Carrier Frequency	IF Frequency	RX Sensitivity	TX Power	Channel Modulation	Data Rate	Band Width	RX Noise Figure
30GHz	2GHz	-90.5dBm	5mW	OOK	890KBps	890KHz	8dB

V.2.3 The Receiver Architecture

The receiver branch is composed of LNA, VCO, even-harmonic mixer, multi-slice IF amplifier, envelope detector and comparator. The LNA has been described in Chapter IV. Other blocks are described briefly here.

V.2.3.1 VCO Block

Frequency source of a coherent receiver is very complicated and is a power hungry part of receiver. However in WSN receivers in which receiver is non-coherent, a simple VCO is sufficient and as mentioned, even in the case of low RF frequency, VCO is not needed. Due to its low power, high start-up reliability and good tuning range and differential output, cross-coupled oscillator is the most popular VCO circuit in CMOS RF transceivers [100], [101], [102]. In low power applications, complementary cross-coupled architecture is preferred over only-NMOS cross-coupled architecture [101], [103], [104]. For equal bias current, voltage swing of complementary cross-coupled is twice of the only-NMOS cross-coupled. Regarding to the Lesson phase noise equation [103], phase noise is inversely proportional with the square of the voltage swing.

The main this advantage of cross-coupled VCO is its high noise phase. Phase noise is the most important parameter of VCO for high data rate communication, but is not important for low data rate non-coherent receivers [76], [103], [73]. In high data rate receivers, phase noise causes jittering in the received pulses and this lowers the eye diagram opening in horizontal direction. If pulse duration is low, the eye opening reduction can cause noticeable increase of BER [105]. As mentioned, WSNs are low data rate systems and hence phase noise is not critical for them.

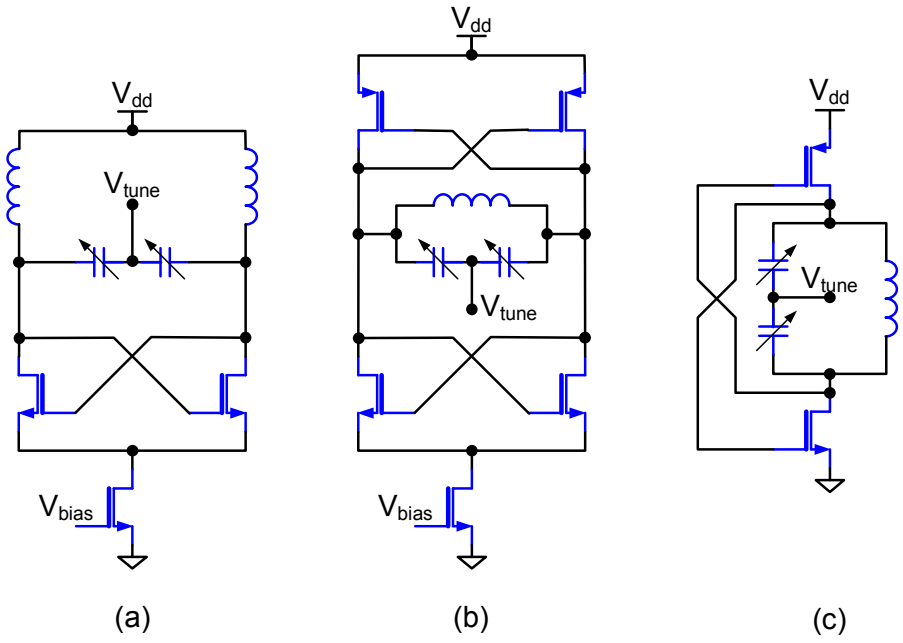


Fig. V-12. Schematic view of NMOS cross-coupled (a), complementary cross-coupled (b) and current reuse cross-coupled (c) oscillators

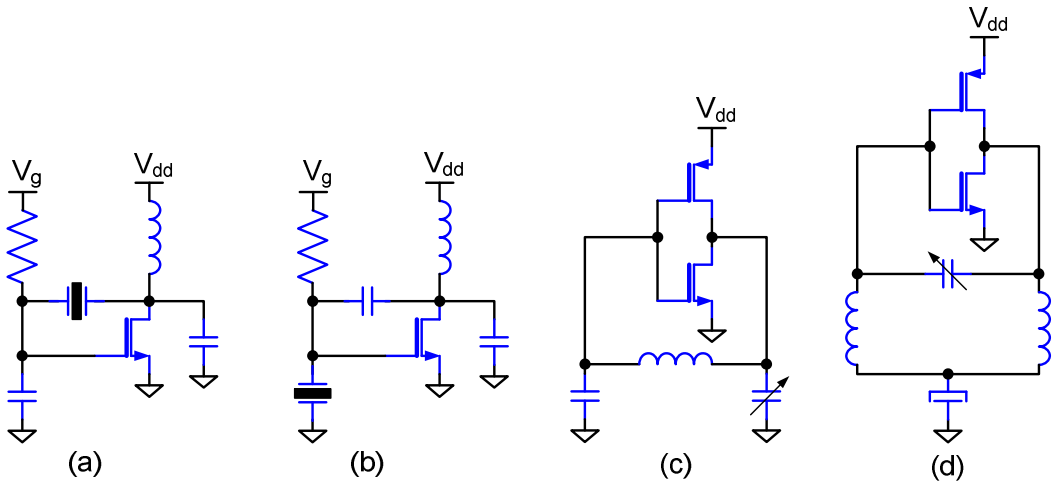


Fig. V-13. Schematic view of Pierce oscillator (a), Miller oscillator (b) [107] and the oscillators proposed in our work: current reuse Pierce-like oscillator (c) and current reuse Miller-like oscillator (d)

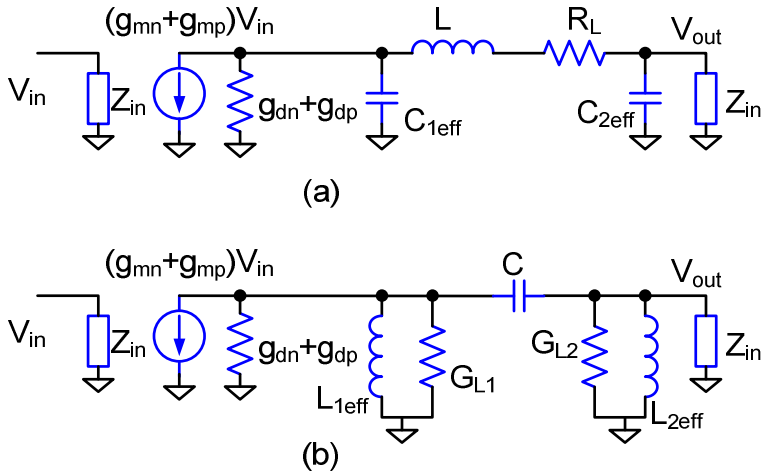


Fig. V-14. Small signal model of Pierce-like (a) and Miller-like (b) oscillators

Cross-coupled topology has been considered in WSN applications [103], [73]. Nevertheless other VCO circuits may be necessary in some cases. Due to low efficiency of power amplifiers in low power transmitters (See Table V-1), the trend in WSN is to avoid them or use very simple power amplifiers. One solution is using power oscillator in transmitter, by which the oscillator is connected directly to antenna [103], [73]. However when oscillator is connected to antenna, antenna load reduces the VCO quality factor and reduces the frequency stability.

To overcome this problem, a simple ultra low power reference oscillator is required. For example, in [73] a simple 90uW FBAR oscillator with Pierce topology has been used for injection locking the power oscillator. Some other simple oscillator circuits have been used in WSN applications [72], [75]. Tuned Input-Tuned Output (TITO) configuration was reported in 2008 in [102]. Current reuse is a common way to reduce power consumption in low power applications. Two current reuse oscillator circuits have been proposed for WSN applications. One circuit is obtained with some modification of complementary cross coupled oscillator [76], [79], denoted as current reuse cross-coupled, and the other is a Pierce oscillator [106].

We have examined three oscillator circuits in our work. First circuit is the above mentioned current reuse cross-coupled configuration. This circuit has been shown in Fig. V-

12, in comparison with NMOS and complementary cross-coupled oscillators. Two other circuits are modifications of Pierce and Miller oscillators [107], as shown in Fig. V-13 and we denote them as Pierce-like and Miller-like configurations, respectively. So we excluded it from our investigation.
To investigate the characteristics of three low power oscillators, i.e. current reuse cross-coupled, Pierce-like and Miller-like oscillators, and compare them we perform a simple analysis.

A) Pierce-like Oscillator

The small signal equivalent of Pierce-like oscillator has been shown in Fig. V-14. Miller equivalent of gate–drain feedback capacitance has been considered as a part of gate and drain nodal capacitances. Using this figure the loop gain is calculated as:

$$\frac{V_{out}}{V_{in}} = -\frac{g_{mn}+g_{mp}}{1-\omega^2 L\left(1-\frac{j}{Q}\right)\left(C_2+C_g\right)}\frac{1}{Y} \tag{V-7}$$

where:

$$Y = g_{dn}+g_{dp}+j\omega\left(C_1+C_d\right)+\frac{j\omega\left(C_2+C_g\right)}{1-\omega^2 L\left(1-\frac{j}{Q}\right)\left(C_2+C_g\right)} \tag{V-8}$$

Q is the inductor's quality factor:

$$Q = \frac{L\omega}{R_L} \tag{V-9}$$

And C_g and C_d are equivalent input capacitances of two transistors at gate and drain nodes, respectively. Using Miller approach and considering that in oscillation the gate-drain voltage gain is equal to -1, these capacitors are calculated as:

$$\begin{aligned} C_g &= C_{gsp}+C_{gsn}+2\left(C_{gdp}+C_{gdn}\right) \\ C_d &= C_{gdp}+C_{gdn} \end{aligned} \tag{V-10}$$

n and *p* denotes for NMOS and PMOS transistors, respectively. Assuming that the equivalent capacitance in gate and drain nodes are equal, we can write:

$$\begin{aligned} C &= C_2+C_g \\ C &= C_1+C_d \end{aligned} \tag{V-11}$$

Substituting (V-10) in (V-7) we rewrite the loop gain equation:

$$\frac{V_{out}}{V_{in}} = -\frac{g_{mn}+g_{mp}}{\left(g_{dn}+g_{dp}\right)\left(1-\omega^2 L\left(1-\frac{j}{Q}\right)C\right)+j\omega C\left(2-\omega^2 L\left(1-\frac{j}{Q}\right)C\right)} \tag{V-12}$$

For a given DC power consumption, the transistors small signal model elements are determined and hence we have two design parameters, i.e. *L* and *C*. Oscillation occurs when the loop gain is unity. Consequently the oscillation conditions and oscillation frequency is obtained:

$$\begin{cases} \omega C = \dfrac{g_{dn}+g_{dp}}{Q}+\dfrac{2}{\omega L} \\ A_L = \dfrac{g_{mn}+g_{mp}}{\omega L\left(g_{dn}+g_{dp}\right)\left(\dfrac{g_{dn}+g_{dp}}{Q}+\dfrac{1}{\omega L}\right)+\left(\dfrac{g_{dn}+g_{dp}}{Q}+\dfrac{2}{\omega L}\right)^2\dfrac{\omega L}{Q}} > 1 \end{cases} \tag{V-13}$$

In practice there are many losses in the circuit, such as inductors and substrate losses that can be modeled as a shunt conductance at the drain node. Consequently, we rewrite the oscillation condition as:

$$A_L = \frac{g_{mn} + g_{mp}}{\omega L\left(g_{dn} + g_{dp}\right)\left(\frac{g_{dn} + g_{dp}}{Q} + \frac{1}{\omega L}\right) + \left(\frac{g_{dn} + g_{dp}}{Q} + \frac{2}{\omega L}\right)^2 \frac{\omega L}{Q} + g_{loss}} > 1 \quad \text{(V-14)}$$

where g_{loss} is the conductance equivalent to the losses. If we assume ideal inductor, the equations reduce to:

$$\begin{cases} f = \frac{1}{\pi}\sqrt{\frac{1}{2LC}} \\ A_L = \frac{g_{mn} + g_{mp}}{g_{dn} + g_{dp} + g_{loss}} > 1 \end{cases} \quad \text{(V-15)}$$

Obviously, more loss in the circuit corresponds to higher g_m and hence more power consumption.

B) Miller-like Oscillator

In the case of Miller-like configuration, using Fig. V-14(b) we deduce:

$$\frac{V_{out}}{V_{in}} = -\frac{j\omega C\left(g_{mn} + g_{mp}\right)}{\frac{1}{j\omega L_2} + j\omega\left(C_g + C\right) + G_{L2}} \frac{1}{Y} \quad \text{(V-16)}$$

where:

$$Y = g_{dn} + g_{dp} + j\omega C_d + G_{L1} + \frac{1}{j\omega L_1} + \frac{j\omega C\left(\frac{1}{j\omega L_2} + G_{L2} + j\omega C_g\right)}{j\omega C + \frac{1}{j\omega L_2} + G_{L2} + j\omega C_g} \quad \text{(V-17)}$$

And G_{Li} is equivalent to the inductor's loss, defined as:

$$G_{Li} = \frac{Q_i}{\omega L_i\left(1 + Q_i^2\right)} \quad \text{(V-18)}$$

Assuming that effective shunt inductance in gate and drain is equal, we can write:

$$\begin{aligned} \frac{1}{j\omega L} + G &= j\omega C_d + G_{L1} + \frac{1}{j\omega L_1} \\ \frac{1}{j\omega L} + G &= j\omega C_g + G_{L2} + \frac{1}{j\omega L_2} \end{aligned} \quad \text{(V-19)}$$

where L is effective shunt inductance in gate and drain nodes and G represents the quality factor of the effective inductance and is calculated as:

$$G = \frac{Q}{\omega L\left(1 + Q^2\right)} \quad \text{(V-20)}$$

C_g and C_d are similar to the previous section, calculated in (V-10). Substituting (V-10) and (V-19) in (V-17) we obtain:

$$Y = \frac{\left(g_{dn} + g_{dp}\right)\left(j\omega C + \frac{1}{j\omega L} + G\right) + \left(\frac{1}{j\omega L} + G\right)\left(2j\omega C + \frac{1}{j\omega L} + G\right)}{j\omega C + \frac{1}{j\omega L} + G}$$

And using (V-16) we calculate the loop gain:

$$\frac{V_{out}}{V_{in}} = -\frac{j\omega C\left(g_{mn}+g_{mp}\right)}{\left(g_{dn}+g_{dp}\right)\left(j\omega C+\frac{1}{j\omega L}+G\right)+\left(\frac{1}{j\omega L}+G\right)\left(2j\omega C+\frac{1}{j\omega L}+G\right)} \tag{V-21}$$

Oscillation occurs when the loop gain is unity and hence we obtain the oscillation conditions, after substituting G from (V-20):

$$\begin{cases} \omega C = \dfrac{1}{2\omega L} - \dfrac{Q}{2\left(1+Q^2\right)}\left(\dfrac{Q}{\omega L\left(1+Q^2\right)}+g_{dn}+g_{dp}\right) \\ A_L = \dfrac{\omega^2 LC\left(g_{mn}+g_{mp}\right)}{\left(g_{dn}+g_{dp}\right)\left(1-\omega^2 LC\right)+\dfrac{2Q\left(1-\omega^2 LC\right)}{\omega L\left(1+Q^2\right)}+\omega^2 LCg_{loss}} > 1 \end{cases} \tag{V-22}$$

C) Current Reuse Cross-Coupled

To analyze the current reuse cross-coupled oscillator, consider Fig. V-15. The oscillation occurs when the admittance seen from X-Y nodes is equal to the negated of LC resonance circuit admittance. Regarding to Fig. V-15, from the small signal model we can write:

$$\begin{aligned} I_{on} &= g_{dsn}V_{on} + g_{mn}V_{op} + j\omega C_{gdn}\left(V_{on}-V_{op}\right) \\ I_{op} &= g_{dsp}V_{op} + g_{mp}V_{on} + j\omega C_{gdp}\left(V_{op}-V_{on}\right) \end{aligned} \tag{V-23}$$

Subscribes n and p denotes NMOS and PMOS transistors, respectively . On the other hand, in the oscillator we have:

$$\begin{aligned} V_{osc} &= V_{op} - V_{on} \\ I_{on} &= -I_{op} \end{aligned} \tag{V-24}$$

So after some calculations we deduce:

$$\begin{aligned} V_{on} &= \frac{j\omega\left(C_{gdn}-C_{gdp}\right)-g_{mn}-g_{dsp}}{g_{dsn}+g_{mn}+g_{dsp}+g_{mp}}V_{osc} \\ V_{op} &= \frac{j\omega\left(C_{gdn}-C_{gdp}\right)+g_{dsn}+g_{mp}}{g_{dsn}+g_{mn}+g_{dsp}+g_{mp}}V_{osc} \end{aligned} \tag{V-25}$$

And the admittance to the X-Y nodes pair is obtained:

$$\begin{aligned} Y_{XY} &= \frac{I_{op}}{V_{osc}} \\ &= \frac{j\omega\left(C_{gdn}-C_{gdp}\right)\left(g_{dsp}+g_{mp}\right)+g_{dsp}\left(g_{dsn}+g_{mp}\right)-g_{mp}\left(g_{mn}+g_{dsp}\right)}{g_{dsn}+g_{mn}+g_{dsp}+g_{mp}} + j\omega C_{gdp} \end{aligned} \tag{V-26}$$

Oscillation occurs when Y_{XY} is equal to the minus of the LC resonance circuit. Consequently we obtain:

$$\frac{j\omega C_{gdn}\left(g_{dsp}+g_{mp}\right)+j\omega C_{gdp}\left(g_{dsn}+g_{mn}\right)+g_{dsp}g_{dsn}-g_{mp}g_{mn}}{g_{dsn}+g_{mn}+g_{dsp}+g_{mp}} = \frac{Q\left(jQ-1\right)}{\omega L\left(Q^2+1\right)} - j\omega C \tag{V-27}$$

After some manipulations we obtain the oscillation conditions:

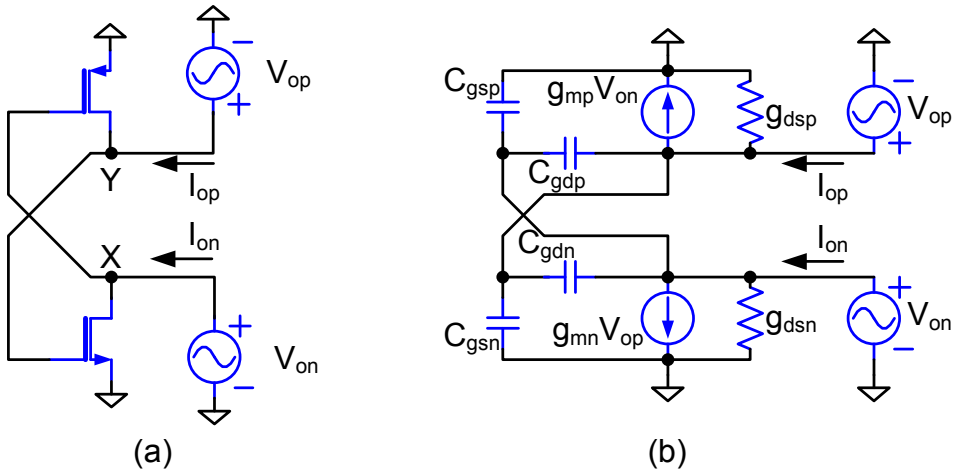


Fig. V-15. (a) Equivalent circuit and (b) small signal model of current reuse cross-coupled oscillator

$$\begin{cases} \omega C = \dfrac{Q^2}{\omega L\left(Q^2+1\right)} - \dfrac{\omega C_{gdn}\left(g_{dsp}+g_{mp}\right)+\omega C_{gdp}\left(g_{dsn}+g_{mn}\right)}{g_{dsn}+g_{mn}+g_{dsp}+g_{mp}} \\ \dfrac{g_{mn}g_{mp}-g_{dsp}g_{dsn}}{g_{dsn}+g_{mn}+g_{dsp}+g_{mp}} > \dfrac{Q}{\omega L\left(Q^2+1\right)} \end{cases} \quad \text{(V-28)}$$

For compatibility with the two later analyses, we define the loop gain, considering additional losses:

$$A_L = \frac{\omega L\left(Q^2+1\right)\left(g_{mn}g_{mp}-g_{dsp}g_{dsn}\right)}{Q\left(g_{dsn}+g_{mn}+g_{dsp}+g_{mp}\right)} > 1 \quad \text{(V-29)}$$

D) Comparing the Oscillators

Using the analytic equations derived in the previous section, we compare three oscillator circuits to choose the proper one for our applications. Regarding section V.2.2.1, VCO frequency in our transceiver is half of the carrier frequency. Consequently, we compare three VCOs at 15GHz. Regarding the analytic equations, we have freedom in selecting the inductor value for all of the above oscillators. This is very useful, because the inductor has its individual optimization process, but each capacitance is easily by MIM capacitors. Based on our experience, we choose the inductance equal to 600pH for all three oscillators and the quality factor is obtained equal to 15. To obtain maximum swing, the NMOS and PMOS transistors are sized to achieve $V_{dd}/2$ volts at the drain.

With these conditions we have used our MOS transistor model for designing three oscillators for various power consumptions. The loop gain of Pierce-like, Miller-like and current reused cross-coupled oscillators have been shown in Fig. V-16. The loop gains have been calculated using (V-12), (V-21) and (V-29), respectively. Note that for all powers, the phase of loop gains are zero. This figure has very important implications: For high power applications, the current reused cross-coupled topology has excellent loop gain. High loop gain implies that the oscillator has very good drive capability. However for low power

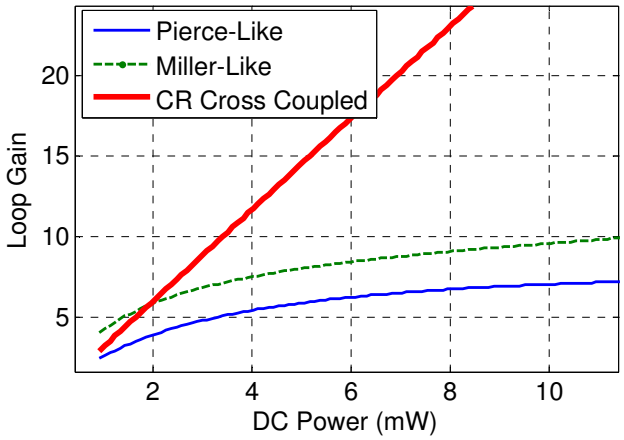


Fig. V-16. Loop gain of Pierce-like, Miller-like and current reused cross-coupled oscillators at 15GHz, designed with various DC powers using (V-12), (V-21) and (V-29), respectively.

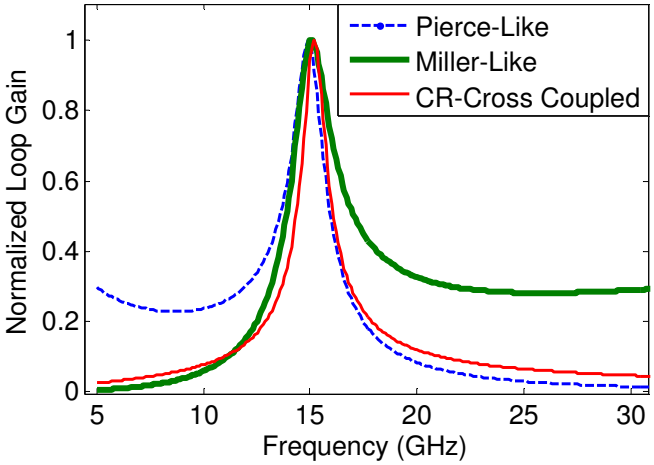


Fig. V-17. Loop gain of Pierce-like, Miller-like and current reused cross-coupled oscillators as a function of frequency, designed at 15GHz

applications, less than 2mW in our case optimized Miller oscillator out performances the current reused cross-coupled topology. Consequently this oscillator is a good choice for WSN applications. Optimized Miller oscillator has week performance, in comparison with two other oscillators. Fig. V-17 shows the loop gain of three oscillators, as a function of frequency. The oscillators have been designed for 1mW power consumption and 15GHz oscillation frequency. This figure shows that the feedback network of Pierce-like and Miller-like oscillators have low-pass and high-pass nature, respectively, as it is evident from their circuits. As we will show, high-pass nature of Miller-like oscillator leads to semi-square signal that is useful in power amplifier drive circuits.

To compare the swing and phase noise of three oscillators, we have designed them using the derived equations, for 15GHz and 1mW. Then the designed oscillators have been simulated in the STMicroelectronics CMOS 90nm design kit. Fig. V-18 shows the phase noise of three oscillators. Miller-like oscillator has the best phase noise, -83dBc/Hz at 100KHz offset. As we mentioned, phase noise is not important in low data rate communications, especially in dense WSN applications. Waveforms of oscillators have been shown in Fig. V-19. From this figure we deduce that Miller-like oscillator has semi-square signal that is useful in driving switch mode power amplifiers.

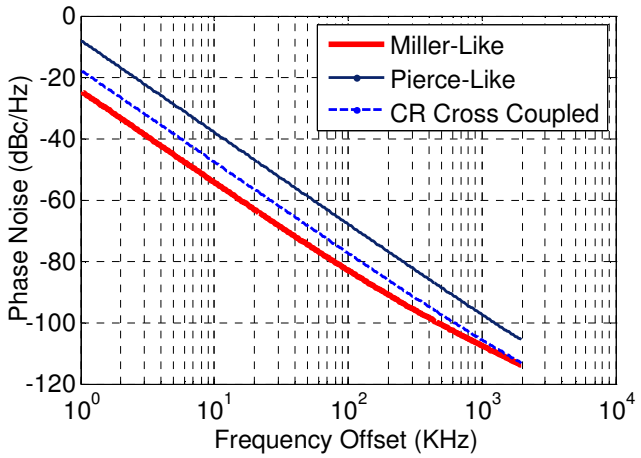


Fig. V-18. Phase noise of 1mW, 15GHz Pierce-like, Miller-like and current reused cross-coupled oscillators, simulated using foundry design kit and Spectre-RF simulator

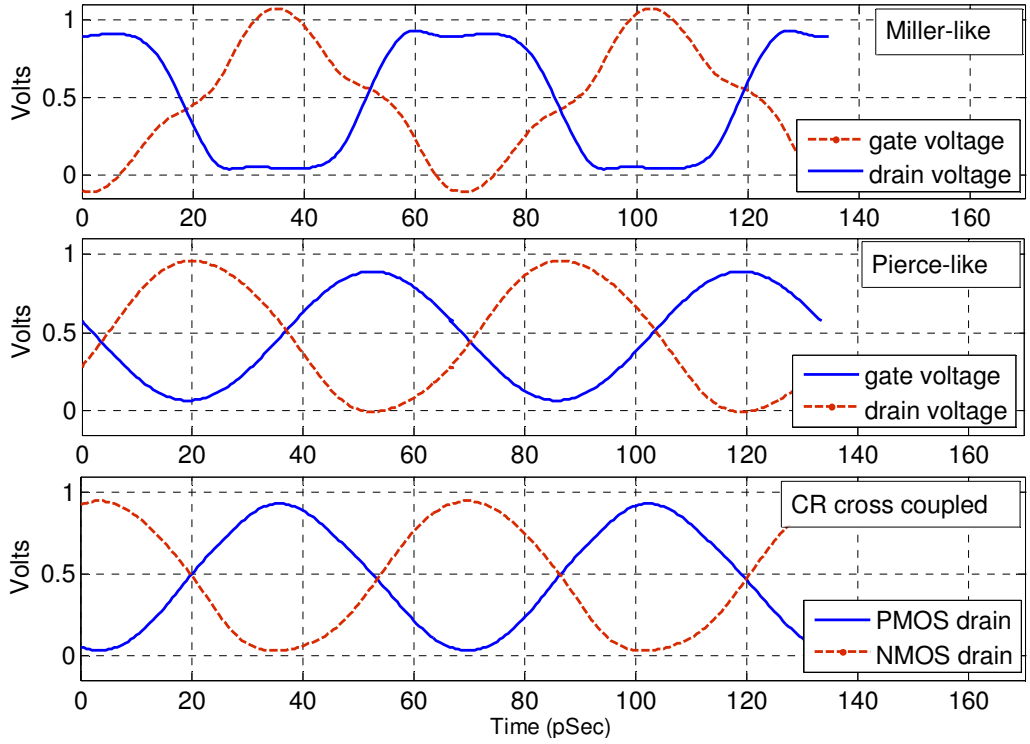


Fig. V-19. Wave forms of 1mW, 15GHz Pierce-like, Miller-like and current reused cross-coupled oscillators, simulated using foundry design kit and Spectre-RF simulator

As we mentioned, the semi-square waveform is due to the high pass nature of feedback network in Miller-like oscillator. Wave forms of Pierce-like and current reuse cross coupled oscillators are the same, but regarding Fig. V-16, the later has higher driving capability. In addition, current reuse cross-coupled oscillator is suitable for the cases in which VCO with differential outputs is required. In Miller-like configuration, the inductors are grounded in one end and this makes possible use of line-type inductors.

As a consequence of the above suggestions, we have chosen current reuse cross coupled oscillator as local oscillator for the receiver and Miller-like oscillator as direct modulator and driver for class-E power amplifier in the transmitter.

V.2.3.2 Even Harmonic Mixer

Sub Harmonic Mixers (SHM) offer an alternative solution to fundamental mixers, possessing some advantages over fundamental mixers, in some applications. Unlike fundamental mixers, in which the VCO frequency is equal to the required LO frequency, in n^{th} order SHM, the VCO frequency is equal to *1/n* of the LO frequency. Due to some limitations, practical value of *n* is not greater that 4 [108], [84]. SHMs with even value of n are known as Even Harmonic Mixers (EHM).

The leakage generated by the coupled LO signal is the most important design issue in direct conversion receivers. As explained in section V.1.3.1, LO signal leakage enters into the mixer and generates DC components in the mixer output that degrades the received signal quality. This problem can be drastically reduced by using EHMs [96], [109], [108]. The other advantage of SHM is reducing the pulling effect of the power amplifier output signal. Power amplifier output is a high power wide spectrum signal and can leak into the VCO and reduce the VCO output quality by pulling its frequency [73]. In mm-wave applications, in addition of the above advantages, using SHMs allows use of low frequency VCO with better phase noise, higher output power and lower DC power consumption [110], [84], [111], [109].

Sub-harmonic technique can be applied for both of active and passive mixers. Like fundamental harmonic passive mixers, passive SHMs have lower DC power consumption and better noise performance, in expense of low conversion gain. In addition they are free of DC offset, an important issue for direct conversion receivers [109], [112]. In contrast to passive SHMs, active SHMs offers high conversion, higher linearity and higher reverse isolation that makes them attractive for many applications, specially in mm-wave band [110], [96]. In frequencies well below mm-wave band, 4^{th} order SHM with doubly balanced Gilbert cell structure posses good performance [108]. However this mixer needs 8-pahse LO signal that is very difficult to achieve in mm-wave band. Simple mixer circuits, such as gate-pumped [110] and single-balanced active CMOS mixer [96] are of more interest in mm-wave band.

We have used the EHM circuit proposed in [96], with small difference. Conventional single balanced active CMOS mixer, the even harmonic mixer proposed in [96] and the similar one in our work have been depicted in Fig. V-20. In our design IF filter has been merged in the mixer, to reduce the power consumption and increase the conversion gain. Here after we denote the EHM of Fig. V-20 as *active CMOS EHM*. In a conventional single balanced active CMOS mixer, the RF signal is applied to the gate of tail transistor and the differential pair transistors are switched (in ideal case) on/off by LO signal. In contrast, in the active CMOS EHM the RF signal is applied to the differential pair transistors and the LO is applied to the tail transistors.

The operation principles of both of mixers have been depicted in Fig. V-21. To compare the performance of these mixers, we calculate their conversion gain in ideal operation condition. Assuming single-tone RF signal, for conventional active CMOS mixer we can write:

$$\begin{aligned} i_d^+ &= g_m v_{RF} P_T(t) = g_m V_{RF} \cos(\omega t) P_T(t) \\ i_d^- &= g_m v_{RF} P_T(t - T/2) = g_m V_{RF} \cos(\omega t) P_T(t - T/2) \end{aligned} \quad \text{(V-30)}$$

where w is the carrier angular frequency, gm is the tail transistor's trans-conductance and $P_T(t)$ is the pulse train with period T and unit amplitude. Using Fourier series expansion of $P_T(t)$ and tacking the low frequency terms in the expansion of (V-30) we deduce:

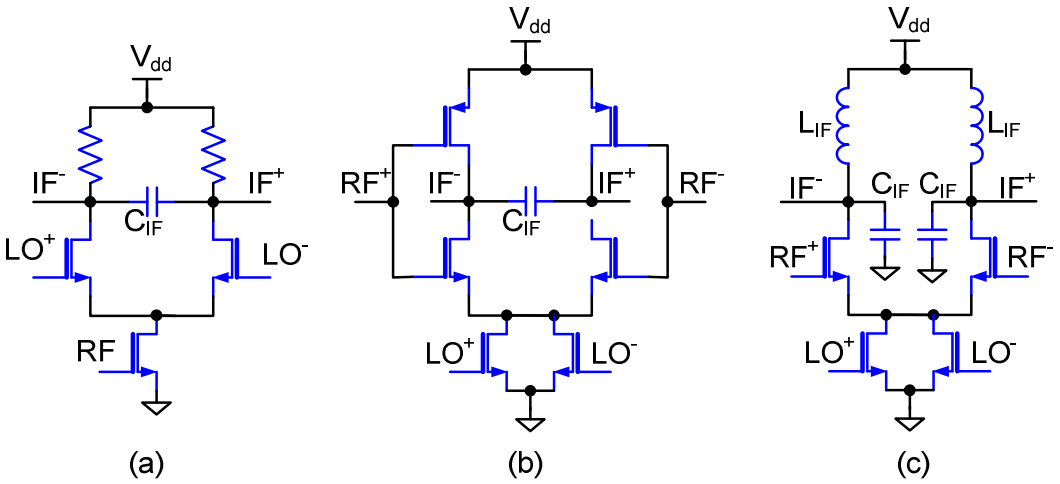


Fig. V-20. Conventional active CMOS mixer, the even harmonic mixer proposed in [96] and the even harmonic mixer in our work

$$i_d^+ = \frac{1}{\pi} g_m V_{RF} \cos\left((\omega - \omega_0)t\right)$$
$$i_d^- = \frac{-1}{\pi} g_m V_{RF} \cos\left((\omega - \omega_0)t\right) \quad \text{(V-31)}$$

As an approximating, we assume that g_m is proportional to the transistor's current, i.e.

$$g_m(t) = \varphi \cdot i_d(t) \quad \text{(V-32)}$$

φ is the proportionality coefficient. So from (V-31) we obtain:

$$I_{IF} = \frac{2}{\pi} \frac{\varphi P_{DC}}{V_{dd}} V_{RF} \quad \text{(V-33)}$$

where I_{IF} is the amplitude of the IF component of drain current and V_{dd} is drain supply voltage. In the case of active CMOS EHM we have:

$$i_d^+ = \frac{\varphi P_{DC}}{V_{dd}} P_T(t) \frac{v_{RF}}{2}$$
$$i_d^- = \frac{\varphi P_{DC}}{V_{dd}} P_T(t) \frac{-v_{RF}}{2} \quad \text{(V-34)}$$

And with similar approach we obtain:

$$I_{IF} = \frac{2}{\pi} \frac{\varphi P_{DC}}{V_{dd}} V_{RF} \quad \text{(V-35)}$$

That is exactly the same as the active CMOS mixer. This shows that with equal DC power, the even harmonic mixer has potentially the same conversion gain as the active CMOS mixer.

To obtain an accurate analytic equation of active CMOS EHM, we deal with the realistic condition, in which the tail transistors are driven by a sinusoidal voltage, as shown in Fig. V-22. Reminding that in short-channel MOS transistors, for large gate-source voltage, the drain current is linear function of gate-source voltage, and regarding that the LO signal amplitude is well beyond the device threshold voltage, we can approximate the tail current as:

$$\begin{cases} i_t = \dfrac{\mu C_{ox} W}{L}\left(V_{gs} - \alpha V_{th}\right) & V_{gs} \geq \alpha V_{th} \\ i_t = 0 & V_{gs} < \alpha V_{th} \end{cases} \quad \text{(V-36)}$$

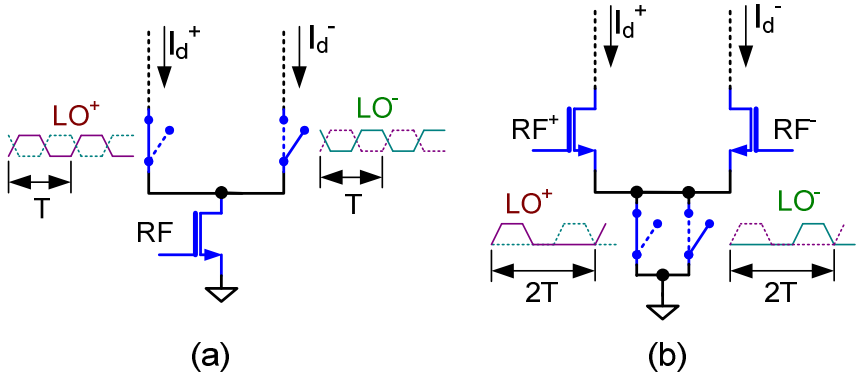


Fig. V-21. The operation principles of conventional active CMOS mixer and the active CMOS even harmonic mixer

Where α is a constant equal to 1.2. Accurate and approximated value of drain current has been shown in Fig. V22. Using this figure we can calculate the DC component and first harmonic of the tail current:

$$\begin{aligned} I_{t0} &= \frac{4}{T_o}\int_{-t_{on}}^{+t_{on}} \frac{\mu C_{ox} W}{L}\left(V_{LO}\cos(\omega_0 t)+V_o-\alpha V_{th}\right)dt \\ &= \frac{8}{T_o}\frac{\mu C_{ox} W}{L}\left(\frac{V_{LO}\sin(\omega_0 t_{on})}{\omega_0}+(V_o-\alpha V_{th})t_{on}\right) \\ I_{t1} &= \frac{4}{T_o}\int_{-t_{on}}^{+t_{on}} \frac{\mu C_{ox} W}{L}\left(V_{LO}\cos(\omega_0 t)+V_o-\alpha V_{th}\right)\cos(2\omega_0 t)dt \\ &= \frac{4}{T_o}\frac{\mu C_{ox} W}{L}\left(V_{LO}\left(\frac{\sin(\omega_0 t_{on})}{\omega_0}+\frac{\sin(3\omega_0 t_{on})}{3\omega_0}\right)+(V_o-\alpha V_{th})\frac{2\sin(2\omega_0 t_{on})}{2\omega_0}\right) \end{aligned} \quad \text{(V-37)}$$

where T_o and ω_o are period and angular frequency of the VCO, respectively and:

$$t_{on} = \frac{1}{\omega_o}\arccos\left(\frac{\alpha V_{th}-V_o}{V_{LO}}\right) \quad \text{(V-38)}$$

Now we can approximate the tail current:

$$i_t \approx I_{t0}+I_{t1}\cos(2\omega_0 t) \quad \text{(V-39)}$$

Note that higher components of the drain current have no effect on the conversion gain, but they cause losses in the equivalent resistance between the supply and ground.

$$\begin{aligned} i_d^+ &= \frac{i_t}{2}+\frac{\varphi V_{RF}}{4}\left(I_{t0}+I_{t1}\cos(2\omega_0 t)\right)\cos(\omega t) \\ i_d^- &= \frac{i_t}{2}-\frac{\varphi V_{RF}}{4}\left(I_{t0}+I_{t1}\cos(2\omega_0 t)\right)\cos(\omega t) \end{aligned} \quad \text{(V-40)}$$

High frequency components are filtered out and the IF current is obtained:

$$i_{IF}(t) = \frac{\varphi V_{RF}}{4} I_{t1}\cos((2\omega_0-\omega)t) \quad \text{(V-41)}$$

The mixer normalized conversion gain (trans-conductance) is obtained as:

$$CG_N = \frac{\varphi\mu C_{ox} W}{T_o L}\left(V_{LO}\left(\frac{\sin(\omega_0 t_{on})}{\omega_0}+\frac{\sin(3\omega_0 t_{on})}{3\omega_0}\right)+(V_o-\alpha V_{th})\frac{\sin(2\omega_0 t_{on})}{\omega_0}\right) \quad \text{(V-42)}$$

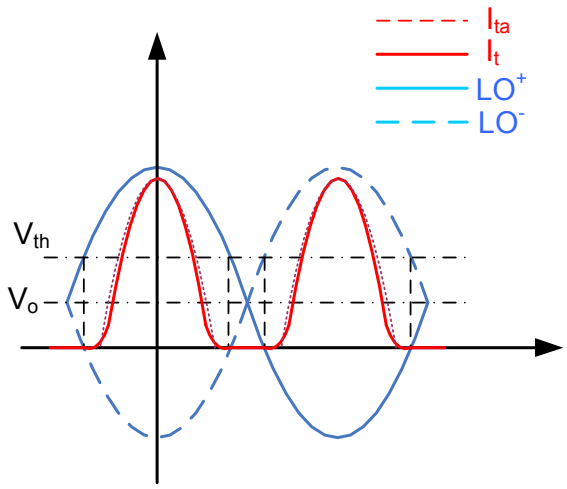


Fig. V-22. Representation of tail drive signal (LO signal) of active CMOS even harmonic mixer

On the other hand, power consumption of mixer is calculated using (V-37):

$$P_{DC} = V_{dd} I_{t0}$$
$$= \frac{8\mu C_{ox} W V_{dd}}{T_o L}\left(\frac{V_{LO}\sin(\omega_0 t_{on})}{\omega_0} + (V_o - \alpha V_{th})t_{on}\right) \quad \text{(V-43)}$$

So we deduce:

$$V_o = \frac{L T_o P_{DC}}{8 V_{dd}\mu C_{ox} W t_{on}} - \frac{V_{LO}\sin(\omega_0 t_{on})}{t_{on}\omega_0} + \alpha V_{th} \quad \text{(V-44)}$$

t_{on} is calculated using this (V-38) and for given P_{DC} and VCO signal frequency and amplitude, the VCO signal offset (gate bias of tail transistors) is calculated. Then the normalized conversion gain is calculated using (V-42). This makes possible to analytically calculate the optimum LO drive signal level and offset for the EHM. For example, normalized conversion gain of a 14GHz active EHM has been calculated using (V-42) with different DC power consumption values and has plotted in Fig. V-13 as a function of LO signal level. This figure shows that for each DC power, there is an optimum LO signal level.

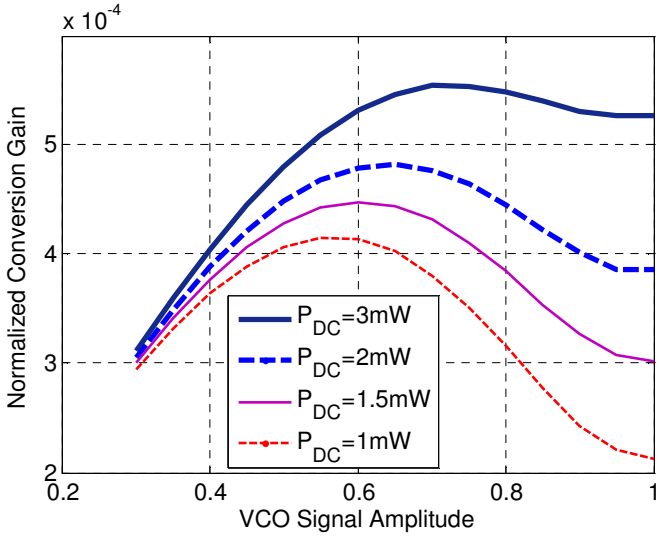


Fig. V-23. Normalized conversion gain of a 14GHz active EHM with different DC power consumptions, calculated using (V-42)

In our work, the VCO frequency and RF signal frequency are 14GHz and 30GHz, respectively. We have dedicated 2mW for mixer. The mixer was optimized using our analysis results and using optimization in Spectre-RF simulator and attached 90nm CMOS foundry design kit. Periodic Steady State (PSS) analysis, in conjunction with Periodic S-Parameters analysis was used for simulation of the designed mixer. S-parameters of the mixer have been shown in Fig. V-24. Both of input and output matching are good in the desired IF frequency. Conversion gain has been plotted in Fig. V-25. 4-dB conversion gain has been obtained at 2GHz. 3-dB band width is 180MHz and gain has ±0.5dB flatness in 60MHz bandwidth. Fig. V-26 shows the simulated single side band (SSB) and double side band (DSB) noise figures. Fig. V-27 shows the power spectrum of the supply voltage and the mixer draws 2.2mW DC power from 1V supply. Tail current of the mixer, obtained from simulation and from our analytic model has been shown in Fig. V-28. This figure reveals the accuracy of our simple model. Performance of the designed mixer has been compared with the recently published mm-wave mixers in Table V-4. Based on our knowledge, as the table shows, our design has superior performance for ultra low power applications.

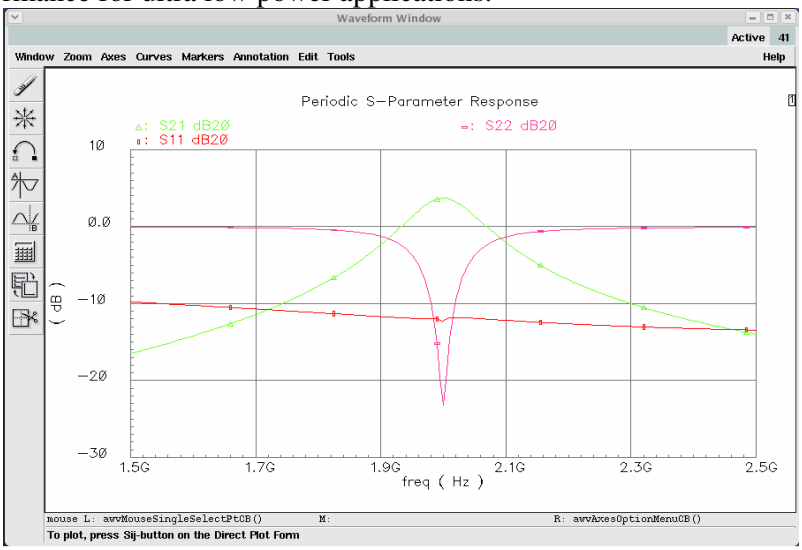


Fig. V-24. S-Parameters of the deigned mixer, simulated in Spectre-RF simulator and CMOS 90nm foundry design kit, with PSS and PSP analysis

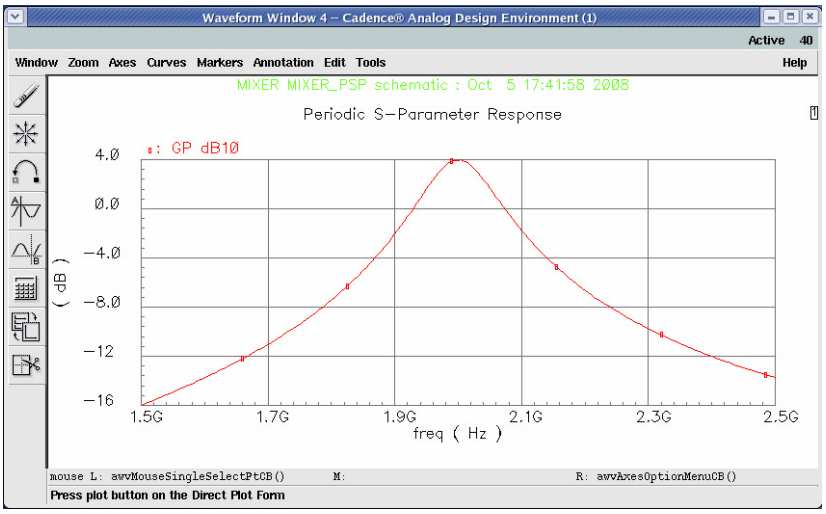


Fig. V-25. Conversion gain of the deigned mixer, simulated in Spectre-RF simulator and CMOS 90nm foundry design kit, with PSS and PSP analysis

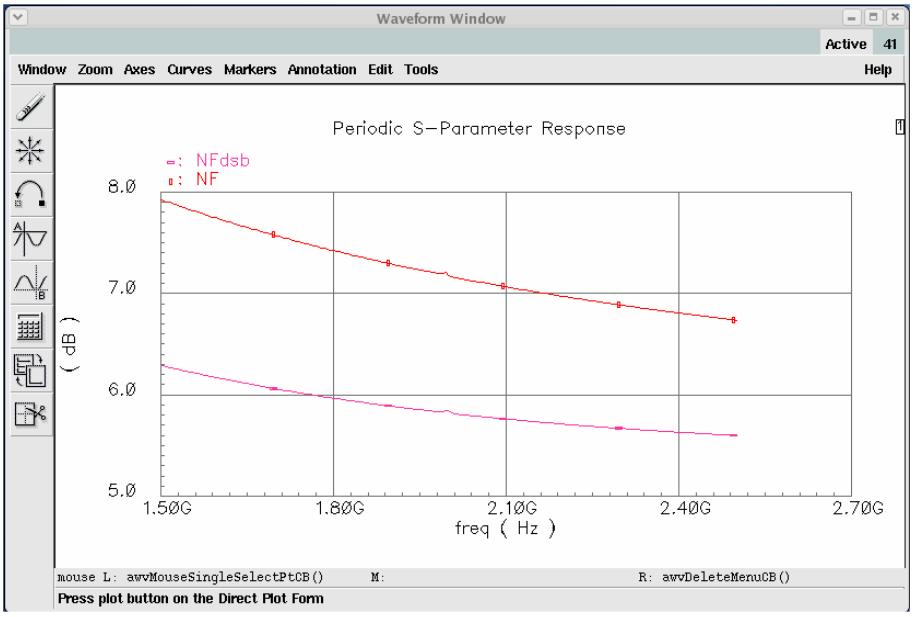


Fig. V-26. Single Side Band (SSB) and Double Side Band (DSB) noise figure of the deigned mixer, simulated in Spectre-RF simulator and CMOS 90nm foundry design kit, with PSS and PSP analysis

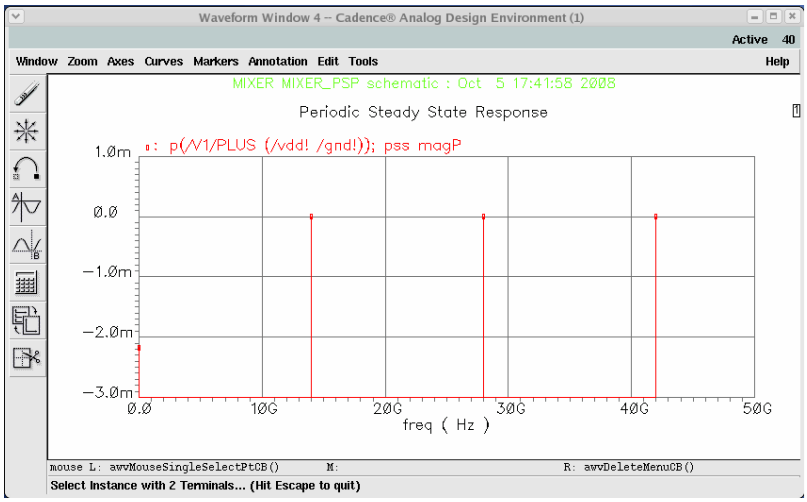


Fig. V-27. Power spectrum of the supply voltage in the deigned mixer, simulated in Spectre-RF simulator and CMOS 90nm foundry design kit, with PSS and PSP analysis

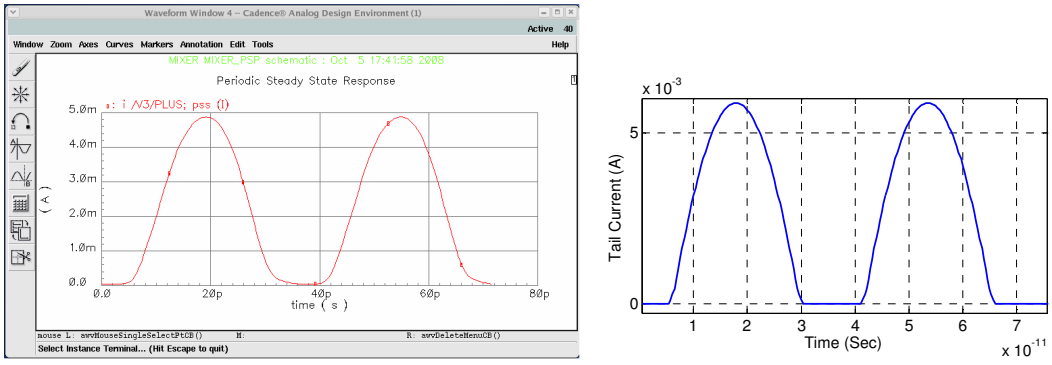


Fig. V-28. Tail current of the designed mixer, obtained from simulation in Spectre-RF (a) and obtained from our simple analytic model (b)

TABLE V-4
Comparison of Recently Published Ka Band Mixers

Ref.	Year	Topology	Technology	Frequency (GHz)	NF (DSB) (dB)	CG (dB)	DC Power (mW)
[109]	2008	D. Bal. Gilb Cell EHM	0.13um CMOS	24	10	3.2	21.8*
[113]	2004	S. Bal. Gilb. Cell	90nm CMOS	30	10.5	-2.6	20
[111]	2008	Gate Pumped SHM	GaAs	28~32	NA	-13~-15	9.3
[114]	2007	Gilb. Cell	90nm CMOS	25~75	NA	3	93
[115]	2007	Gilb. Cell	0.18um CMOS	28	15	12.5	40
This Work**	2008	Active EHM	90nm CMOS	30	5.8	4	2.2

*Plus RF pre-amp and IF buffer
**Simulation in Foundry design kit

V.2.3.3 IF and Base Band Circuits

IF stage has been designed as multi-slice amplifier, the voltage gain of each channel is one decade higher than the preceding channel. Regarding the received signal strength, proper channel and hence proper IF gain is chosen. This method eliminated the need for AGC and meanwhile preserves the advantages of AGC over limiter or logarithmic amplifiers. At each instance in the on period of the receiver, only one channel is active and the others are in idle state with very small power consumption. Schematic of the multi channel IF amplifier has been shown in Fig. V-29. Each amplifier cell is a simple inverter-like class A amplifier with a resistor between gate and drain of transistors [74]. This resistor has the self-bias roll, as well as feed back effect to linearize the amplifier. The last amplifier cells in each slice has the roll of limiter amplifier.

The multi-slice IF amplifier was designed and optimized using Spectre-RF simulator and the 90nm CMOS foundry design kit. Each CMOS stage draws about 100uA and 15nA in active and idle state, respectively. So maximum and minimum power consumption when receiver is on, is about 400uW and 100uW, respectively. Gain of the IF amplifier with different channel states have been shown in Fig. V-30.

Noise effect of the IF amplifier may be considerable when Channel I is on, i.e. in the maximum IF gain. In this state the IF amplifier has the worst noise performance. To investigate the noise effect, we have simulated the output noise voltage spectral density, when Channel I is active, shown in Fig. V-31. The noise spectral density in around 2GHz is about $6\mu V/\sqrt{Hz}$. Considering about 200KHz bandwidth of receiver, the voltage noise standard deviation is obtained 2.68 mV. As will be explained, we have designed the receiver for 300mV IF signal amplitude, prior to the detector and hence the noise of IF amplifier has no noticeable effect in the receiver performance.

The envelope detector is after IF amplifier and detects the IF signal amplitude. The envelope detector circuit schematic has been shown in Fig. V-32, that is a common-drain differential stage, biased close to the sub-threshold region. This stage converts the IF voltage signal to a rectified current signal that is filtered by a RC filter that keeps the low frequency (base band OOK pulses) and grounds the high frequency components.

The voltage transfer curve of the envelope detector and its power consumption has been obtained using simulation in Spectre-RF and has been depicted in Fig. V-33. The detector has linear response for the IF signal amplitude greater than about 100mV.

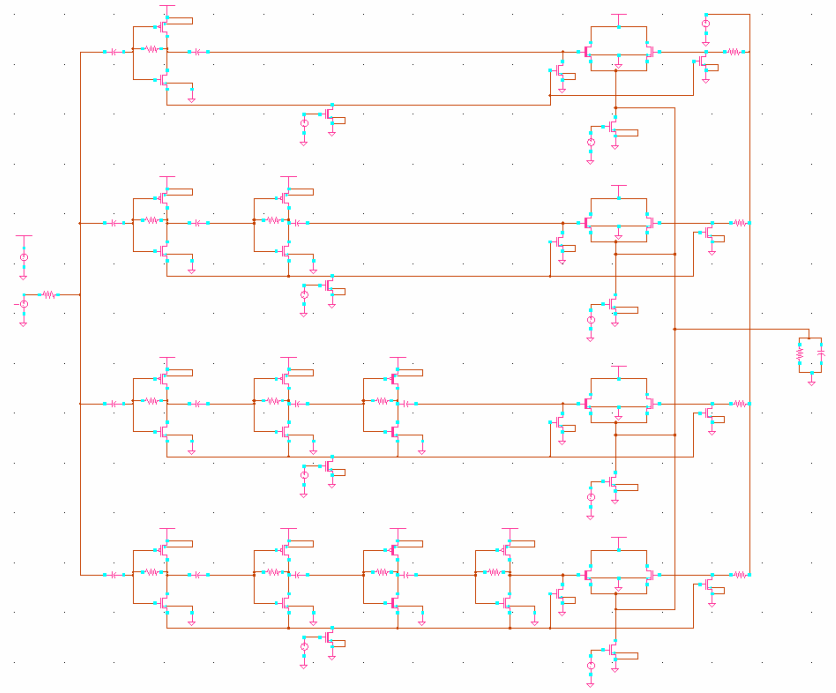


Fig. V-29. Schematic of the multi channel IF amplifier, in CADENCE environment

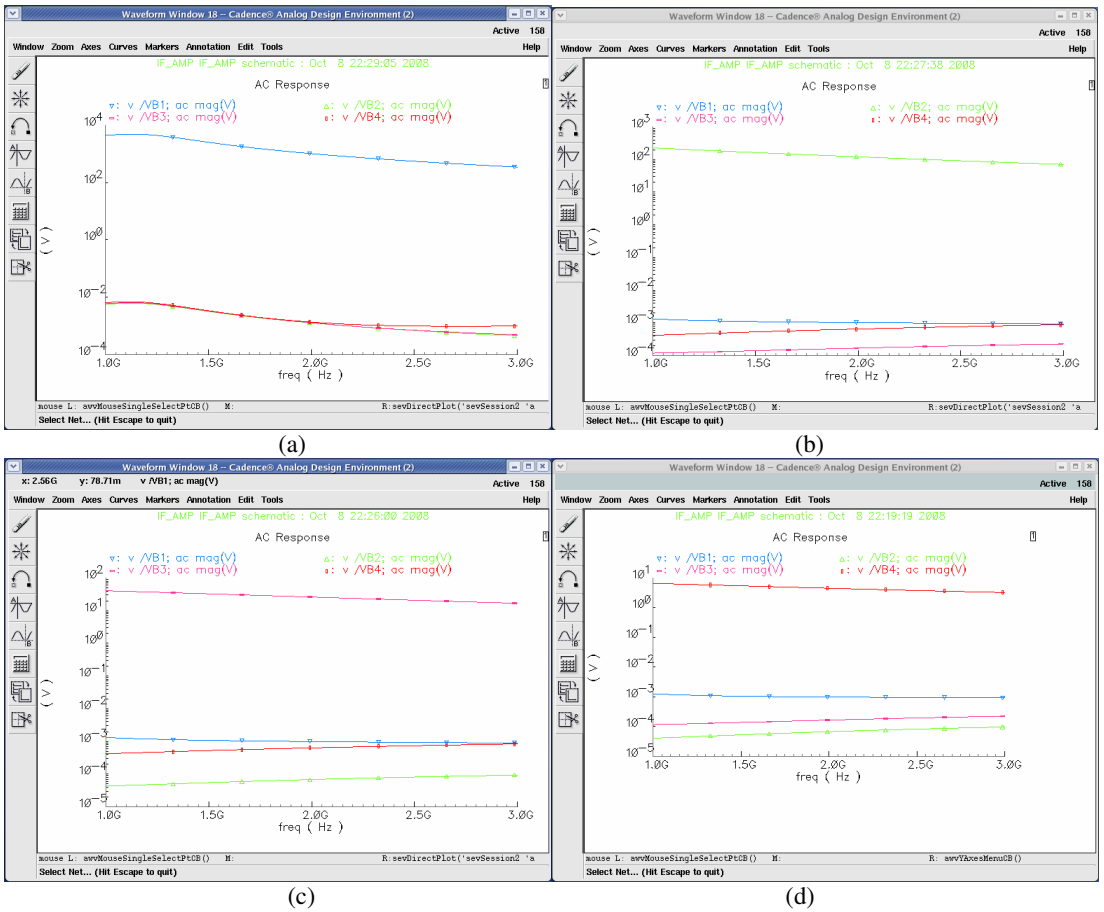


Fig. V-30. Gain of IF amplifier channels when (a) channel I is active, (b) channel II is active, (c) channel III is active and (d) channel IV is active.

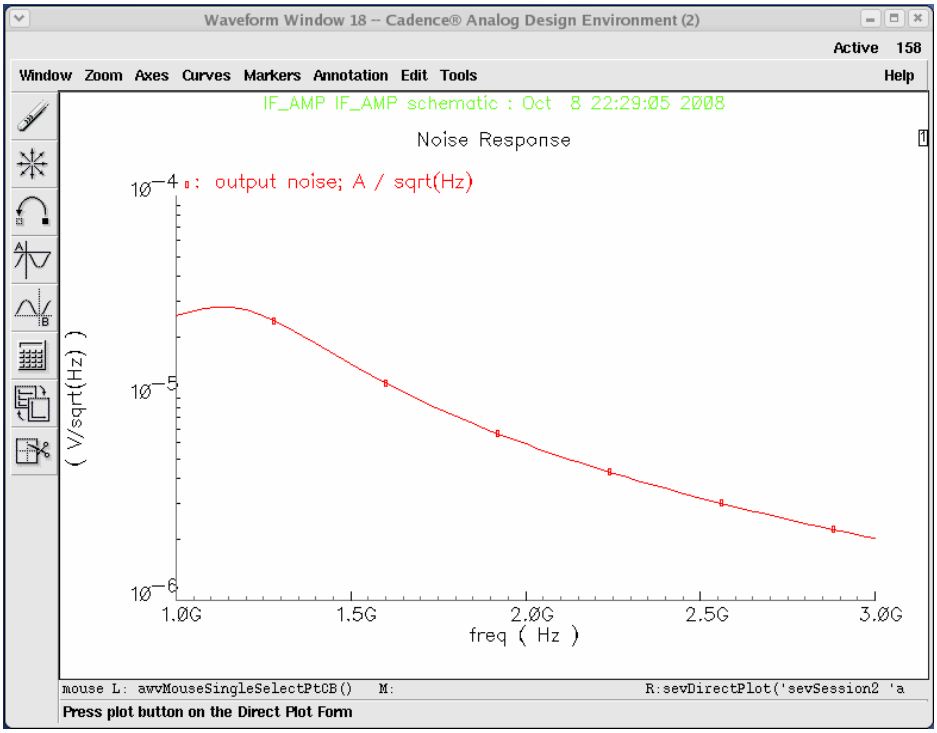


Fig. V-31. The output noise voltage spectral density of the IF amplifier in maximum gain

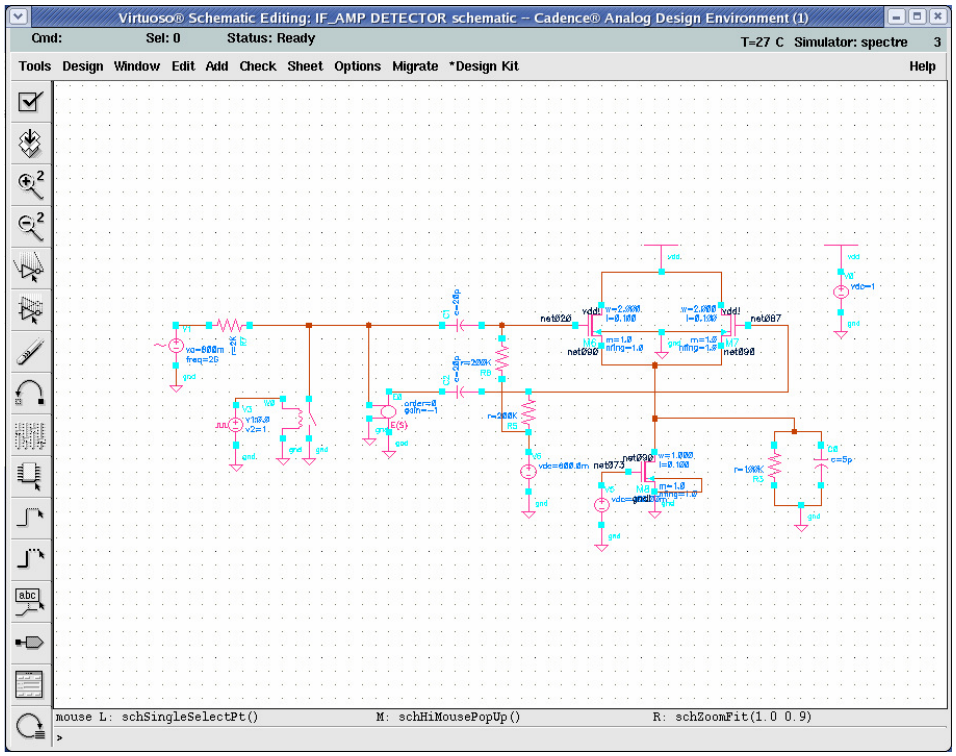


Fig. V-32. The envelope detector circuit schematic

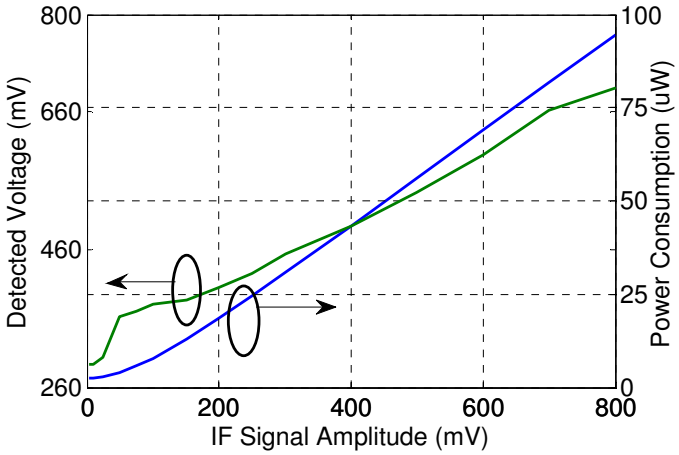


Fig. V-33. voltage transfer curve and power consumption of the designed envelope detector as a function of the IF signal amplitude, simulated using Spectre-RF

V.2.3.4 Receiver Performance Evaluation

We evaluate the designed receiver performance in two ways, analysis and simulation. The performance measure in our work is bit error rate (BER), defined as the ration of the number of erroneous received data bits over total received bits, for enough large number of bits.

A) Receiver Analysis

Analytic equation of BER in OOK modulation in ideal condition, i.e. considering all of the noises as Gaussian white noise, is obtained simply using detection theory, as stated in many text books and literatures, e.g. [116]. The resulted equation is as follows:

$$BER = Q\left(\sqrt{\frac{E_b}{2N_0}}\right) \tag{V-45}$$

Where E_b is the average energy-per-bit and N_0 is the single-sided noise power spectral density. Q is the well-known Q-function, defined as:

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^{\infty} e^{-\frac{\beta^2}{2}} d\beta \tag{V-46}$$

E_b and N_0 are calculated as:

$E_b = P_s \times T_b$

$N_0 = P_n \times BW$

P_s is the signal power, P_n is the signal power, T_b is bit period and BW is the receiver bandwidth. So considering that the receiver bandwidth is equal to inverse of bit period, from (V-45) we deduce:

$$BER = Q\left(\sqrt{\frac{SNR}{2}}\right) \tag{V-47}$$

where SNR is the signal-to-noise ratio. Other useful representation of (V-45) is:

$$BER = Q\left(\sqrt{\frac{P_s}{2N_0T_b}}\right) \tag{V-48}$$

P_s is the received signal power. When N_0 is the noise spectral density at the receiver input, this equation relates BER to the input signal power and is used to fine the receiver sensitivity.

Single-sided noise spectral density in the input of a circuit with noise factor equal to F is calculated as:

$$N_0 = (F-1)kT \qquad V^2/Hz \tag{V-49}$$

T is the ambient temperature and k is Boltzmann constant. In the case of our receiver, using Frees equation we obtain:

$$N_0 = \left(F_{LNA} - 1 + \frac{F_{MIXER} - 1}{G_{LNA}} \right) kT \tag{V-50}$$

We have calculated BER of our receiver, using (V-48) and the results have been plotted in Fig. V-34. This figure shows that with minimum acceptable BER equal to 0.001, the receiver sensitivity is equal to -89, 2dB lower than the predicted value in primary design.

B) Receiver Simulation

To more accurately evaluate the receiver performance, we have simulated it in MATLAB, using IF-Band modeling. Due to high RF frequency, RF-sampling leads to enormous number of samples that can not be manipulated with ordinary PC facilities. So we have modeled the receiver system in IF band, i.e. at 2GHz. Each block of the receiver has been modelled behaviourally and parameters of different blocks have been obtained from accurate simulation of designed circuits in the foundry design kit. Signal source produces random "0" or "1" data with uniform distribution and creates base band signal equivalent to the random data. Then the base band signal is filtered by the pulse shaping filter to limit the base band signal spectrum. Pulse shaping filter is a Square Root Raised Cosine (SRRS) filter with 0.22 roll-off factor. Frequency response of LNA and mixer has modelled using proper filters, to capture the noise power reduction due to the limited bandwidth. IF amplifier has been modelled with gains obtained from simulation, and noise floor of $6\mu V/\sqrt{Hz}$ around 2GHz, as shown in Fig. V-31. The detector has been modelled based on the simulated characteristics of Fig. V-33 and proper low-pass filter.

An example of the simulation results for a 100-bit data stream has been shown in Fig. V-35. The received signal level is -87dBm. Fig. V-36 shows the eye diagram of the received base-band signal, corresponding to the 100-bit data stream. Eye diagram offers an intuitive view of the receiver performance, specially in the measurement time. In addition, using eye diagram one can calculate the required input signal power to achieve the ideal eye opening [105]. BER has been calculated from running the simulator for a 100,000-bit data stream and value of 0.0012 has been obtained with -87dBm received signal power.

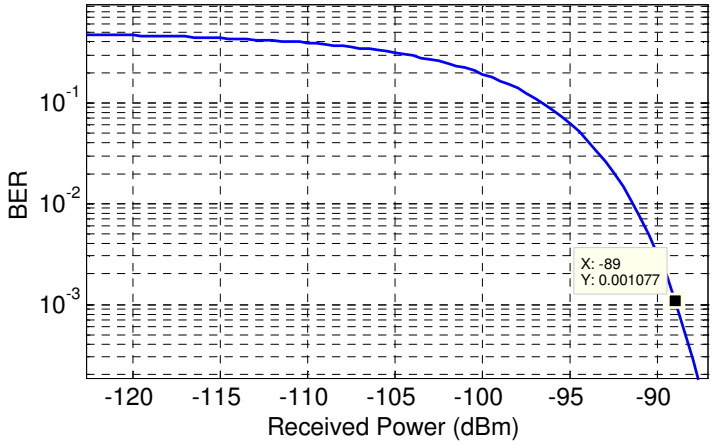


Fig. V-34. BER of our receiver as a function of the received signal power

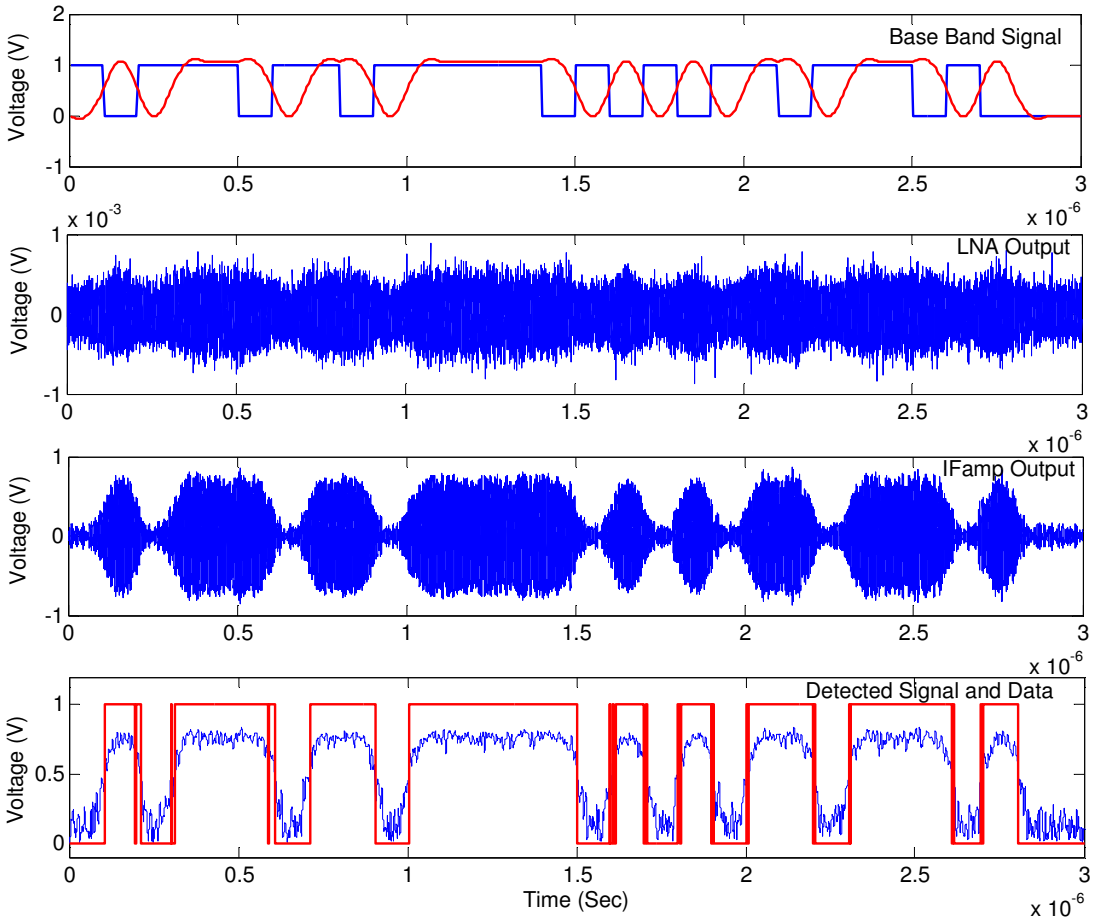


Fig. V-35. An example of the simulation results of the receiver in MATLAB, for a 100-bit data stream and -87dBm received signal level

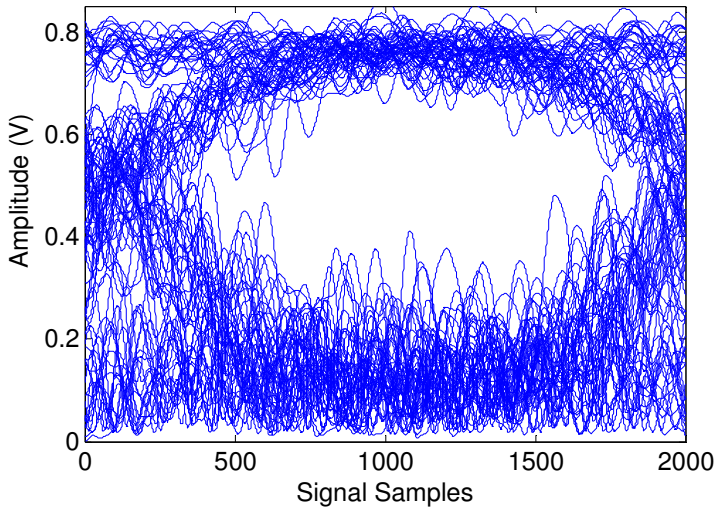


Fig. V-36. Eye diagram of received base band signal, corresponding to a 100-bit data stream

C) Receiver Performance Summary

Summary of the designed receiver and its performance has been listed in Table V-5. All of the receivers and transmitters in Table V-1 and Table V-2 are in the frequencies well below 30GHz and hence can not be compared with our work. Unfortunately we could not find any reported case of Ka band transceiver in CMOS technology. However some reported works are available in 60GHz band, but not for WSN application. We have tabulated the power consumption of these cases in Table V-6. The purpose is only to give an insight to the power consumption of conventional mm-wave transceivers.

TABLE V-5
Summary of Designed Receiver Parameters

	Carrier frequency (GHz)	30		Mixer	Topology	ACEH**
	IF frequency (GHz)	2			RF frequency (GHz)	30
	Modulation	OOK			LO frequency (GHz)	14
	Sensitivity (dBm)	-87			IF frequency (GHz)	2
	Bit Rate (Kb/Sec)	890			Conversion Gain (dB)	4
	DC Power (mW)	6.65			Noise Figure (SSB)	7
LNA	Power Gain (dB)	13.8			DC Power (mW)	2.2
	Noise Figure (dB)	3.6			S11 (dB20)	-12
	DC Power (mW)	3			S22 (dB20)	-25
VCO	Topology	CRCC*		IF amplifier	DC power (mW)	<0.25
	Center frequency (GHz)	14			Voltage Gain I	1000
	Swing (mV)	450			Voltage Gain II	120
	Phase noise @100KHz (dBc/Hz)	-83			Voltage Gain III	26
	DC Power (mW)	1.2			Voltage Gain IV	4.5

CRCC: Current Reused Cross Coupled
ACEH: Active CMOS Even Harmonic

TABLE V-6
Comparison of our Receiver with Reported mm-wave Receivers

Reference	Year	Receiver Topology	Carrier Frequency	DC power (mW)	Technology
[83]	2006	Heterodyne (LNA+Mixer)	60GHz	10.8	130nm CMOS
[117]	2007	Heterodyne	60GHz	77	130nm CMOS
[14]	2007	Heterodyne (LNA + Mixer + LO)	60GHz	80	90nm CMOS
[118]	2008	Heterodyne (IRRM with 30GHz IF, without LO)	60GHz	36	90nm CMOS
This Work	2008	Heterodyne (EHM + LO)	30GHz	6.65	90nm CMOS

V.2.4 The Transmitter Architecture

We tried various reported nonlinear and switching power amplifiers in 30GHz band, e.g. cascode class C, driven directly by VCO [99], pseudo differential class B amplifier [119] and power VCO technique [73]. We also developed a novel design approach for accurate design of Class E power amplifiers [120]. Unfortunately, simulations in the foundry design kit revealed that in 30GHz band forcing the NMOS transistor with enough gate width, into on and off states, requires very high power drive circuit and is not practical for a ultra-low power transmitter. Consequently we excluded the switch mode power amplifiers. On the other hand, other classes of power amplifiers have very low efficiency. Finally we found that the Voltage Controlled Power Oscillator (PVCO) is the best choice for our work. This technique was proposed by Rabaey et *al.* in the Berkeley Wireless Research Center, in 2006 to avoid the DC power required for drive stage of power amplifier, in low power transmitter for WSN applications [73]. In this technique the VCO is designed with enough power to directly feed the antenna, without any power amplifier. One problem with this technique is VCO frequency pulling due to the limited reverse isolation of antenna. To eliminate this problem, they used

an ultra-low power high-Q MEMS oscillator to increase the power oscillator stability by injection locking. In the next generations of their work, they replaced the power oscillator with lower power amplifier, directly matched to the antenna and achieved 46% transmitter efficiency at 1.9GHz [78].

Schematic view of the power VCO circuit in our work has been shown in Fig. V-37. The VCO has been designed as a conventional cross coupled CMOS topology. Using N and P transistors leads higher drive capability. OOK modulation is performed simply using a switch MOS transistor at the tail of NMOS transistors. Simple calculation shows that to deliver 7mW RF power to 50Ω load, voltage swing of 830mV is required. To achieve this high voltage swing, we have used high voltage MOS transistors in the VCO. These transistors are provided by the STMicroelectronics 90nm CMOS technology and have 2.5V gate oxide breakdown voltage. Fig. V-38 shows the time domain wave forms of the transmitter, obtained from simulation in CADENCE using Spectre-RF simulator and the attached foundry design kit. From this figure, the start-up delay of the oscillator is about 2.5nSec that is well beyond the requirements of a low data rate system. The oscillator output is very stable in the startup. Power consumption of the VCO and its phase noise have been shown in Fig. V-39. The VCO has noise phase of -85dBc/Hz at 100KHz offset and consumes 24mW power from 2.5V supply. The RF power delivered to the 50 load is greater than 6mW that corresponds with 25% power efficiency of the transmitter. Regarding Table V-2, 25% power efficiency in 30GHz band is a superior result, if it proven with measurement. Assuming equal probability of transmitted "1" and "0" bits, the average power consumption of the transmitter is 12mW that is in good agreement with which we calculated in the radio link design step of section V.2.1.

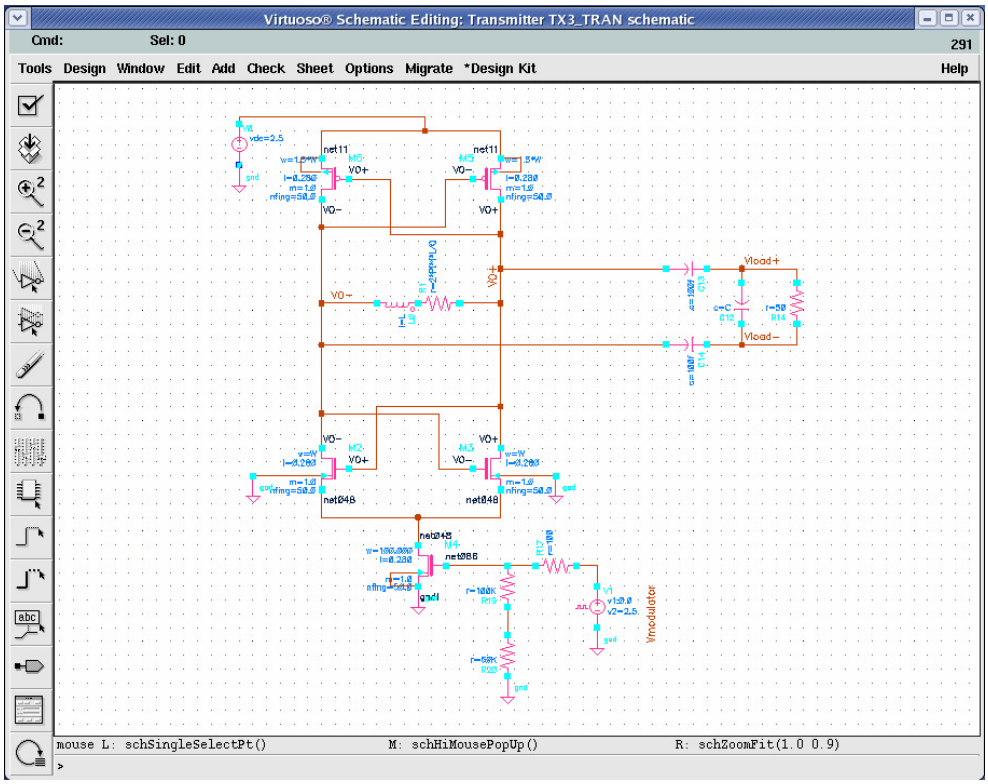


Fig. V-37. Schematic view of the power VCO circuit in our work

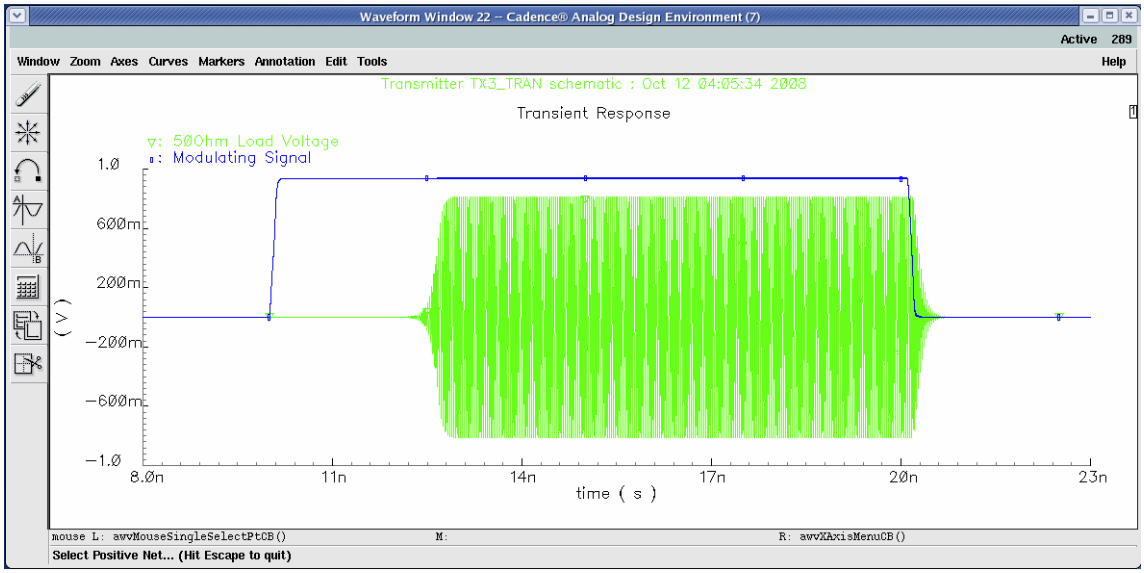
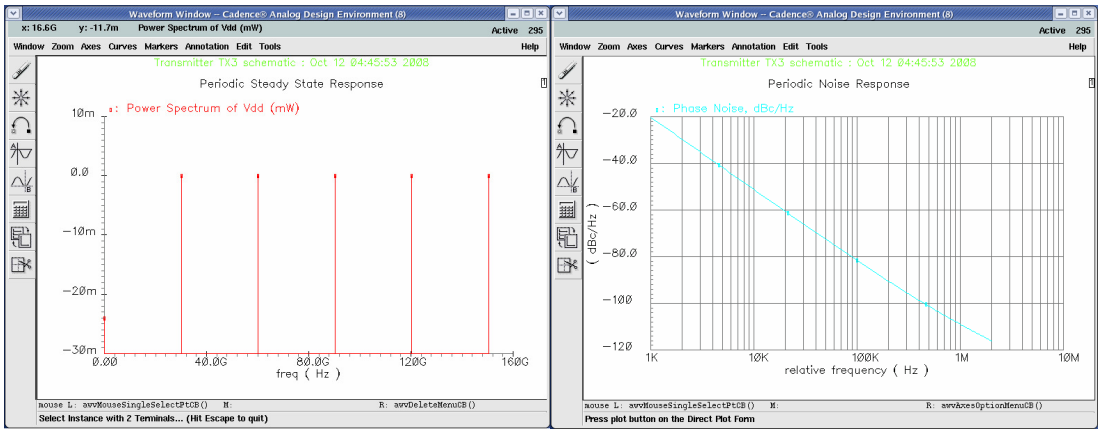


Fig. V-38 Time domain wave forms of the transmitter, obtained from simulation in CADENCE using Spectre-RF simulator and the attached foundry design kit



(a) (b)

Fig. V-39. (a) power consumption and (b) phase noise of the designed power VCO

References

[1] R. Naik, H. P. Le, J. Singh, J. Devlin, "Potential of reconfigurable digital backend in UWB receiver for wireless sensor network," *In proceedings of the IEEE International Conference on Intelligent Sensors, Sensor Networks and Information (ISSNIP 2007),* pp. 215-220, Dec. 2007.

[2] G. M. Maggio, N. Rulkov, L. Reggiani, "Pseudo-chaotic time hopping for UWB impulse radio," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, issue 12, pp. 1424-1435, Dec. 2001.

[3] I. D. O'Donnell, R. W. Brodersen, "An ultra-wideband transceiver architecture for low power, low rate, wireless systems," *IEEE Transactions on Vehicular Technology*, vol. 54, issue 5, pp. 1623-1631, Sept. 2005.

[4] N. Pletcher, S. Gambini, J. Rabaey, "A 65μW, 1.9 GHz RF to digital baseband wakeup receiver for wireless sensor nodes," *IEEE Custom Integrated Circuits Conference (CICC2007)*, pp. 539-542, 2007.

[5] P. Kolinko, L. E. Larson, "Passive rf receiver design for wireless sensor networks," *In proceedings of the IEEE International Symposium on Microwave (MTT-S)*, pp. 567 – 570, June 2007.

[6] Asad **A.** Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 12, pp. 1399-1410, Dec. 1995.

[7] C.-K. Weng, Y.-M Lin, and W. I. Way, "Radio-Over-Fiber 16-QAM, 100-km transmission at 5 Gb/s using DSB-SC transmitter and remote heterodyne detection," *IEEE Journal of Light wave Technology*, vol. 26, Issue 6, pp. 643 – 653, March 2008.

[8] G. Chattopadhyay, "Future of heterodyne receivers at sub-millimeter wavelengths," In proceedings of the The Joint 30th International Conference on Infrared and Millimeter Waves and 13th International Conference on Terahertz Electronics, vol. 2, pp. 461-462, Sept. 2005.

[9] G. P. Timms, J. D. Bunton, M. L. Brothers, J. W. Archer, "190 GHz millimetre-wave imaging using MMIC-based heterodyne receivers," *In proceedings of the 2nd International Conference on Wireless Broadband and Ultra Wideband Communications*, pp. 32-32, Aug. 2007.

[10] H.-W.HÜbers , "Terahertz heterodyne receivers," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 14, Issue 2, pp. 378-391, March-April 2008.

[11] Xiaohui-Li, Ya-Liu, Danni-Wang, Yujing-Bian, "Heterodyne frequency measurement method based on virtual instrument," In proceedings of the IEEE International Frequency Control Symposium, 2007 Joint with the 21st European Frequency and Time Forum. pp. 220-222, May-June 2007.

[12] Tim Denison, Wes Santa, Randy Jensen, Dave Carlson, Gregory Molnar, Al-Thaddeus Avestruz, "An 8uW heterodyning chopper amplifier for direct extraction of 2uVrms neuronal biomarkers," *IEEE International Solid-State Circuits Conference (ISSCC 2008), Digest of Technical Papers*. pp. 162-603, Feb. 2008.

[13] Behzad Razavi, "A Millimeter-wave CMOS heterodyne receiver with on-chip LO and divider," *IEEE Journal of Solid-State Circuits*, vol 43, Issue 2, pp. 477-485, Feb. 2008.

[14] Behzad Razavi, "A mm-wave CMOS heterodyne receiver with on-chip LO and divider," *IEEE International Solid-State Circuits Conference (ISSCC 2007), Digest of Technical Papers*. pp. 188 – 596, Feb. 2007.

[15] Behzad Razavi, "Heterodyne phase locking: a technique for high-frequency division," *IEEE International Solid-State Circuits Conference (ISSCC 2007), Digest of Technical Papers*, pp. 428 – 429, Feb. 2007.

[16] Vincent Peiris, Claude Arm, Stéphane Bories, Stefan Cserveny, Frédéric Giroud, Philippe Graber, Stève Gyger, Erwan Le Roux, Thierry Melly, Michel Moser, Olivier Nys, Franz Pengg, Pierre-David Pfister, Nicolas Raemy, Antoine Ribordy, Pierre-François Ruedi1, David Ruffieux, Lauri Sumanen, Silvio Todeschini2, Patrick Volet1, "A 1 V 433/868 MHz 25 kb/s-FSK 2 kb/s-OOK RF transceiver SoC in standard digital 0.18 /spl mu/m CMOS," *IEEE International Solid-State Circuits Conference (ISSCC 2005),* vol. 1, pp. 258-259Feb. 2005.

[17] E. Mohns, M. Kahmann, "Heterodyne measurement system (HMS) for determining phase angles," *IEEE Transactions on Instrumentation and Measurement*, vol 56, Issue 2, pp.505-508, April 2007.

[18] Hirad Samavati, Hamid R. Rategh, and Thomas H. Lee, "A 5-GHz CMOS wireless LAN receiver front end," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 5, pp. 765-772, May 2000.

[19] A. Baki, M. N. El-Gamal, "RF CMOS fully-integrated heterodyne front-end receivers design technique for 5 GHz applications," *In Proceedings of the International Symposium on Circuits and Systems (ISCAS '04)*, vol. 1, pp I - 960-3, May 2004.

[20] J. J. O. Mitrea, Ocampo-Hidalgo, M. Glesner, "A low-IF architecture for dual-standard GSM/UMTS fully integrated receivers," *In proceedings of the IEEE International Conference on Electronics, Circuits and System (ICECS 2003)* vol. 3, pp. 1101-1104, Dec. 2003.

[21] Ellie Cijvat, Shahrzad Tadjpour, and Asad A. Abidi , "Spurious mixing of Off-channel signals in a wireless receiver and the choice of IF," *IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing*, vol. 49, no. 8, pp. 539-544, Aug. 2002.
[22] Behzad Razavi , "Design considerations for direct-conversion receivers," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 44, no. 6, pp. 428-435, June 1997.
[23] Behzad Razavi, "Heterodyne phase locking: a technique for high-speed frequency division," *IEEE Journal of Solid-State Circuits*, vol. 42, Issue 12, pp. 2887-2892, Dec. 2007.
[24] J. C. Rudell, Paul R. Gray, "A 1.9 GHz wide-band IF double conversion CMOS receiver for cordless telephone applications," *IEEE Journal of Solid State Circuits*, vol. 32, no. 12, pp. 2071-2087, Dec. 1997.
[25] Jan Crols, Michel S. J. Steyaert, "A single-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology," *IEEE Journal of Solid State Circuits*, vol. 30, no. 12, pp. 1483-1492, Dec. 1995.
[26] I. Nam, Choi Kyudon, Lee Joonhee, Hyouk-Kyu Cha, Bo-Ik Seo, K. Kwon, Kwyro Lee, "A 2.4-GHz low-power low-IF receiver and direct-conversion transmitter in 0.18-μm CMOS for IEEE 802.15.4 WPAN applications," *IEEE Transactions on Microwave Theory and Techniques*, vol 55, Issue 4, pp. 682-689, April 2007.
[27] Adrian Maxim, Ramin K. Poorfard, Richard A. Johnson, Philip John Crawley, James T. Kao, Zhiwei Dong, Madhu Chennam, Tim Nutt, David Trager, and Mitchell Reid, "A fully integrated 0.13um CMOS Low-IF DBS satellite tuner using automatic signal-path gain and bandwidth calibration," *IEEE Journal of Solid-State Circuits*, vol. 42, Issue 4, pp. 897-921, April 2007.
[28] Hoesam Jeong, Byoung-Joo Yoo, Cheolkyu Han, Sang-Yoon Lee, Kang-Yoon Lee, Suhwan Kim, Deog-Kyoon Jeong, and Wonchan Kim, "A 0.25um CMOS 1.9-GHz PHS RF transceiver with a 150-kHz Low-IF architecture," *IEEE Journal of Solid-State Circuits*, vol 42, Issue 6, pp. 1318-1327, June 2007.
[29] R. Hartley, "Modulation System," *U.S. Patent 1,666,206*, April 1928.
[30] Donald K. Weaver, "A third method of generation and detection of single-sideband signals," *Proceedings of the IRE*, pp. 1703-1705, 1956.
[31] Available [Online]: http://www.bwrc.eecs.berkeley.edu/Publications/2001/THESES/adapt_calib_meth/Sever_MSThesis.pdf
[32] Behzad Razavi, "*RF Microelectronics*," Upper Saddle River: Prentice Hall, 1998.
[33] Available [Online]: http://rfwireless.rell.com/pdfs/TN_WJmms2.pdf
[34] Wenqing Lu, Shiwei Cheng, Yang Liu, Shengguo Cao, Ke Zhang, Xiaofang Zhou, "A CMOS poly-phase low-IF filter with on-chip frequency control," *In proceedings of the 7th International Conference on ASIC (ASICON '07)*, pp. 680-683, Oct. 2007.
[35] Farbod Behbahani, John C. Leete, Yoji Kishigami, Andreas Roithmeier, Koichi Hoshino, and Asad A. Abidi, "A 2.4-GHz low-IF receiver for wideband WLAN in 0.6-_m CMOS—architecture and front-end," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 12, pp. 1908-1915, Dec. 2000.
[36] A. Gimeno-Martin, J. M. Pardo-Martin, F. J. Ortega-Gonzalez, "Adaptive algorithm for increasing image rejection ratio in low-IF receivers," *Electronics Letters*, vol. 44, Issue 6, pp. 447-448, March 2008.
[37] Gye-Tae Gil, Young-Doo Kim, Y. H. Lee, "Non-data-aided approach to I/Q mismatch compensation in low-IF receivers," *IEEE Transactions on Signal Processing*, vol. 55, Issue 7, pp. 3360-3365, July 2007.
[38] S. Di Pascoli, L. Fanucci, F. Giusti, B. Neri, D. Zito, "Fully integrated heterodyne RF receiver for ISM band applications," *In proceedings of the IEEE International Symposium on Signals, Circuits and Systems (SCS 2003)*, vol. 1, pp. 125-128 , July 2003.
[39] Asad A. Abidi, "Low-power radio-frequency IC's for portable communications, *Proceedings of the IEEE*, vol. 83, no. 4, pp. 544-569, April 1995.
[40] K. W. Hamed, A. P. Freundorfer, Y. M. M. Antar, P. Frank, D. Sawatzky, "A high-bit rate Ka-band direct conversion QPSK demodulator," *IEEE Microwave and Wireless Components Letters*, vol 18, Issue 5, pp. 365-367. May 2008.
[41] Jing-Hong Zhan, B. R. Carlton, S. S. Taylor, "Low-cost direct conversion RF front-ends in deep submicron CMOS," *In proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 203-206, June 2007.
[42] M. Brandolini, M. Sosio, F. Svelto, "A 750 mV fully integrated direct conversion receiver front-end for GSM in 90-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol 42, Issue 6, pp. 1310-1317, June 2007.
[43] Xuemin Yang, A. Davierwalla, D. Mann, K. G. Gard, "A 90nm CMOS direct conversion transmitter for WCDMA," *In proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 17-20, June 2007.
[44] O. Panfiov, R. Hickling, T. Turgeon, "Narrowband interference suppression for direct conversion software radios," *In proceedings of the 2nd IEEE International Design and Test Workshop*, pp. 33-37, Dec. 2007.
[45] Pengfei Zhang, Thai Nguyen, Christopher Lam, Douglas Gambetta, Theerachet Soorapanth, Baohong Cheng, Siegfried Hart, Isaac Sever, Taoufik Bourdi, Andrew (KhongMeng) Tham, and Behzad Razavi, "A

5-GHz direct-conversion CMOS transceiver," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2232-2238, Dec. 2003.

[46] Bing Wang; H.M. Kwon, J. Mittel, "Simple DC removers for digital FM direct-conversion receiver," *In proceedings of the IEEE 49th Vehicular Technology Conference,* , vol.: 2 , pp. 1222-1226, May 1999.

[47] Hsing-Hung Chen, Po-Chiun Huang, Chao-Kai Wen, Jiunn-Tsair Chen, "Adaptive compensation of even-order distortion in direct conversion receivers," *In proceedings of the IEEE 58th Vehicular Technology Conference (VTC 2003-Fall)*, vol. 1, pp. 271-274, Oct. 2003.

[48] W. Namgoong, "Modeling and analysis of nonlinearities and mismatches in AC-coupled direct-conversion receiver," *IEEE Transactions on Wireless Communications,* , vol. 4 , Issue 1, pp.163-173, Jan. 2005.

[49] N. C. Hamilton, "Aspects of direct conversion receiver design," In proceedings of the IEEE International Conference on HF Radio System and Technology, pp. 299-303, 1991.

[50] K. Negus, B. Koupal, J. Wholey, K. Carter, D. Millicker, C. Snapp, and N. Marion, "Highly integrated transmitter RFIC with monolithic narrowband tuning for digital cellular handsets," *IEEE International Solid- State Circuits Conference (ISSCC 1994), Digest of Technical Papers*, pp. 38-39, 1994.

[51] C. Takahashi, R. Fujimoto; *S.* Arai, T. Itakura, T. Ueuo, H. Tsurumi, H. Tanimoto, S. Watanahe, and K. Hirakawa, "A 1.9 GHz Si direct conversion receiver IC for QPSK modulation systems," *International Solid-State Circuits Conference (ISSCC 1995), Digest of Technical Papers,* pp. 138-139, 1995.

[52] A. Loke, F. Ali, "Direct conversion radio for digital mobile phones-design issues, status, and trends," *IEEE Transactions on Microwave Theory and Techniques,* vol. 50 , Issue 11 , pp. 2422-2435Nov. 2002.

[53] J. Min, H.-C. Liu, A. Rofougaran, S. Khorram, H. Samueli and A.A. Abidi , "Low power correlation detector for binary FSK direct conversion receivers," *Electronics Letters,* vol. 31 no. 73, pp. 1030-1031, June 1995.

[54] Asad A. Abidi, "Direct-conversion radio transceivers for digital communications." *IEEE International Solid-State Circuits Conference (ISSCC 1995), Digest of Technical Papers*, pp. 186-364, 1995.

[55] H. Okuni, R. Ito, H. Yoshida, T. Itakura, "A direct conversion receiver with fast-settling DC offset canceller," *In Proceedings of the IEEE 18th International Symposium on Personal, Indoor and Mobile Radio Communications (PIMRC 2007)*, pp. 1-5, Sept. 2007.

[56] Y. Furuta, T. Heima, H. Sato, T. Shimizu, "A low flicker-noise direct conversion mixer in 0.13um CMOS with dual-mode DC offset cancellation circuits," *In Proceedings of the IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 265 – 268, Jan. 2007.

[57] Myung-Woon Hwang, Seung-Yup Yoo, Jeong-Chul Lee, Joonsuk Lee, Gyu-Hyeong Cho, "A high IIP2 direct-conversion mixer using an even-harmonic reduction technique for cellular CDMA/PCS/GPS applications," *In Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium,* pp. 39-42, June 2004.

[58] S.A. Leyonhjelm, M. Faulkner, "Digital signal processing and direct conversion for multi-channel transmitters," *In Proceedings of the IEEE 44th Vehicular Technology Conference*, pp. 494-498, June 1994.

[59] D.S. Hilborn, S.P. Stapleton, J.K. Cavers, "An adaptive direct conversion transmitter," *IEEE Transactions on Vehicular Technology*, vol. 43 , Issue 2 , pp. 223-233, May 1994.

[60] R. Salmeh, B.J. Maundy, R.H. Johnston, "Design issues of direct conversion radio frequency receivers in SiGe technology," *In Proceedings of the Canadian Conference on Electrical and Computer Engineering,* vol. 1, pp. 61-64, May 2004.

[61] B. Matinpour, S. Chakraborty, J. Laskar, "Novel DC-offset cancellation techniques for even-harmonic direct conversion receivers," *IEEE Transactions on Microwave Theory and Techniques,* , vol. 48 , Issue 12, pp. 2554-2559, Dec. 2000.

[62] J. H. Lee, . K. Han, S. S. Ahn, S. H. Lee, H. D. Kim, "A low phase noise octa-phase LC VCO for multi-band direct conversion receiver," *In Proceedings of the IEEE International Conference on Electro magnetic in Advanced Applications (ICEAA 2007)*, pp. 411-414, Sept. 2007.

[63] Won Namgoong, T.H. Meng, "Direct-conversion RF receiver design," *IEEE Transactions on Communications*, vol. 49, Issue 3, pp. 518-529, March 2001.

[64] N. J. Oh, "Corrections to A low-power CMOS direct conversion receiver with 3-dB NF and 30-kHz flicker-noise corner for 915-MHz band IEEE 802.15.4 ZigBee standard," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, Issue 6, pp. 1256-1256, June 2007.

[65] S. Paschalis, K. Eleni-Sotiria, B. Antonios, P. Yannis, "Design and implementation of a 1-V low flicker noise direct conversion mixer at 5.5 GHz using a 90nm CMOS RF technology," *In Proceedings of the 14th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2007)*, pp. 605-608, Dec. 2007.

[66] E. Edwin, Bautista, Babak Bastani, and Joseph Heck, "A High IIP2 down-conversion mixer using dynamic matching," *IEEE Journal of Solid State Circuits*, vol. 35,no. 12, pp. 1934-1941, Dec. 2000.

[67] A. Cantoni, J. Tuthill, "Digital compensation of frequency dependent imperfections in direct conversion I-Q modulators," *In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS 2007)*, pp. 269- 272, May 2007.

[68] Young-wan Kim, "Spurious signal rejection using real-time imbalance compensation in direct conversion transmitter," *IEEE Communications Letters*, vol. 11, Issue 6, pp. 477-479, June 2007.

[69] H. Darabi, "A 2.4 GHz CMOS transceiver for Bluetooth," IEEE International Solid-State Circuits Conference (ISSCC 2001), Digest of Technical Papers, pp. 200-201, Feb. 2001.

[70] Ji-Hoon Kim, Hyung-Joun Yoo, "Low power octa-phase LC VCO for direct conversion 5 GHz WLAN receiver, " *In Proceedings of the IEEE Asia-Pacific Microwave Conference (APMC 2005)*, vol. 5, pp.4-7, Dec. 2005.

[71] Denis C. Daly, Anantha P. Chandrakasan , "An energy-efficient OOK transceiver for wireless sensor networks," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 1003-1011, May 2007.

[72] B. Otis, Y.H. Chee, J. Rabaey , "A 400μW-RX, 1.6mW-TX super- regenerative transceiver for wireless sensor networks," *IEEE International Solid-State Circuits Conference (ISSCC 2005), Digest of Technical papers,* pp. 396-606, Feb. 2005.

[73] Y. H. Chee, A. M. Niknejad, J. M. Rabaey, "An ultra-low-power injection locked transmitter for wireless sensor networks," *IEEE Journal of Solid-State Circuits*, vol. 41, issue 8, pp. 1740-1748, Aug. 2006.

[74] Bo Yang, S. Salter Thomas, Neil Goldsman, "A physically designed 2.2 GHz OOK receiver for minimum power wireless sensor network applications," *In Proceedings of the International Semiconductor Device Research Symposium*, pp. 1-2, Dec. 2007.

[75] B.P. Otis, Y.H. Chee, R. Lu, N.M. Pletcher, J.M. Rabaey , "An ultra-low power MEMS-based two-channel transceiver for wireless sensor networks," *In Proceedings of the IEEE International Symposium On VLSI Circuits, Digest of Technical Papers*, pp. 20-23, 2004.

[76] T. Song, H. -S. Oh, E. Yoon, S. Hong, "A low-power 2.4-GHz current-reused receiver front-end and frequency source for wireless sensor network," *IEEE Journal of Solid-State Circuits*, vol. 42, issue 5, pp. 1012-1022, May 2007.

[77] A. Molnar, B.n Lu, S. Lanzisera, Ben W. Cook and K. S. J. Pister, "An ultra-low power 900 MHz RF transceiver for wireless sensor networks," *In Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 401-404, 2004.

[78] Y. H. Chee, A. M. Niknejad, J. Rabaey, "A 46% efficient 0.8dBm transmitter for wireless sensor networks," *In Proceedings of the IEEE Symposium on VLSI Circuits*, pp. 43-44, 2006.

[79] Byung-Sung Kim, Moon-Que Lee, Sangwook Nam, Jiho Ryu, Minchul Kim, and Jaechun Lee, "Low power OOK transmitter for wireless capsule endoscope," *In Proceedings of the IEEE International Microwave Symposium (MTT-S2007)*, pp. 855-858, June 2007.

[80] Chen Wenjian; T. Copani, H. J. Barnaby, S. Kiaei, "A 0.13-/spl mu/m CMOS ultra-low power front-end receiver for wireless sensor networks," *In Proceedings of IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 105-108, June 2007.

[81] Taeksang Song, Hyoung-Seok Oh, Sang-Hyun Baek, Songcheo Hong, and Euisik Yoon, "A 2.4-GHz sub-mW CMOS current-reused receiver front-end for wireless sensor network," *In Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, June 2006.

[82] Yu-Tso Lin, Tao Wang, Shey-Shi Lu, Guo-Wei Huang, "A 0.5 V 3.1 mW fully monolithic OOK receiver for wireless local area sensor network," *In Proceedings of the Asian Solid-State Circuits Conference*, pp. 373-376, Nov. 2005.

[83] Behzad Razavi, "A 60-GHz CMOS Receiver Front-End," *IEEE Journal of Solid State Circuits*, vol. 41, no. 1, pp. 17-22, Jan. 2006.

[84] S. E. Gunnarsson, "Analysis and design of a novel 4-times sub-harmonically pumped resistive HEMT mixer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, Issue 4, pp. 809-816, April 2008.

[85] Jan M. Rabaey, J. Ammer, T. Karalar, S. Li, Brian Otis, M. Sheets, T. Tuan1, "Pico-Radios for wireless sensor networks: the next challenge in ultra-low power design," *IEEE International Solid-State Circuits Conference (ISSCC 2002), Digest of Technical papers*, Feb. 2002.

[86] Q. Tang, L. Yang, G. B. Giannakis, T. Qin, "Battery power efficiency of PPM and FSK in wireless sensor networks," *IEEE Transactions on Wireless Communications*, vol. 6, issue 4, pp. 1308-1319, April 2007.

[87] Qu Fengzhong, Yang Liuqing, A. Swami, "Battery power efficiency of PPM and OOK in wireless sensor networks," *In proceedings of the IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP 2007)*, vol. 3, pp. III-525-III-528, April 2007.

[88] M. D. Scott, B. F. Boser, K. S. J. Pister, "An ultra low-energy ADC for Smart Dust," *IEEE Journal of Solid-State Circuits*, vol. 38, issue 7, pp. 1123-1129, July 2003.

[89] B. A. Warneke, M. D. Scott, B. S. Leibowitz, Lixia Zhou; C. L. Bellew, J. A. Chediak, J. M. Kahn, B. E. Boser, K. S. J. Pister, "An autonomous 16 mm/sup 3/ solar-powered node for distributed wireless sensor networks," *Proceedings of IEEE, Sensors*, 2002.

[90] H. Barthelemy, S. Bourdel, J. Gaubert, S. Meillere, "OOK/NCP-FSK modulator based on coupled open-closed-loop VCOs," *In Proceedings of the 18th European Conference on Circuit Theory and Design (ECCTD 2007)*, pp. 380-383, Aug. 2007.

[91] J. Zhao, C. Maxey, A. Narayanan, S. Raman, "A SiGe BiCMOS ultra wide band RFIC transmitter design for wireless sensor networks," *In Proceedings of the IEEE Radio and Wireless Conference*, pp. 215-218, Sept. 2004.

[92] Dennis Roddy, "*Microwave technology*," Englewood, New Jersey, Prentice Hall, 1986.

[93] Sébastien Montusclat, Fréderic Gianesello, Daniel Gloria, "Silicon full integrated LNA, filter and antenna system beyond 40 GHz for MMW wireless communication links in advanced CMOS technologies," *In Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, June 2006.

[94] Fawwaz T. Ulaby, Richard K. Moore, Adrian K. Fung, "*Microwave remote sensing: active and passive*," Volume I, Norwood, Artech House, 1981.

[95] Ming-Feng Huang, Shuenn-Yuh Lee, and Chung J. Kuo, "A CMOS even harmonic mixer with current reuse for low power applications," *In Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED'04)*, pp. 290-295, 2004.

[96] Shuenn-Yuh Lee, Ming-Feng HuangC. J. Kuo, "Analysis and implementation of a CMOS even harmonic mixer with current reuse for heterodyne/direct conversion receivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol 52, Issue 9, pp. 1741-1751, Sept. 2005.

[97] Chun-Lin Kuo, Che-Chung Kuo, Chun-Hsien Lien, Jeng-Han Tsai, Huei Wang, "A novel reduced-size rat-race broadside coupler and its application for CMOS distributed sub harmonic mixer," *IEEE Microwave and Wireless Components Letters*, vol. 18, Issue 3, pp. 194-196, March 2008.

[98] Hung-Ju Wei, Chinchun Meng, Po-Yi Wu, Kuan-Chang Tsung, "K-band CMOS sub-harmonic resistive mixer with a miniature marchand balun on lossy silicon substrate," *IEEE Microwave and Wireless Components Letters*, vol. 18, Issue 1, pp. 40-42, Jan. 2008.

[99] B.W. Cook, A. D. Berny, A. Molnar, S. Lanzisera, K. S. J. Pister, "An ultra-low power 2.4GHz RF transceiver for wireless sensor networks in 0.13/spl mu/m CMOS with 400mV supply and an integrated passive RX front-end," *IEEE International Solid-State Circuits Conference (ISSCC 2006), Digest of Technical Papers,* pp. 1460-1469, Feb. 2006.

[100] D.Y. Jung, C.S. Park, "Power efficient Ka-band low phase noise VCO in 0.13 μm CMOS," *Electronics Letters,* vol. 44, Issue 10, pp. 630-631, May 8 2008.

[101] T. -H. Huang, J. -J. Hsueh, "5-GHz low phase-noise CMOS VCO integrated with a micro-machined switchable differential inductor," *IEEE Microwave and Wireless Components Letters*, vol. 18, Issue 5, pp. 338-340, May 2008.

[102] S. Shekhar, J. S. Walling, S. Aniruddhan, D. J. Allstot, "CMOS VCO and LNA using tuned-input tuned-output circuits," *IEEE Journal of Solid-State Circuits*, vol. 43, Issue 5, pp. 1177-1186, May 2008.

[103] P. Upadhyaya, M. Rajashekharaiah, D. Heo, D. M. Rector, Yi-Jan Emery Chen, "100 Mbs OOK transmitter with low power and low phase noise LC VCO for neurosensory application," *In Proceedings of the IEEE Southeast Conference*, pp. 75-78, April 2005.

[104] P. Upadhyaya, M. Rajashekharaiah, D. Heo, D. M. Rector, Yi-Jan Emery Chen, "Low power and low phase noise 5.7 GHz LC VCO in OOK transmitter for neurosensory application," *In Proceedings of the IEEE International Microwave Symposium (MTT-S2005)*, June 2005.

[105] C. -S. Li, F. F. -K. Tong, K. Liu, D. G. Messerschmitt, "Channel capacity optimization of chirp-limited dense WDM/WDMA systems using OOK/FSK modulation and optical filters," *IEEE Journal of Light wave Technology*, vol. 10, Issue 8, pp. 1148-1161, Aug. 1992.

[106] Y. H. Chee, A. M. Niknejad, and J. Rabaey, "A sub-100 _W 1.9 GHz CMOS oscillator using FBAR resonator," *In Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 123-126, Jun. 2004.

[107] Kenneth K. Clarke Donald T. Hess, "*Communication circuits: Analysis and design*," Addison-Wesley Publishing Company, 1971.

[108] B. R. Jackson, C. F. Saavedra, "A CMOS Ku-band 4x subharmonic mixer," *IEEE Journal of Solid-State Circuits*, vol. 43, Issue 6, pp. 1351-1359, June 2008.

[109] R. M. Kodkani, L. E. Larson, "A 24-GHz CMOS passive subharmonic mixer/downconverter for zero-IF applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, Issue 5, pp. 1247-1256, May 2008.

[110] Juo-Jung Hung, T. M. Hancock, G. M. Rebeiz, "A 77 GHz SiGe sub-harmonic balanced mixer," *IEEE Journal of Solid-State Circuits*, vol. 40, Issue 11, pp. 2167-2173, Nov. 2005.

[111] J. -A. Hou, Y. -H. Wang, "A Ka band balanced third LO-harmonic mixer using a lumped-elements quadrature hybrid," *IEEE Microwave and Wireless Components Letters*, vol. 18, Issue 6, pp. 404-406, June 2008.
[112] Sining Zhou, M. -C. F . Chang, "A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver," *IEEE Journal of Solid-State Circuits*, vol. 40, Issue 5, pp. 1084-1093, May 2005.
[113] F. Ellinger, "26–34 GHz CMOS mixer," *Electron Letters*, vol. 40, no. 22, pp. 1417-1419, Oct. 2004.
[114] Jeng-Han Tsai, Pei-Si Wu, Chin-Shen Lin, Tian-Wei Huang, J. G. J. Chern, Wen-Chu Huang, "A 25–75 GHz broadband Gilbert-cell mixer using 90-nm CMOS technology," *IEEE Microwave and Wireless Components Letters*, vol 17, Issue 4, pp. 247-249, April 2007.
[115] Hsieh-Hung Hsieh, Liang-Hung Lu, and Chung-Ru Wu, "An ultra-wideband distributed active mixer MMIC in 0.18-µm CMOS technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, Issue 4, pp. 625-632, April 2007.
[116] M. D. Audeh, J. M. Kahn, "Performance evaluation of baseband OOK for wireless indoor infrared LAN's operating at 100 Mb/s," *IEEE Transactions on Communications*, vol. 43, Issue 6, pp. 2085-2094, June 1995.
[117] S. Emami, C. H. Doan, A. M. Niknejad and R. W Brodersen, "A highly integrated 60GHz CMOS front-end receiver," *IEEE International Solid-State Circuits Conference (ISSCC 2007), Digest of Technical Papers*, pp. 190-191, Feb. 2007.
[118] Ali Parsa, Behzad Razavi, "A 606Hz CMOS receiver using a 30GHz LO," *IEEE International Solid-State Circuits Conference (ISSCC 2008), Digest of Technical Papers*, pp. 190-606, Feb 2008.
[119] T. Melly, A. -S. Porret, C. C. Enz, E. A. Vittoz, "An ultralow-power UHF transceiver integrated in a standard digital CMOS process: transmitter," *IEEE Journal of Solid-State Circuits*, vol. 36, Issue 3, pp. 467-472, March 2001.
[120] Javad Yavand Hasani, Mahmoud Kamarei, "Analysis and optimum design of a class E RF power amplifier," *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 55, no. 6, pp. 1759-1768, July 2008.