Optimized Design of Stationary Frame Three Phase AC Current Regulators

D. G. Holmes, T. A. Lipo, B. P. McGrath, and W. Y. Kong

(Invited Paper)

***Abstract*—Current regulation plays an important role in modern power electronic ac conversion systems. The most direct strategy to regulate such currents is to use a simple closed loop proportional-integral (PI) regulator, which has no theoretical stability limits as the proportional and integral gains are increased, since it is only a second order system. However, pulsewidth modulation (PWM) transport and controller sampling delays limit the gain values that can be achieved in practical systems. Taking these limitations into account, this paper presents an analytical method to determine the best possible gains that can be achieved for any class of practical linear ac current controller. The analysis shows that the maximum possible proportional gain is determined by the plant series inductance, the dc bus voltage and the transport and sampling delays, while the maximum possible integral gain is determined primarily by the transport and sampling delays. The work is applicable to stationary frame PI regulators, stationary frame controllers with back electromotive force compensation, stationary frame P+resonant (PR) controllers, and synchronous *d–q* frame controllers, since they all have identical proportional and integral gains that must be optimized for any particular application.**

***Index Terms*—Back electromotive force (EMF) compensation, current regulation, feed forward, P+resonant (PR), proportional integral (PI), stationary frame, synchronous *d–q* frame.**

I. Introduction

CURRENT regulation plays a key role in modern power electronic ac conversion systems such as variable speed drive systems, reactive power controllers and active filter systems [1], [2]. High performance drive systems, for example, require control strategies which directly command motor currents rather than just specifying motor terminal voltages, since precise control of motor currents is a mandatory prerequisite for accurate torque and speed control [3], [4]. For uninterruptible power supplies [5], high bandwidth current control is essential to achieve good dynamic response, when the system supplies nonlinear loads such as diode rectifiers, while for grid connected systems [2], accurate current control is important to effectively regulate real and reactive power flow between the grid and the inverter. However, irrespective of the application, the essential concept of a current regulator is always to compare a measured load current against a reference target, and use the difference ("error") between these two quantities to adjust the switching of the associated power electronic converter so as to minimize this tracking error. Specifically, the primary goals of a current regulator can be summarized as [6], [7]:

1) minimize the steady-state magnitude and phase error, preferably achieving zero steady-state error;
2) accurately track the commanded reference current during transient changes. This requires a control system with as high a bandwidth as possible, to achieve the best possible dynamic response;
3) limit the peak current, to avoid overload conditions;
4) minimize low order harmonics in the load current, and compensate for dc-link voltage ripple, deadtime delays, semiconductor device voltage drops and other practical second order effects associated with the inverter operation.

Achieving these goals, particularly for ac current regulators, has proved to be very challenging problem for several decades, and has been the subject of substantial research effort throughout this period [2], [6], [7].

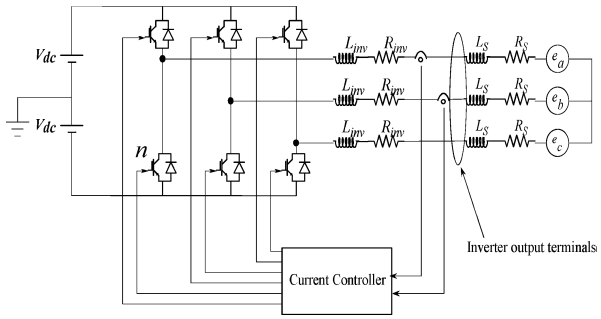

Fig. 1. Current regulated three-phase VSI connected to a back EMF type load (induction motor) through a series impedance.

Fig. 1 shows the essential structure of a current regulated three phase ac system, driven from a standard dc–ac voltage source inverter (VSI) into an induction motor load [12]. While simple, this structure is a very effective representation of the vast majority of ac current regulated applications [7]. For the current regulator itself, there are two major alternative approaches in common use, as follows.

Nonlinear current regulators use the instantaneous current error to directly control the VSI switching states, by explicitly switching the converter phase legs as the current error(s) exceed predefined "hysteresis" boundaries that are located around the target reference. This class of controller has the advantage of

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implicit peak current regulation, very rapid dynamic response, and direct compensation for second order inverter distortion effects, but it can have a highly variable switching frequency and must be matched to any particular load system. Many variations of this strategy have been proposed over the years to improve its performance in a multitude of ways [7], [11].

Linear current regulators operate by calculating the low-frequency averaged voltage that minimizes the current error, and then commanding a VSI modulator to implement this voltage over the pulsewidth modulation (PWM) switching period as an equivalent volt-second switched waveform. This process decouples the error correction and the inverter modulation functions. However, it is important for this class of controller that the PWM switching current ripple is not included in the measured current error using techniques such as synchronous sampling, to achieve optimum performance. The most well known of these strategies are the stationary frame proportional-integral (PI) [7], stationary frame P+resonant (PR) [9], synchronous *d–q* frame [6] controllers, and predictive deadbeat controllers [15]. The focus of this paper is this second class of current regulator.

For the simple first-order type system shown in Fig. 1, classical linear control theory suggests that simple PI control should be quite effective as a regulator, with the proportional action managing the high frequency system response and the integral control minimizing the steady-state error. In fact, these systems do achieve excellent dc current control, with minimal steady-state error because of the (almost) infinite dc gain provided by the integral control action. However, in contrast their ac current control performance is generally unsatisfactory [8], because the PI controller gains cannot be set high enough to avoid a delayed tracking response, with a consequential steady-state error [9]. The usual strategy to solve this limitation is to transform the current regulation process into the synchronous *d–q* rotating frame for a three-phase system [6], or use a PR controller as a stationary frame equivalent [9], although in principle it is not immediately obvious why a simple PI controller is not an adequate solution. Simple linear analysis identifies a PI regulated system as second order with no theoretical stability limits as the gains are increased. However, since it is well established that system instability inevitably eventually occurs as the PI gains are increased [12], clearly the PI gains of practical systems must be limited by second order effects. But identification of these effects, and hence identification of the boundaries of the practical achievable response of a simple PI controller for ac current regulation, have to date not been well reported in the literature.

This paper presents an analytical basis to optimally design the gains of practical closed loop ac current regulators. It identifies PWM transport and digital sampling delay as the main second order factors that limit these gains, and shows how these limitations influence both reference tracking and back electromotive force (EMF) disturbance errors. From this understanding, back EMF feed forward compensation is proposed as a way in many cases of achieving satisfactory stationary frame PI regulator performance without requiring the use of more advanced regulation strategies. The outcome of the work allows a considered design choice to be made as to whether a simple stationary frame PI regulator or a more sophisticated current regulation concept should be used to achieve a particular level of performance for any specific application.

II. AC Current Regulation Using an Idealized Stationary Frame PI Regulator

A well-established strategy to simplify the analysis of a power electronic conversion system is to replace the power stage with a linear amplifier that produces the same output as the commanded volt-second average of the switched output over each PWM (half) period [7]. With this simplification, the voltages across the three phases of the motor load shown in Fig. 1 can be written as

$$\begin{aligned}\hat{v}_{as} &= \hat{v}_{an} - \hat{v}_{sn} \\ &= R_s i_a + L_l \frac{di_a}{dt} + \frac{L_m}{L_m + L_{lr}} \frac{d}{dt}\lambda_{ar} = R_s i_a + L_l \frac{di_a}{dt} + e_{as}\end{aligned} \tag{1}$$

$$\begin{aligned}\hat{v}_{bs} &= \hat{v}_{bn} - \hat{v}_{sn} \\ &= R_s i_b + L_l \frac{di_b}{dt} + \frac{L_m}{L_m + L_{lr}} \frac{d}{dt}\lambda_{br} = R_s i_b + L_l \frac{di_b}{dt} + e_{bs}\end{aligned} \tag{2}$$

$$\begin{aligned}\hat{v}_{cs} &= \hat{v}_{cn} - \hat{v}_{sn} \\ &= R_s i_c + L_l \frac{di_c}{dt} + \frac{L_m}{L_m + L_{lr}} \frac{d}{dt}\lambda_{cr} = R_s i_c + L_l \frac{di_c}{dt} + e_{cs}\end{aligned} \tag{3}$$

where $\hat{v}$ represents the average value of the switched voltage v over a half carrier period, "*s*" is the neutral point of the motor "stator" windings, "*n*" is the dc bus center point (i.e., the inverter "neutral" point), L_l is the machine "transient" inductance, given by

$$L_l = L_{ls} + \frac{L_{lr} L_m}{L_{lr} + L_m} \tag{4}$$

with $L_{ls}, L_{lr},$ and L_m being the stator leakage, rotor leakage, and magnetizing inductances, respectively, and e_{xs} is the back EMF of phase "*x*" created by the rotating rotor flux linkages, defined by

$$e_{xs} = \frac{L_m}{L_m + L_{lr}} \frac{d}{dt}\lambda_{xr}. \tag{5}$$

Equations (1)–(3) are coupled by $\hat{v}_{sn}$, which appears in all three equations. Summing these equations gives

$$\begin{aligned}\hat{v}_{an} + \hat{v}_{bn} + \hat{v}_{cn} - 3\hat{v}_{sn} &= R_s(i_a + i_b + i_c) \\ &+ L_l \frac{d}{dt}(i_a + i_b + i_c) + \frac{L_m}{L_{lr} + L_m} \frac{d}{dt}(\lambda_{ar} + \lambda_{br} + \lambda_{cr}).\end{aligned} \tag{6}$$

For a three wire system $i_a + i_b + i_c = 0$. Furthermore, by Gauss' Law the total rotor flux linking to the stator also equals zero, so that $\lambda_{ar} + \lambda_{br} + \lambda_{cr} = 0$. Hence (6) reduces to

$$\hat{v}_{sn} = \frac{1}{3}(\hat{v}_{an} + \hat{v}_{bn} + \hat{v}_{cn}). \tag{7}$$

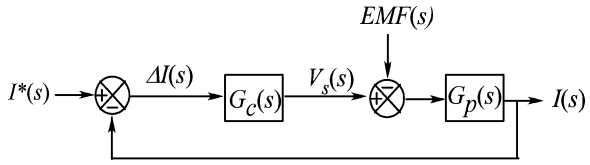

Fig. 2. Average value model block diagram representation of Fig. 1.

If the sum of the commanded average inverter voltages $\hat{v}_{an} + \hat{v}_{bn} + \hat{v}_{cn}$ equals zero, substituting (7) into (1) gives

$$\hat{v}_{as} = \hat{v}_{an} = R_s i_a + L_l \frac{di_a}{dt} + e_{as} \tag{8}$$

which is an independent current regulator for phase "*a*" only. Clearly, a similar result can be obtained for phases "*b*" and "*c*" under the same voltage summation constraint. Hence, any two of the three phase currents can be independently regulated provided that the commanded third phase voltage for the inverter is made equal to the negative of the sum of the two controlled phase voltages for each PWM average (typically half carrier) period, i.e., for example $\hat{v}_{cn} = -(\hat{v}_{an} + \hat{v}_{bn})$.

It should be noted that this control constraint is independent of any common mode voltage that may be added to the PWM commanded voltage references after the control loop calculation, to either increase the inverter voltage headroom, using third harmonic injection or a space vector offset component, or to achieve some other PWM harmonic advantage, such as offered by discontinuous PWM.

The plant transfer function for this system is found by taking the Laplace transform of (8), to give

$$G_p(s) = \frac{1}{R}\left(\frac{1}{1 + sT_p}\right) \tag{9}$$

where $T_p = L/R$, and *R* and *L* include both the load resistance R_s and load inductance L_l, and the resistance and inductance of the converter switches and feeder cables to the motor (respectively). Fig. 2 shows the resulting closed loop regulator for each independent controlled current, where $I^*(s)$ is the commanded current input, $\Delta I(s)$ is the current error, $V_s(s)$ is the "average" commanded voltage fed to the PWM modulator and *I*(*s*) is the regulated current output. Note that the $V_{\rm dc}$ gain provided by the PWM modulator has been integrated into the controller block function $G_c(s)$, and the load back EMF effect has been modeled as a disturbance input EMF(*s*).

The overall closed loop transfer function for this system is given by

$$I(s) = I^*(s)\frac{G_c(s)G_p(s)}{1 + G_c(s)G_p(s)} - \mathrm{EMF}(s)\frac{G_p(s)}{1 + G_c(s)G_p(s)} \tag{10}$$

where the function of the controller $G_c(s)$ is to match the output *I*(*s*) to the commanded input $I^*(s)$ as closely as possible, while minimizing any error caused by the back EMF disturbance. In principle, this is achieved by making the gain of the forward controller block $G_c(s)$ as large as possible, since the plant transfer block $G_p(s)$ is defined by the primary plant equipment and is generally unchangeable for any particular application.

It is instructive to develop a transfer function for the current error $\Delta I(s)$ as a function of the control and disturbance inputs. This can be readily developed as

$$\Delta I(s) = \frac{I^*(s) + \mathrm{EMF}(s)G_p(s)}{1 + G_c(s)G_p(s)} = \Delta I_I(s) + \Delta I_D(s). \tag{11}$$

This transfer function has two elements-–a *closed loop tracking error* sensitivity given by

$$E_I(s) = \frac{\Delta I_I(s)}{I^*(s)} = \frac{1}{1 + G_c(s)G_p(s)} \tag{12}$$

which identifies the ability of the plant to follow the commanded current reference, and a *closed loop disturbance rejection error* sensitivity given by

$$E_D(s) = \frac{\Delta I_D(s)}{\mathrm{EMF}(s)} = \frac{G_p(s)}{1 + G_c(s)G_p(s)} \tag{13}$$

which identifies the plant sensitivity to a back EMF disturbance. The ratio of disturbance to tracking error sensitivity is given by

$$\frac{E_D(s)}{E_I(s)} = \frac{I^*(s)}{\mathrm{EMF}(s)} = G_p(s) = \frac{1}{R}\left(\frac{1}{1 + sT_p}\right) \tag{14}$$

which is independent of the controller block $G_c(s)$, and depends only on the plant load resistance *R* and the plant operating frequency (i.e., disturbance error falls away compared to tracking error as the reference frequency increases above the plant time constant T_p). To achieve minimal overall steady-state error, both $E_I(s)$ and $E_D(s)$ need to approach zero, which for a given plant requires the magnitude of the controller function $G_c(s)$ to be made as large as possible.

The forward transfer block $G_c(s)$ for a simple PI controller is defined by

$$G_c(s) = k_p V_{\rm dc}\left(1 + \frac{1}{s\tau_i}\right) \tag{15}$$

where k_p is the proportional gain, and τ_i is the reciprocal of the integrator gain (expressed as a time constant in accordance with normal PI controller convention). While the magnitude of $G_c(s)$ is essentially infinite at dc because of the $1/s\tau_i$ term, it rolls down to k_p at the integrator breakpoint frequency. Hence, to use this controller as an ac current regulator, k_p should be made as large as possible and τ_i should be made as small as possible, to maximize the magnitude of $G_c(s)$ (i.e., the controller bandwidth) up to the maximum system operating frequency and thus minimize the reference and tracking errors.

The overall system forward path open loop gain is given by

$$G_c(s)G_p(s) = \frac{k_p V_{\rm dc}}{R\tau_i}\frac{1 + s\tau_i}{s(1 + sT_p)} \tag{16}$$

which has two poles located at the origin and at $-1/T_p$, and a zero located at $-1/\tau_i$ by the integrator gain. Consequently, the system phase response has an asymptote at -90° for high frequencies, and hence the system is unconditionally stable for any value of controller gain k_p. Fig. 3 confirms this conclusion by presenting the simulated response of a controller with very high gain tracking a target ac current reference, for the test system with parameters as defined in Table I. It can be seen in this figure

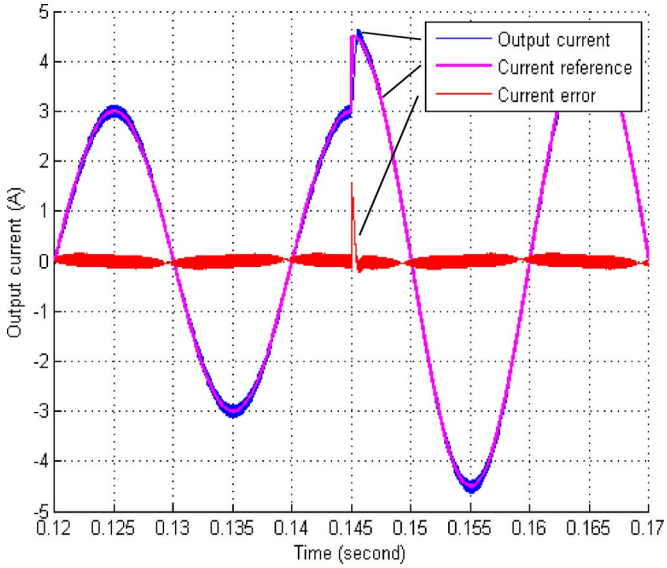

Fig. 3. Simulated response of ideal average value model ac current system with PI regulator, $k_p = 1$, $\tau_i = 0.0002$, 80 $V_{\rm rms}$ back EMF.

TABLE I
TEST SYSTEM CIRCUIT PARAMETERS

Circuit Parameter	Value
Plant Resistance R	1.2Ω
Plant Inductance L	20mH
Plant Time Constant T_p	16.67msec
Controller Sampling Frequency (2 x carrier f_s)	10kHz
DC bus voltage ($2V_{dc}$)	400V
Back *EMF* voltage (EMF)	$80V_{rms}$
Back *EMF* frequency	50 Hz

that the regulated current has negligible magnitude and phase error compared with the commanded target, with no suggestion of an unstable transient response despite the relatively high proportional gain that was required to achieve this performance. Of course, it is well known that this idealized response cannot be achieved in practice, since the effects of transport and sampling delays mean that any real system response becomes unstable well before the proportional gain is high enough to achieve this level of performance, as will now be explored.

III. Analysis of Transport and Sampling Delays

Most modern converter control systems use digital processors to implement the modulation process, implementing some variation of asymmetrical regular sampled PWM [14]. Fig. 4 shows the essential concept of PWM for a single phase leg, where the commanded phase leg voltage reference is frozen at the start of each half carrier period $\Delta T/2$ and compared against a triangular carrier "ramp" using a digital counter/comparator circuit that toggles the phase leg output as the ramp crosses the sampled command voltage. Intrinsically, this process introduces a quarter-carrier-period *transport* delay into the control

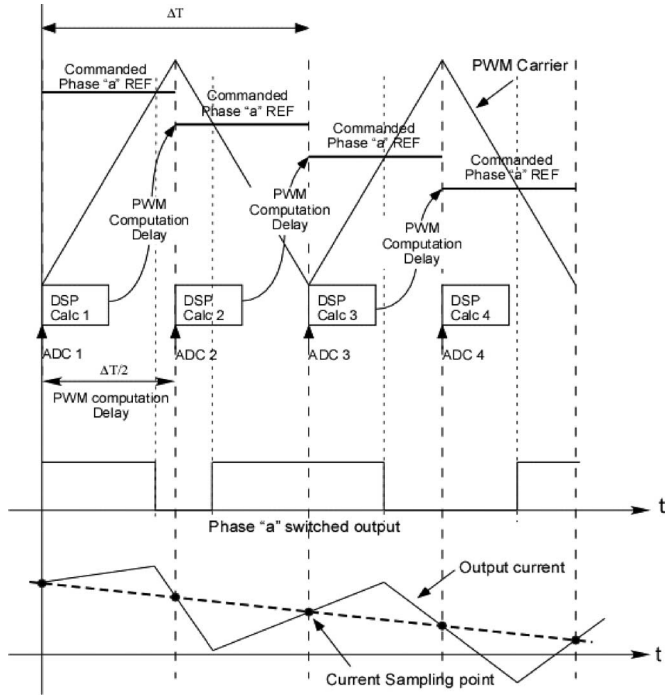

Fig. 4. Transport and sampling delay caused by the PWM process and digital controller sampling/computation.

loop, since the volt-second contribution of the switching process is delivered over the half-carrier period that follows the time instant at which the required volt-seconds were commanded by the current regulator for that period.

Practical digital controllers also require nonzero time to complete their control loop calculation after sampling the measured current. While this delay may be small for a high speed digital controller [i.e., a digital signal processor (DSP)], the measured current should be sampled exactly at the transition of each half-carrier interval to avoid sampling the switching ripple current as well as the underlying fundamental current (this is the time instant when the volt-second contribution of the phase leg switched output exactly matches the volt-second contribution commanded by the controller at the start of the half-carrier period). This introduces a further half-carrier *sampling* delay into the control loop. However, if the current is not synchronously sampled in this way, in most cases the measurement errors introduced will usually compromise the system performance much more seriously than the effects of this additional sampling delay.

Fig. 4 shows how sampling and transport delays, thus combine to create an overall 0.75 carrier period delay $T_d = 0.75\Delta T$ in the control loop. These delays can be incorporated into the system model either using a z-transform approach, or by simply including an e^{-sT_d} time delay block in series with the forward path controller, as shown in Fig. 5. Fig. 6 presents a Bode plot showing the effect of these delays on the forward path open loop gain for the test system described in Table I. Note that for this example, the integrator time constant has been set to 1.72 ms (approximately a decade above the plant time constant of 16.67 ms). From Fig. 6, it can be seen how the ideal forward path phase response approaches -180° above the plant pole breakpoint

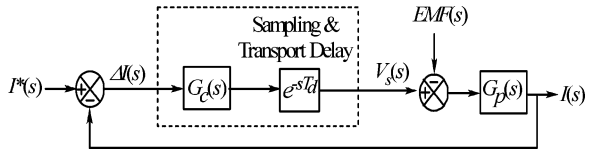

Fig. 5. Average value model block diagram representation of Fig. 1 including the effects of sampling and transport delay.

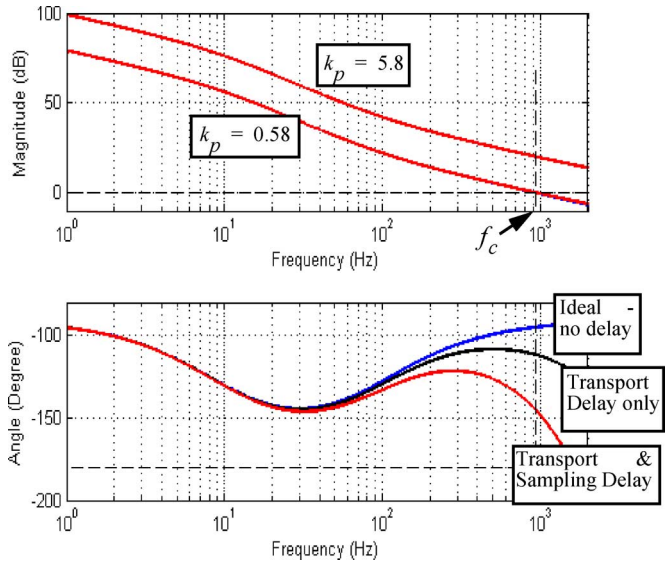

Fig. 6. Magnitude and phase Bode plot of open loop forward path loop gain for ideal controller, transport delay only, transport and sampling delay $\tau_i = 1.72$ ms.

frequency of 9.5 Hz, and then tracks back to the -90° asymptote as the frequency continues to increase and the integrator zero influence becomes significant. However, when transport and sampling delays are taken into account, the forward path phase response never reaches the -90° asymptote despite the integrator zero, but instead lifts up briefly from -180° and then falls back to track toward $-\infty^\circ$, as the frequency increases. The impact of this effect is considerable on the practical forward controller gain that can be achieved, since it is now possible to have an open loop phase shift exceeding -180° as the loop gain passes through unity (0 dB), and this is well known to produce an unstable system. The two magnitude plots shown in Fig. 6 show how increasing k_p simply raises the frequency response characteristic without changing its shape, from which it can be immediately argued that the maximum achievable value for k_p is the value that sets the open loop gain to unity as the open loop phase reaches $-180^\circ + \phi_m$, where ϕ_m is the required stability phase margin (classical control suggests a phase margin of 40° is an appropriate target to achieve an acceptably damped system response). However, determining the precise value of k_p and then τ_i needs further analysis.

IV. Optimized PI Stationary Frame Controller Gains

The key to determining the optimized stationary frame PI controller gains is found by more carefully examining the phase response curve shown in Fig. 6. The target objectives are to maximize the proportional gain k_p and then to minimize the integrator time constant τ_i (maximize the integrator gain), while taking into account the effect of sampling and transport delay and still retaining a phase margin of ϕ_m as the forward path open loop gain tracks through unity.

From Fig. 6, it is clear that maximum proportional gain is best achieved if the system crossover frequency ω_c (i.e., the frequency at which unity gain occurs with the required phase margin ϕ_m) is made as high as possible. Minimizing the integrator time constant then follows on accordingly.

Representing sampling and transport delay as an e^{-sT_d} time delay in the forward path, the system open loop gain becomes

$$G_c(s)G_p(s) = \frac{k_p V_{\rm dc}}{R\tau_i}\frac{(1+s\tau_i)e^{-sT_d}}{s(1+sT_p)}. \tag{17}$$

The phase angle of this forward path loop gain at the cross over frequency ω_c is given by (in radians)

$$\begin{aligned}&\angle\{G_c(j\omega_c)G_p(j\omega_c)\}\\ &= \angle\left\{\frac{k_p V_{\rm dc}}{R\tau_i}\frac{(1+j\omega_c\tau_i)e^{-j\omega_c T_d}}{j\omega_c(1+j\omega_c T_p)}\right\}\\ &= -\pi + \phi_m\\ &= \tan(\omega_c\tau_i)^{-1} - \pi/2 - \omega_c T_d - \tan(\omega_c T_p)^{-1}.\end{aligned} \tag{18}$$

Almost invariably, the system cross over frequency will be well above the plant pole frequency, and hence the angular contribution of $\tan^{-1}(\omega_c T_p)$ will be approximately $\pi/2$. Thus, from (18)

$$\phi_m \approx \tan^{-1}(\omega_c\tau_i) - \omega_c T_d \tag{19}$$

which gives

$$\omega_c = \frac{\tan^{-1}(\omega_c\tau_i) - \phi_m}{T_d}. \tag{20}$$

From (20), the maximum value of ω_c for a given ϕ_m clearly occurs when $\tan^{-1}(\omega_c\tau_i) = \pi/2$, so that

$$\omega_{c(\max)} = \frac{\pi/2 - \phi_m}{T_d}. \tag{21}$$

The maximum possible magnitude of k_p can now be found by setting the open loop gain at this value of $\omega_{c(\max)}$ to unity using (17), which gives

$$k_p = \frac{R\tau_i}{V_{\rm dc}}\omega_{c\,(\max)}\sqrt{\frac{(1+\omega^2_{c(\max)}T_p^2)}{(1+\omega^2_{c(\max)}\tau_i^2)}}. \tag{22}$$

If $\omega_{c(\max)}\tau_i \gg 1$ and $\omega_{c(\max)}T_p \gg 1$, as is usually the case for a typical ac current regulated system controlled by a PWM inverter, (22) reduces to

$$k_p \approx \frac{\omega_{c(\max)}L}{V_{\rm dc}} \tag{23}$$

which is dependant only on the plant series inductance, the cross over frequency (determined by the transport and sampling delays) and the dc bus voltage. Finally, the integral time constant τ_i can be minimized by making $\tan^{-1}(\omega_{c(\max)}\tau_i) \approx \pi/2$ (say

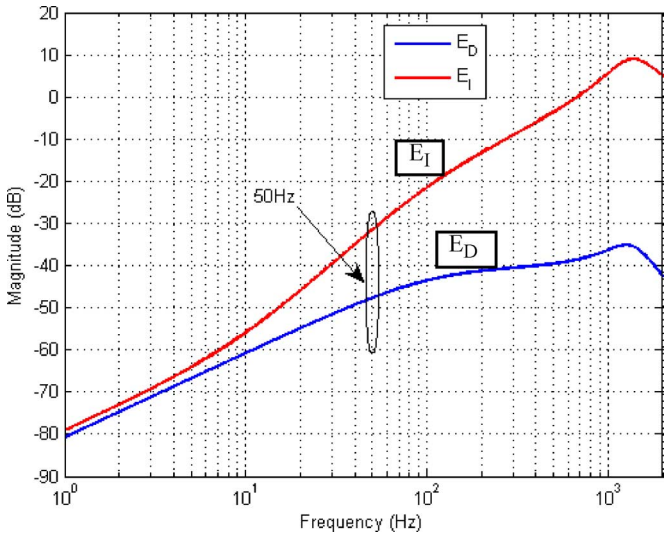

Fig. 7. Tracking and disturbance error for optimized PI stationary frame current regulator $k_p = 0.58$, $\tau_i = 1.72$ ms.

85°), which gives

$$\tau_i \approx \frac{10}{\omega_{c(\max)}}. \tag{24}$$

Taken together, this strategy allows the optimized gain values for any particular plant system to be deterministically calculated. Applying the approach to the test system described in Table I gives controller gains of $k_p = 0.58$ and $\tau_i = 1.72$ ms for a phase margin of $\phi_m = 40°$, with the resulting forward open loop magnitude and phase responses as already shown in Fig. 6.

V. Optimized Stationary Frame PI Regulator Performance

Once the controller gains have been optimized, the performance of the regulator can be readily evaluated by looking again at the tracking and disturbance errors as defined by (12) and (13), respectively. Fig. 7 shows these errors as a function of the frequency of the ac reference current. From this figure, it can be seen how the errors at dc are essentially zero, because of the almost infinite $G_c(s)$ controller gain that occurs at dc, and then increase as the target frequency increases and the magnitude of $G_c(s)$ correspondingly reduces. It can also be seen how the tracking error increases more rapidly than the disturbance error, because of the beneficial contribution made to the disturbance error by the plant dominant pole defined in the plant transfer function (9).

For the example system used in this paper, the error sensitivities at the nominal reference target frequency of 50 Hz can be calculated as 0.026 A/A for the tracking error, and 0.0042 A/V for the disturbance error. However, despite the fact that the disturbance error sensitivity is smaller than the tracking error sensitivity, for many ac current regulated systems the absolute magnitude of the disturbance injection (i.e., the back EMF) is substantially larger than the commanded reference current. Thus, in most cases the actual magnitude of the disturbance error will exceed the tracking error. For example, considering the test system used in this paper, the 80 $V_{\rm rms}$ back EMF will cause an absolute disturbance of $\Delta I_D = 0.0042 \times \sqrt{2} \times 80 = 0.48 A_{\rm peak}$ while an $8 A_{\rm peak}$ commanded current will only cause a tracking error of $\Delta I_I = 0.026 \times 7.5 = 0.195 A_{\rm peak}$. Hence, the absolute current error caused by the back EMF disturbance is more than twice the error caused by current reference tracking, and this is often the case in a practical ac current regulation system. Fig. 10(a) and (b) illustrates this error response, by presenting simulation and matching experimental results for the test system when commanded to produce a $5 A_{\rm peak}$, step changing to $7.5 A_{\rm peak}$, 50 Hz ac sine wave current, without and then with a back EMF disturbance present. From this figure, it can be seen how the phase *a* fundamental error peaks at 0.195 A without any back EMF present, but increases to nearly 0.5 A when back EMF is introduced into the system. These results almost exactly match the predictions based on the theoretical analysis presented above, and clearly confirm that sampling and transport delays are the dominant second order effects that constrain the proportional and integral gains of a practical PI stationary frame current regulation system. Furthermore, since the design strategy outlined previously optimizes the PI controller gains to their maximum possible achievable values for a given stability phase margin, the transient responses exhibited by the controller as shown in Fig. 10(a) and (b) will be the best that can be achieved with this type of controller structure.

The experimental results were obtained using a standard laboratory inverter controlled by a TI TMS320C240 digital signal processor operated with a center tapped 400 $V_{\rm dc}$ bus. The load was a three phase inductor set with parameters as listed in Table I, feeding into an 80 $V_{\rm rms}$ back EMF generated by a variac transformer, so that the back EMF could be readily measured and fed back to the controller to create the back EMF compensation signal when required.

VI. Reduction of Back EMF Disturbance Error Using Feed Forward Compensation

The analysis and results presented so far clearly illustrate the central limitation of a stationary frame PI regulator for ac current control—the proportional and integral gains are limited by the effects of sampling and transport delays, and when these gains are set to their maximum possible values as determined by stability considerations, there will often still be some residual fundamental target tracking error depending on the ratio of fundamental frequency to sampling frequency. The only way to reduce this error is to either increase the system controller gain at the fundamental reference frequency without affecting its higher frequency response (which would compromise the system stability), or to reduce the influence of at least one of the factors that cause steady-state error, such as back EMF [16].

Since back EMF is not a random disturbance input, its effect on fundamental tracking error can be substantially reduced by incorporating feed forward injection of a measured or estimated compensation signal into the current regulator, as shown in Fig. 8. Of course, when the back EMF is measured to provide the feed forward injection signal, it is subject to the same sampling and transport delay effects as for the main current

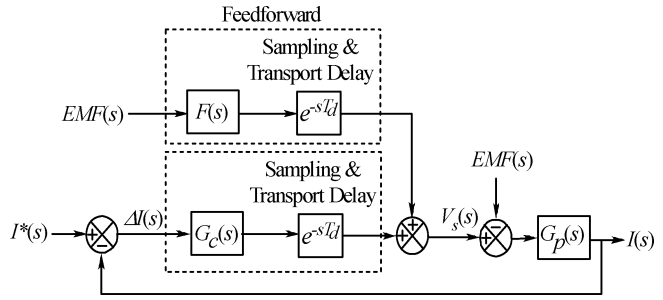

Fig. 8. Average value model block diagram representation of a PI current regulator with delay effects and feed forward compensation.

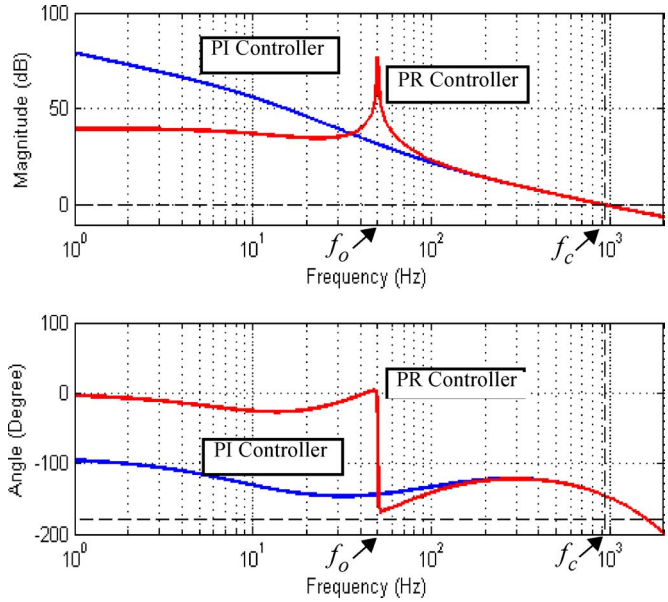

Fig. 9. Magnitude and phase Bode plot of $G_c(s)G_p(s)$ for PI and PR regulators with sampling/transport delay $T_d = 0.15$ ms, $k_p = 0.58$, $\tau_i = 1.72$ ms, $\omega_r = 0.1$ Hz.

regulator path, for the same practical implementation reasons. Equations (25) and (26) show the effect of this compensation on the output current and current error transfer functions, where $F(s)$ is a mismatch factor that can be used to assess the effect of inaccuracy in measuring or estimating the back EMF

$$I(s) = I^*(s)\frac{G_c(s)e^{-sT_d}G_p(s)}{1+G_c(s)e^{-sT_d}G_p(s)} - \mathrm{EMF}(s)\frac{G_p(s)(1-F(s)e^{-sT_d})}{1+G_c(s)e^{-sT_d}G_p(s)} \quad (25)$$

$$\Delta I(s) = \frac{I^*(s)+\mathrm{EMF}(s)\left\{G_p(s)(1-F(s)e^{-sT_d})\right\}}{1+G_c(s)e^{-sT_d}G_p(s)}. \quad (26)$$

With perfect feed forward, the second terms in (25) and (26) become zero, the back EMF disturbance error is eliminated $(E_D(s) = 0)$ and only the current reference tracking error $E_I(s)$ remains. The controller design process remains the same, optimizing k_p, and then τ_i as discussed previously, but the control decision now reduces to deciding whether the remaining $E_I(s)$ at the maximum required ac reference target frequency is sufficiently small to allow this simple PI regulator to be used. Fig. 10(c) shows the simulated and experimental test system responses for the test system controlled by a PI regulator with feed forward back EMF compensation, where it can be seen how the tracking error response has now returned to essentially that which was achieved without any back EMF disturbance, Fig. 10(a). However, it must be appreciated that back EMF compensation does not change the *closed loop disturbance rejection error* sensitivity defined by (13). Rather, it significantly reduces the level of disturbance input injection into the control loop, to the point where the tracking error introduced by this disturbance then becomes negligible. Overall, the results shown in Fig. 10 show that with optimized gain tuning and appropriate back EMF feed forward compensation, a simple PI regulator can achieve an excellent ac current regulation response and in many cases a more sophisticated strategy may be quite unnecessary.

It is interesting to reflect on the sensitivity of the feed forward disturbance cancellation to measurement or estimation error of the load back EMF [16]. From (26), it can be seen that even if there is a substantial 10% error in back EMF estimation, $F(s) = 0.9$ the strategy will still achieve a 20 dB improvement in the disturbance error contribution $\Delta I_D(s)$. For the test system considered in this paper, this would still reduce the back EMF disturbance error contribution to approximately $0.05\ A_{\mathrm{peak}}$ for the $80\ V_{\mathrm{rms}}$ back EMF (10 times less than the previously calculated $0.48\ A_{\mathrm{peak}}$), and this is much less than the *closed loop reference tracking error* of $0.195\ A_{\mathrm{peak}}$, which of course is still present in the system.

VII. Further Reduction of Steady-State Error Using a PR Regulator

For higher performance or lower switching frequency ac current regulation systems, the residual reference tracking error even after introducing back EMF compensation may still be unacceptably large. In this situation, the only remaining alternative is to increase the gain of the forward controller block at the target reference frequency, but without increasing the high frequency open loop gain since this would reduce the system phase stability margin. This is the essential strategy of the synchronous frame *d–q* controller for a three-phase system [6] and the PR controller in the stationary frame [9]. However, since the PR controller has previously been established to be essentially the stationary frame equivalent of the three-phase synchronous frame *d–q* controller [10], only the PR controller will be considered further in this paper.

The forward gain block $G_c(s)$ of an ideal PR controller is described by the transfer function

$$G_c(s) = k_p V_{\mathrm{dc}}\left[1+\frac{s}{\tau_i(s^2+\omega_0^2)}\right] \quad (27)$$

where ω_0 is the target reference current frequency. From this expression it can be seen how the $(s^2+\omega_0^2)$ term in the denominator creates infinite forward controller gain at ω_0. For higher frequencies, (27) gradually returns to the same transfer function as the simple PI regulator (15), and hence a similar high frequency response is to be expected for the two controller types.

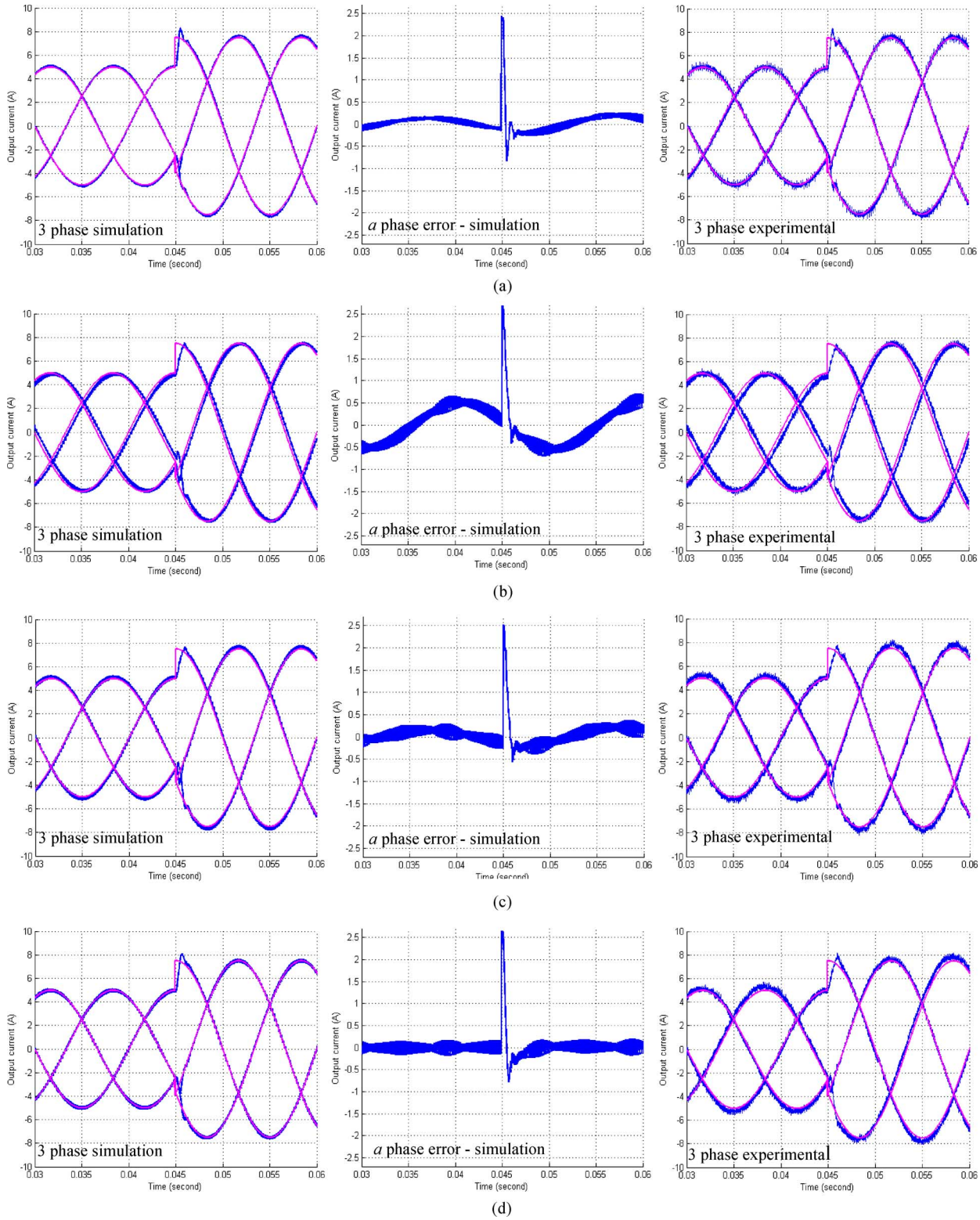

Fig. 10. AC current regulation response of simulated and experimental optimized stationary frame PI and PR current regulators $k_p = 0.58,\ \tau_i = 1.72$ ms. (a) PI controller, without back EMF. (b) PI controller, with back EMF, no feed forward compensation. (c) PI controller, with back EMF, with feed forward compensation. (d) PR controller, with back EMF.

Unfortunately, the ideal PR controller response defined by (27) can be challenging to physically realize [10], particularly using a fixed-point calculation as is typically available in current generation DSPs with PWM capability. Hence, a more practical alternative with damping is [9], [10]

$$G_c(s) = k_p V_{\rm dc}\left[1 + \frac{s}{\tau_i(s^2 + \omega_r s + \omega_0^2)}\right] \tag{28}$$

where ω_r is the resonant cut off frequency. While this form of controller limits the forward gain at ω_0 to $G_c(j\omega_0) = k_p V_{\rm dc}[1 + 1/\tau_i\omega_r]$, this is still a large gain increase of approximately ω_0/ω_r compared to the PI controller at the same frequency. In practice, gain increases of 40–60 dB are readily achievable using this PR formulation. As before, the effects of sampling and transport delay can be taken into account by adding an e^{-sT_d} term after $G_c(s)$. Fig. 9 illustrates the improvement that can be gained with a PR regulator by comparing the forward path open loop gain and phase responses for both controllers for the test system used in this paper.

In particular, it can be seen from this response how the PR controller phase reverts back to the PI controller phase response at higher frequencies, including the lift above the -180° asymptote because of the influence of the high frequency integrator zero, before the roll off caused by sampling and transport delays becomes dominant. Since this phase lead was used for the PI controller to maximize k_p while achieving unity loop gain with a required ϕ_m phase margin at the maximum possible crossover frequency $\omega_{c(\max)}$ and then to minimize the integral gain τ_i, exactly the same approach can be used to optimize the k_p and τ_i gains for the PR regulator, as follows:

The phase angle of the PR controller forward path at the cross over frequency ω_c is given by

$$\begin{aligned}
&\angle G_c(j\omega_c)G_p(j\omega_c) \\
&= \angle\left\{\frac{k_p V_{\rm dc}}{R}\left[1 + \frac{j\omega_c}{\tau_i\left\{(\omega_0^2 - \omega_c^2) + j\omega_r\omega_c\right\}}\right]\frac{e^{-j\omega_c T_d}}{(1 + j\omega_c T_p)}\right\} \\
&= (-\pi + \phi_m) \\
&\approx \tan^{-1}(\omega_c\tau_i) - \pi/2 - \omega_c T_d - \tan^{-1}(\omega_c T_p)
\end{aligned} \tag{29}$$

provided that the crossover frequency is high enough so that

$$\left|\frac{j\omega_c}{\tau_i\left\{(\omega_0^2 - \omega_c^2) + j\omega_r\omega_c\right\}}\right| \approx \left|\frac{1}{j\omega_c\tau_i}\right|. \tag{30}$$

Using a similar approximation as was used to develop (19) for the PI regulator, the forward path open loop phase margin can be expressed as

$$\phi_m \approx \tan^{-1}(\omega_c\tau_i) - \omega_c T_d. \tag{31}$$

Since (31) is the same condition as (19), the solution process leads to optimized PR controller k_p and τ_i gains (or synchronous *d–q* frame controller gains since this controller is equivalent to a PR controller) that are identical to those calculated for the PI controller, as might have been expected from the above discussion. This leads to the further conclusion that an identical transient response will be expected from an optimally tuned PR controller as from an optimally tuned PI controller. Matching simulation and experimental steady state and transient responses are shown in Fig. 10(d) for a PR regulator designed for the test system to confirm these concepts and analysis, with the same controller gains of $k_p = 0.58$ and $\tau_i = 1.72$ ms for all examples.

VIII. Conclusion

The analysis presented in this paper has been that the major performance constraint for linear closed loop ac current regulators is the proportional gain limitation imposed by transport and sampling delays associated with the control calculation and modulation processes. To improve the performance of an ac current controller beyond what can be achieved with a PI regulator, it is necessary to use PR or synchronous frame controllers that introduce a gain resonance at the reference target frequency without affecting the high frequency stability.

From this understanding, a method has been presented to deterministically calculate the maximum possible proportional and integral gain settings for a stationary frame PI ac current regulator, so as to achieve the lowest possible regulation error for this class of controller. The basic controller was then extended to implement feed forward compensation of the load back EMF to minimize the error caused by this disturbance, and leave only a reference tracking error that cannot be eliminated because of the controller gain limitations. The analysis was then applied to a PR regulator (and by association to a synchronous *d–q* frame regulator) to identify that the same delay limitations constrain the maximum proportional and integral gains for these controllers. In fact, the same gain optimizing design process can be used for all forms of linearized ac current regulators with, in most cases, the integrator time constant thus obtained being essentially independent of the parameters of the load. The analysis and conclusions are supported by precisely matched simulation and experimental results for a test system that is representative of a low to medium power level motor drive.

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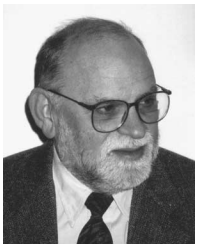

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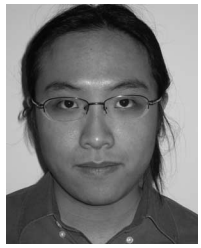

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