Energy Conversion and Management xxx (2010) xxx–xxx

Contents lists available at ScienceDirect

Energy Conversion and Management

journal homepage: www.elsevier.com/locate/enconman

Review of multilevel voltage source inverter topologies and control schemes

Ilhami Colak [a], Ersan Kabalci [b,*], Ramazan Bayindir [a]

[a] Department of Electrical Education, Faculty of Technical Education, Gazi University, Besevler, Ankara 06500, Turkey
[b] Department of Technical Programs, Vocational Collage of Haci Bektas, Nevsehir University, Hacibektas, Nevsehir 50800, Turkey

ARTICLE INFO

Article history:
Received 18 January 2010
Accepted 4 September 2010
Available online xxxx

Keywords:
Multilevel inverter
Neutral point clamped
Flying capacitor
Cascaded H-bridge
SPWM
SVM
SHE-PWM
Sigma–delta modulation
Modulation

ABSTRACT

In this study, the most common multilevel inverter topologies and control schemes have been reviewed. Multilevel inverter topologies (MLIs) are increasingly being used in medium and high power applications due to their many advantages such as low power dissipation on power switches, low harmonic contents and low electromagnetic interference (EMI) outputs. The selected switching technique to control the inverter will also have an effective role on harmonic elimination while generating the ideal output voltage. Intensive studies have been performed on carrier-based, sinusoidal, space vector and sigma delta PWM methods in open loop control of inverters. The selection of topology and control techniques may vary according to power demands of inverter. This paper and review results constitute a useful basis for matching of inverter topology and the best control scheme according to various application areas.

1. Introduction

The preliminary studies on multilevel inverters (MLI) have been performed using three-level inverter that has been proposed by Nabae. In the study, the third level has been constituted by using neutral point of DC line and the topology has been defined as diode clamped MLI (DC-MLI) [1,2]. In recent years, multilevel inverters have gained much attention in the application areas of medium voltage and high power owing to their various advantages such as lower common mode voltage, lower voltage stress on power switches, lower dv/dt ratio to supply lower harmonic contents in output voltage and current. Comparing two-level inverter topologies at the same power ratings, MLIs also have the advantages that the harmonic components of line-to-line voltages fed to load are reduced owing to its switching frequencies. The most common MLI topologies classified into three types are diode clamped MLI (DC-MLI), flying capacitor MLI (FC-MLI), and cascaded H-Bridge MLI (CHB-MLI). The hybrid and asymmetric hybrid inverter topologies have been developed according to the combination of existing MLI topologies or applying different DC bus levels respectively [3–9]. The basic topologies of MLIs are shown in Fig. 1. The recent applications of MLIs have a variety including induction machine and motor drives, active rectifiers, filters, interface of renewable energy sources, flexible AC transmission systems (FACTS), and static compensators. The diode clamped inverters, particularly the three-level structure, have a wide popularity in motor drive applications besides other multilevel inverter topologies. However, it would be a limitation of complexity and number of clamping diodes for the DC-MLIs, when the level exceeds three [10–13]. The FC-MLIs are based on balancing capacitors on phase buses and generate multilevel output voltage waveform clamped by capacitors instead of diodes. The FC-MLI topology also requires balancing capacitors per phase at a number of $(m-1)\cdot(m-2)/2$ for an m-level inverter and it will cause to increase the number of required capacitor in high level inverter topologies and complexity of considering DC-link balancing.

Among the three types of multilevel inverters, the cascade inverter has the least components for a given number of levels. Cascade multilevel inverters consists of a series of H-bridge cells to synthesize a desired voltage from several separate DC sources (SDCSs) which may be obtained from batteries or fuel cells. All these properties of cascade inverters allow using various pulse width modulation (PWM) strategies to control the inverter accurately [13–17]. In addition to these topologies, several modulation and control techniques have been developed for multilevel inverters including selective harmonic elimination PWM (SHE-PWM), sinusoidal PWM (SPWM), space vector PWM (SVM), and similar variations of the three main algorithms. The modulation methods used in multilevel inverters can be classified according to switching frequencies as seen in Fig. 2 [18–21].

The SPWM control method is very popular in industrial applications owing to its harmonic reducing opportunities by using

* Corresponding author. Tel.: +90 3844413432; fax: +90 3844413441.
E-mail address: kabalci@nevsehir.edu.tr (E. Kabalci).

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doi:10.1016/j.enconman.2010.09.006

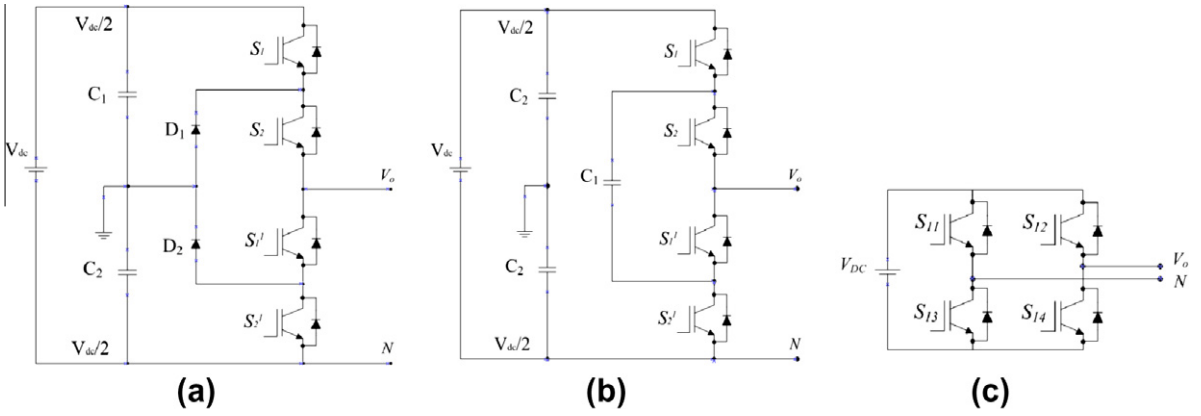

Fig. 1. Multilevel inverter topologies: (a) three-level DC-MLI, (b) three-level FC-MLI, (c) three-level CHB-MLI.

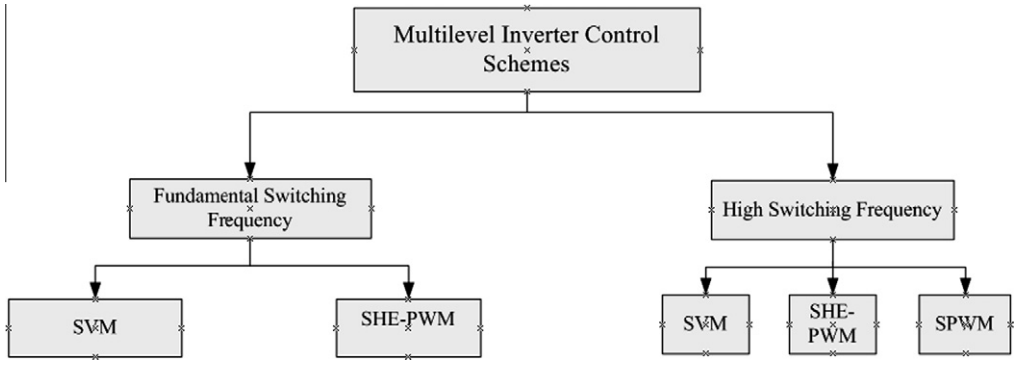

Fig. 2. Classification of multilevel inverter control schemes.

several phase shifting options on carrier signal. In the SPWM, a sinusoidal reference voltage waveform is compared with a triangular carrier waveform to generate gate signals for the switches of inverter. Several multicarrier techniques have been developed to reduce the THD ratios, based on the classical SPWM with triangular carriers. Another alternative modulation technique is SVM strategy, which has been used appropriately in three-level inverters. The SVM and SHE-PWM methods are fundamental frequency switching methods and perform one or two commutations of the power semiconductors during one cycle of the output voltages to generate a staircase waveform [22–26].

This paper presents the multilevel inverter topologies and their control methods according to existing and novel applications, based on a well-surveyed literature summary. A comprehensive study has been performed on common and hybrid multilevel inverters, and the most appropriate control schemes and applications have been proposed according to topologies.

2. Common inverter topologies

Three major multilevel inverter structures which have been mostly applied in industrial applications have been emphasized as the diode clamped, the flying capacitor, and the cascaded H-bridge inverters with separate DC sources. In addition to this, various hybrid multilevel inverters have been developed by using the three basic types mentioned above. Voltage source inverters (VSIs) are widely used in AC motor drives, AC uninterruptible power supplies (UPS), and AC power supplies with batteries, fuel cells, active harmonic filters. VSI topologies are constituted in accord with power demand of application areas and output voltages are either single phase for power demands lower than 2 kV A or three-phase for power demands over 2 kV A as being used in household and industrial loads. The semi converter, half bridge and full bridge inverters were employed for high power applications in 1990s, but recently many researchers have paid much attention to multilevel inverters for high power and medium voltage applications [27–31]. Main three multilevel inverter topologies and hybrid models of these structures have been reviewed in the following part of the paper by demonstrating sample models and control strategies.

2.1. Diode clamped multilevel inverters (DC-MLI)

The diode clamped multilevel proposed by Nabae, Takashi, and Akagi in 1981 was named as neutral point converter and was essentially a three-level diode clamped inverter as shown in Fig. 1a. Several experimental studies and articles published about results of three, four, five and six level DC-MLIs for such uses like static VAR compensators, high voltage grid interconnections, and variable speed motor drives [32–36]. A three-phase five-level DC-MLI topology is shown in Fig. 3. Each of the three-phase outputs of inverter shares a common DC bus voltage that has been divided into five levels over four DC bus capacitors. The capacitors have been subscripted from C_1 to C_4. The middle point of C_2 and C_3 capacitors constitute the neutral point of inverter and output voltages have five voltage states referring to neutral point. The voltage across each capacitor is $V_{dc}/4$ and the voltage stress on each switching device is limited to V_{dc} through the clamping diodes that have been named as $D_{1..3}$ and $D_{1\_3}^{1\_3}$. The key components that differ with this topology from a conventional two-level inverter are clamping diodes. To explain how the staircase voltage is synthesized, the neutral point n has been assumed as the output phase

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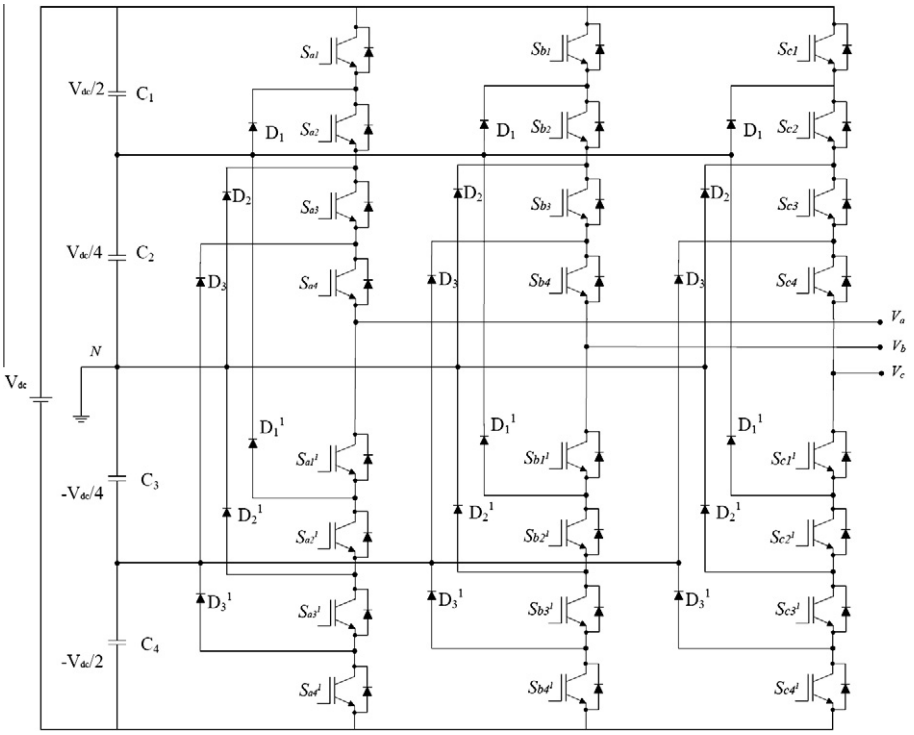

Fig. 3. Three-phase five-level topology of a diode clamped multilevel inverter.

voltage reference and the switching combinations have been analyzed for phase A output voltage V_{an} as seen in Table 1.

For the five-level DC-MLI in Fig. 3, a set of four switches is ON at any given period of time and they are S_{a1} to S_{a4} for voltage level of $V_{an} = V_{dc}/2$. The second switching state shows the voltage level of $V_{an} = V_{dc}/4$ and S_{a2} to S^1_{a1} switches should be triggered. The remaining switching states that constitutes 0 and negative outputs can be seen in Table 1. The clamping diodes require different voltage ratings for reverse voltage-blocking due to each triggered switch is only required to block a voltage level of $V_{dc}/(m-1)$. By assuming the switches from S_{a1} to S_{a4} are triggered as seen in first line of Table 1, D_1 blocking diode needs to block a voltage at the rate of $3V_{dc}/4$ that is generated by three DC bus capacitors.

Since each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be calculated as $(m-1)\cdot(m-2)$, where m represents number of inverter levels. The following equations are used to determine the required device numbers to form a given level of a diode clamped MLI. If m is assumed as the number of levels, the number of capacitors at the DC side (c) can be known by using Eq. (1). The number of freewheeling diodes (d) per phase, and the number of clamping diodes (j) can be calculated by using Eqs. (2) and (3) respectively.

$$c = m - 1 \tag{1}$$

Table 1
Voltage levels of five-level DC-MLI and switching states.

Voltage V_{an}	Switching state							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a1}{}^1$	$S_{a2}{}^1$	$S_{a3}{}^1$	$S_{a4}{}^1$
$V_4 = V_{dc}/2$	1	1	1	1	0	0	0	0
$V_3 = V_{dc}/4$	0	1	1	1	1	0	0	0
$V_2 = 0$	0	0	1	1	1	1	0	0
$V_1 = -V_{dc}/4$	0	0	0	1	1	1	1	0
$V_0 = -V_{dc}/2$	0	0	0	0	1	1	1	1

$$d = 2(m-1) \tag{2}$$

$$j = (m-1)\cdot(m-2) \tag{3}$$

The DC-MLIs are efficient in fundamental frequency switching applications but the number of clamping diodes required is quadratically related to the number of levels. Fundamental frequency switching will cause an increment on voltage and current THD, while increased number of clamping diode makes the topology bulky [34–39].

2.2. Flying capacitor multilevel inverters (FC-MLI)

The FC-MLI has been introduced in 1992 as an alternative topology to DC-MLI by Meynard [40]. A three-phase five-level topology of this inverter is shown in Fig. 4. Main structure of this topology is similar to DC-MLI but the inverter uses DC side capacitors in a ladder form instead of clamping diodes. The voltage change between two adjoining capacitor legs gives the size of the voltage steps in the output waveform. In an m level structure, the FC-MLIs require $(m-1)$ DC link capacitors and $(m-1)\cdot(m-2)/2$ auxiliary capacitors per phase comparing to DC-MLI topology [38,41–43].

In Fig. 4, each of the three-phase outputs of inverter shares a common DC bus voltage that has been divided into five levels over four DC bus capacitors similar to DC-MLI topology. The auxiliary capacitors (C_{a1}, C_{a2}, and C_{a3}) are pre-charged to the voltage levels of $V_{dc}/4$, $V_{dc}/2$, $3V_{dc}/4$ respectively. The pre-charge operation ensures the effectiveness of the inverter allowing it to generate multilevel voltage waveforms. Voltage synthesis in a five-level FC-MLI has more flexibility than a DC-MLI. The FC-MLI topology also consists of complementary switch pairs as $(S_{a1} - S_{a1}{}^1)$, $(S_{a2} - S_{a2}{}^1)$, $(S_{a\,3} - S_{a3}{}^1)$, and $(S_{a4} - S_{a1}{}^4)$ as seen in Fig. 4. The switching pairs may differ as asymmetrically according to control strategies, but both pair selection strategy will cause the switching state redundancy that can be used to achieve voltage balancing in FC-MLIs [8,40,43].

Table 2 shows the switching combinations for phase voltage output (V_{an}) that is relative to neutral point of n. The optional

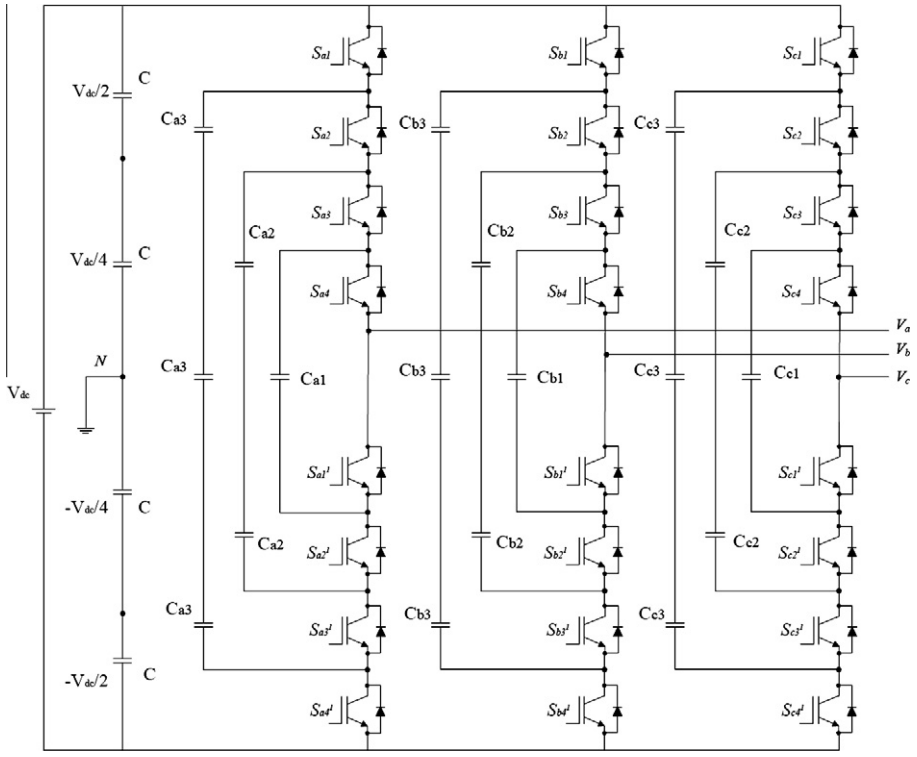

Fig. 4. Three-phase five-level topology of flying capacitor multilevel inverter.

switching states for voltage levels of $V_{dc}/4$, 0, $-V_{dc}/4$ shows the phase redundancies of FC-MLI as an advantage to line-to-line redundancies of DC-MLI. This advantage allows the user to select charging and discharging orders of capacitors by constituting proper switching algorithms.

The most important advantages of FC-MLI topology are preventing the filter demand, and controlling the active and reactive power flow besides phase redundancies. Although these advantages, the increment of m level will restrain the accurate charging and discharging control of capacitors. The cost of inverter will increase and device will be more enlarged due to increased number of capacitors.

2.3. Cascaded H-bridge multilevel inverters (CHB-MLI)

An alternative multilevel inverter topology with less power devices requirement compared to previously mentioned topologies is known as cascaded H-bridge multilevel inverter (CHB-MLI) and the topology is based on the series connection of H-bridges with separate DC sources. Since the output terminals of the H-bridges are connected in series, the DC sources must be isolated from each other. Owing to this property, CHB-MLIs have also been proposed to be used with fuel cells or photovoltaic arrays in order to achieve higher levels [8,11,44–45].

Table 2
Voltage levels of five-level FC-MLI and switching states.

Voltage V_{an}	Switching state							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a1}{}^1$	$S_{a2}{}^1$	$S_{a3}{}^1$	$S_{a4}{}^1$
$V_4 = V_{dc}/2$	1	1	1	1	0	0	0	0
$V_3 = V_{dc}/4$	1	1	1	0	1	0	0	0
	0	1	1	1	0	0	0	1
	1	0	1	1	0	0	1	0
$V_2 = 0$	1	1	0	0	1	1	0	0
	0	0	1	1	0	0	1	1
	1	0	1	0	1	0	1	0
	1	0	0	1	0	1	1	0
	0	1	0	1	0	1	0	1
	0	1	1	0	1	0	0	1
$V_1 = -V_{dc}/4$	1	0	0	0	1	1	1	0
	0	0	0	1	0	1	1	1
	0	0	1	0	1	0	1	1
$V_0 = V_{dc}/2$	0	0	0	0	1	1	1	1

The resulting AC output voltage is synthesized by the addition of the voltages generated by different H-bridge cells. Each single phase H-bridge generates three voltage levels as $+V_{dc}$, 0, $-V_{dc}$ by connecting the DC source to the AC output by different combinations of four switches, S_{A1}, $S_{A1}{}^1$, $S_{A\,2}$, and $S_{A2}{}^1$ as seen in first cell of Fig. 5. The CHB-MLI that is shown in Fig. 5 utilizes two separate DC sources per phase and generates an output voltage with five levels. To obtain $+V_{dc}$, S_{A1} and $S_{A2}{}^1$ switches are turned on, whereas $-V_{dc}$ level can be obtained by turning on the $S_{A\,2}$ and $S_{A1}{}^1$. The output voltage will be 0 by turning on S_{A1} and S_{A2} switches or $S_{A1}{}^1$ and S_{A2} switches. If n is assumed as the number of modules connected in series, m is the number of output levels in each phase as seen in Eq. (4). The switching states of a CHB-MLI (sw) can be determined by using Eq. (5)

$$m = 2n + 1 \tag{4}$$

$$sw = 3^m \tag{5}$$

The first leg phase voltage (V_{an}) of Fig. 5 is constituted by multiplying V_{a1} and V_{a2} values of series connected H-bridge cells and will generate a stepped waveform as seen in Fig. 6.

Positive output pulses are shown with P_1 and P_2 while the negative ones are indicated as $P_1{}^1$ and $P_2{}^1$. The Fourier series expansion of the general multilevel stepped output voltage is shown in Eq. (6) and the transform is applied for Fig. 5 in Eq. (7), where n is the harmonic number of the output voltage of inverter. The switching angles that are indicated as $\Theta_1 \ldots \Theta_5$ in Eq. (6) can be chosen to obtain minimum voltage harmonics and several

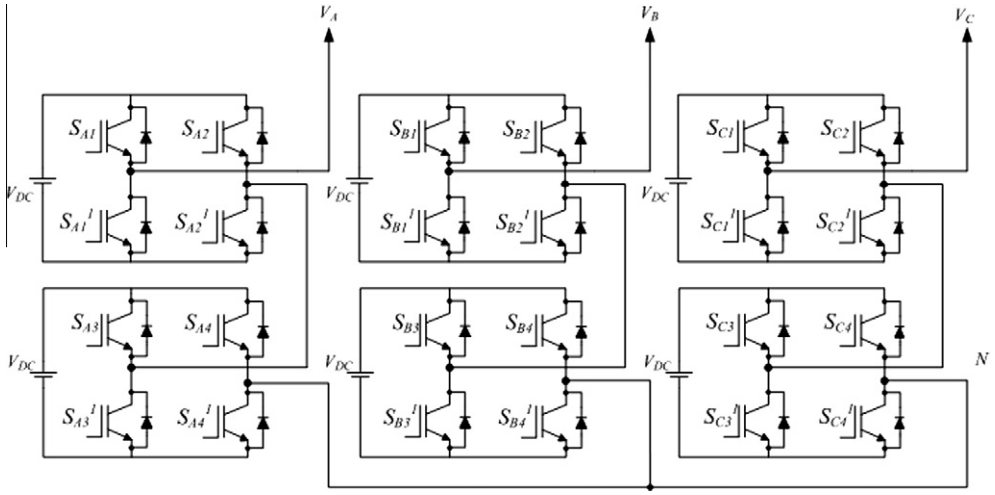

Fig. 5. Three-phase five-level topology of cascaded H-bridge multilevel inverter.

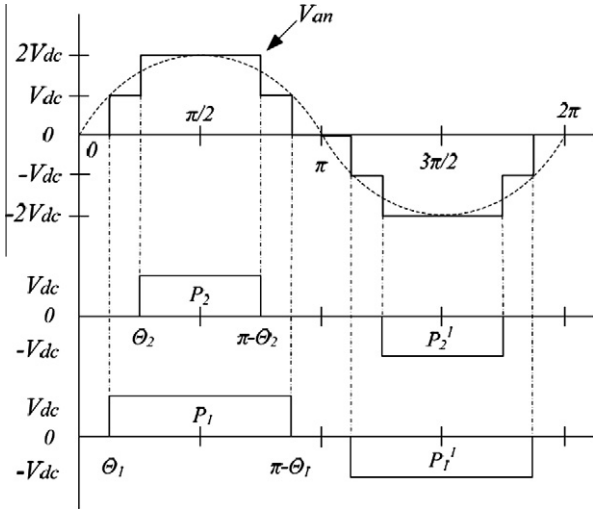

Fig. 6. Phase output voltage waveforms of a five-level topology CHB-MLI with two separate DC sources.

fundamental frequency switching techniques have been evaluated such as selective harmonic elimination PWM or active harmonic elimination PWM.

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_5)] \frac{\sin(n\omega t)}{n} \tag{6}$$

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} [\cos(n\theta_1) + \cos(n\theta_2)] \frac{\sin(n\omega t)}{n} \tag{7}$$

An example switching angle calculation is given in Eq. (8) to eliminate 5th, 7th, 11th, and 13th order harmonics.

$$Cos(\theta_1) + Cos(\theta_2) + Cos(\theta_3) + Cos(\theta_4) + Cos(\theta_5) = 5 \cdot m_i \tag{8}$$

$$Cos(5 \cdot \theta_1) + Cos(5 \cdot \theta_2) + \cdots + Cos(5 \cdot \theta_5) = 0$$

$$Cos(7 \cdot \theta_1) + Cos(7 \cdot \theta_2) + \cdots + Cos(7 \cdot \theta_5) = 0$$

$$Cos(11 \cdot \theta_1) + Cos(11 \cdot \theta_2) + \cdots + Cos(11 \cdot \theta_5) = 0$$

$$Cos(13 \cdot \theta_1) + Cos(13 \cdot \theta_2) + \cdots + Cos(13 \cdot \theta_5) = 0$$

The modulation index is defined as m_i and can be calculated as in Eq. (9),

$$m_i = \frac{\pi V_1}{4V_{dc}} \tag{9}$$

Since the values of Eq. (8) are non-linear, the calculations are obtained by using Newton–Raphson Iteration. The fundamental and high frequency control methods will be reviewed in the next section of the paper. CHB-MLIs have been previously designed for static VAR compensators and motor drives, but the topology has been prepared an interface with renewable energy sources due to using separate DC sources. There are numerous studies have been performed on CHB-MLIs for connecting renewable energy sources with AC grid and power factor correction [45–49].

2.4. Asymmetric hybrid multilevel inverters (AH-MLI)

Besides the three basic multilevel inverter topologies previously discussed, new MLI topologies based on the existing multilevel topologies have been proposed and classified as hybrid topologies. The hybrid multilevel topologies are constituted by using combination of two basic topologies utilize the DC-MLI or FC-MLI to replace the H-bridge as the basic module of the CHB-MLI in order to reduce the number of the separated DC sources. The asymmetric hybrid MLIs synthesize the output voltage waveforms with reduced harmonic content [8,18,33]. This advantage is achieved by using distinct voltage levels in different modules, which can generate more levels in output voltage waveform and reduces the THD ratio, while preventing to increase the number of switching devices and sources. Each power module of a hybrid MLI can be operated at distinctive DC voltage and switching frequency improving the efficiency and THD compensation characteristics of inverter. Nevertheless, conventional PWM strategies, which generates switching frequency at fundamental frequency are not appropriate for AH-MLIs due to switching devices of the higher voltage modules, would have to operate at high frequencies only during some inverting instants. To achieve this control strategy, hybrid modulation methods have been proposed that provide to get higher power cells switched at low frequency and low power cells switched with high frequency [50–53].

The most widely used AH-MLI topologies are shown in Fig. 7 as one phase legs of three-phase applications. The diode clamped and H-bridge cascaded seven-level hybrid topology is shown in Fig. 7a. Other seven-level hybrid topologies that are constituted by cascading flying capacitor module or H-bridges of different

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switching devices to basic CHB-MLI module are seen in Fig. 7b and c, respectively. The hybrid DC-MLI topology in Fig. 7a utilizes CHB-MLI's excellent input current and output voltage property to constitute an efficient and reliable module. On the other hand, DC-MLI has a simple circuit, but requires a large LC output filter in motor drive applications. The hybrid FC-MLI topology obviates filtering requirements proportionally to DC-MLI, but this topology is not robust as hybrid CHB-MLI to reduce harmonic contents and about the cost of construction. The asymmetric hybrid CHB-MLI in Fig. 7c uses a gate turn-off (GTO) module with an insulated-gate bipolar transistor (IGBT) H-bridge module and reveals a high voltage-blocking but a low switching frequency capability. This trade-off can be dealt by using a hybrid asymmetric MLI. Applying this approach to CHB-MLI topology allows reducing the number of H-bridge modules while maintaining the number of output voltage levels.

Hybrid MLIs promise significant improvements for medium voltage and high power industrial drives. Asymmetrical multilevel inverters provide minimizing the harmonic contents of output voltage without increasing the number of power devices. The use of various DC voltages in supply leads the H-MLI topologies in an effort to optimize the power processing of the entire system. The surveyed features increase the flexibility and reliability of H-MLIs.

3. Control schemes

The efficiency parameters of a multilevel inverter such as switching losses and harmonic reduction are principally depended on the modulation strategies used to control the inverter. As depicted in Fig. 2, multilevel inverter control techniques are based on fundamental and high switching frequency. Another widely used popular classification for the modulation methods developed to control the multilevel inverters is depend upon open loop and closed loop concepts as depicted in Fig. 8. Three main control techniques of multilevel inverters are SHE-PWM, PWM, and optimized harmonics stepped pulse width modulation (OHS–PWM). The regular PWM modulation method can be classified as open loop and closed loop owing to its control strategy. The open loop PWM techniques are SPMW, space vector PWM, sigma–delta modulation, while closed loop current control methods are defined as hysteresis, linear, and optimized current control techniques. The modulation methods developed to control the multilevel inverters are based on multi-carrier orders with PWM. Due to pre-defined calculations are required, SHE-PWM is not an appropriate solution for closed loop implementation and dynamic operation in multilevel inverters. Among various control schemes, the sinusoidal PWM (SPWM) is the most commonly used control scheme for the control of multilevel inverters. In SPWM, a sinusoidal reference waveform is compared with a triangular carrier waveform to generate switching sequences for power semiconductor in inverter module [17–18,54–56].

Another fascinating control scheme is SVM as one of the most promising control methods in three-phase systems. Despite three-level SVM control is obtained by using two-level SVM, three-level mode is significantly more complex than two-level structure due to increased number of power semiconductors. As a result of this complexity, three-level SVM algorithm is almost implemented using digital signal processors (DSPs) or microcontroller units (MCUs) [57–58]. One of the most important methods to optimize control of the inverter is to select and design appropriate PWM modulation according to inverter topology. The control methods of hybrid multilevel inverters are based on multi-carrier SPWM. Fundamental switching frequency methods shall be selected to reduce switching losses for high voltage modules, while multi-carrier SPWM is selected to control low voltage modules. A detailed review has been performed for various modulation methods in the following and a comparison list has been presented to match inverter topologies to control methods at the end of this section.

3.1. Selective harmonic elimination PWM (SHE-PWM)

The selective harmonic elimination PWM (SHE-PWM) technique is based on fundamental frequency switching theory proposed by Patel in 1974 [59], and dependent on the elimination of defined harmonic content orders. The main idea of this method is based on defining the switching angles of harmonic orders to eliminate and obtaining the Fourier series expansion of output voltage. An example output voltage Fourier expansion of an 11-level inverter can be written as in Eq. (10).

$$V(wt) = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4Vdc}{n\cdot\pi}\cdot(\cos(n\cdot\theta_1)+\cos(n\cdot\theta_2)+\cdots+\cos(n\cdot\theta_5))\cdot\sin(n\cdot wt) \quad (10)$$

where n defines the harmonic order at the output voltage of multilevel inverter. The required switching angles to eliminate 5th, 7th, 11th, and 13th harmonic orders at fundamental switching

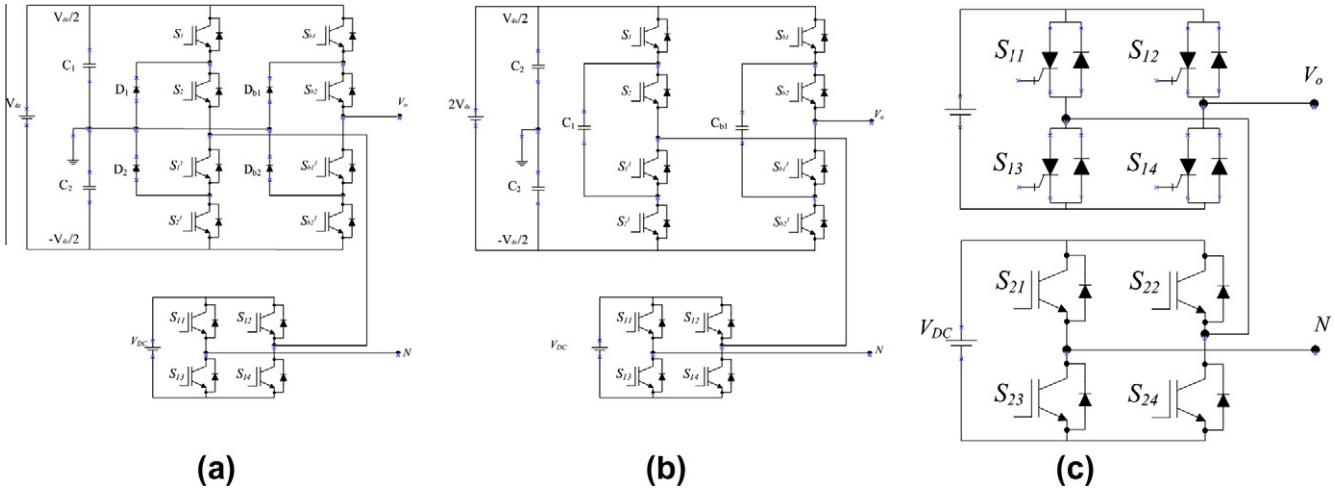

Fig. 7. One phase legs of three-phase asymmetric hybrid MLI topologies: (a) DC-MLI and CHB-MLI cascaded, (b) FC-MLI and CHB-MLI cascaded, (c) asymmetric hybrid CHB-MLI cascaded.

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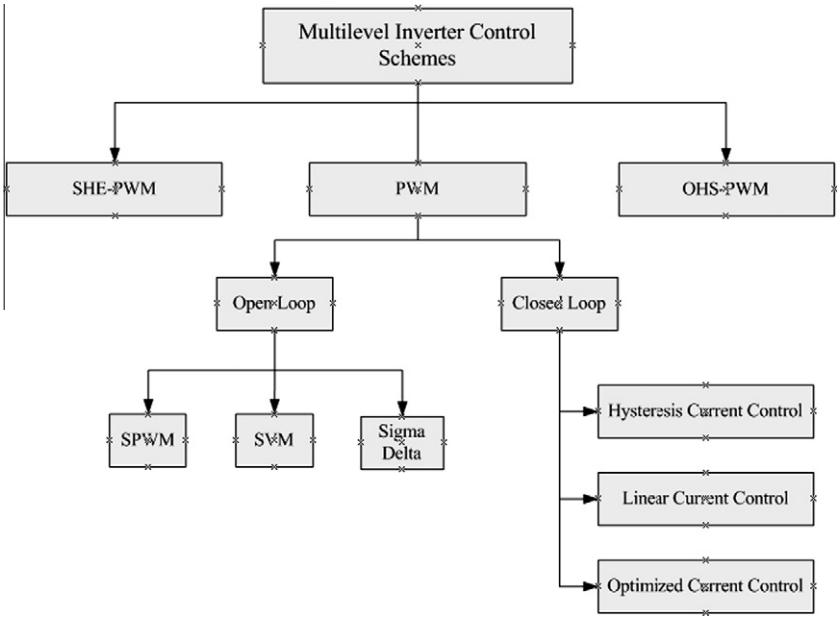

Fig. 8. Control schemes of multilevel inverters.

frequency for an 11-level multilevel inverter can be calculated as given in Eq. (11).

$$Cos(\theta_1) + Cos(\theta_2) + \cdots + Cos(\theta_5) = 5 \cdot m_a \tag{11}$$

$$Cos(5 \cdot \theta_1) + Cos(5 \cdot \theta_2) + \cdots + Cos(5 \cdot \theta_5) = 0$$

$$Cos(7 \cdot \theta_1) + Cos(7\theta_2) + \cdots + Cos(7 \cdot \theta_5) = 0$$

$$Cos(11 \cdot \theta_1) + Cos(11 \cdot \theta_2) + \cdots + Cos(11 \cdot \theta_5) = 0$$

$$Cos(13 \cdot \theta_1) + Cos(13 \cdot \theta_2) + \cdots + Cos(13 \cdot \theta_5) = 0$$

The switching angles of $\theta_1, \theta_2, \ldots, \theta_5$ can be determined to minimize voltage THD ratio, while m_a defines the modulation index of modulator. Since the parameters of Eq. (11) are nonlinear, the values are obtained using Newton–Raphson Iterations. The switching angles can be obtained at the values of $\theta_1 = 6.57°$, $\theta_2 = 18.94°$, $\theta_3 = 27.18°$, $\theta_4 = 45.14°$ and $\theta_5 = 62.24°$ by assuming m_a as 0.8 and solving with Newton–Raphson Iteration. In the application of SHE-PWM, possible switching angles are calculated previously and saved to look-up tables in an independent memory or microprocessor. The main defect of SHE-PWM is the requirement of calculations to determine switching angles as in fundamental frequency switching method. However, Newton–Raphson Iteration is able to solve an equation similar to Eq. (11), the initial values are based on guesses or assumes and the results will not be at accurate values. In addition to this, increased DC sources or switching angles will prevent to obtain the most accurate solution [2,59–62].

3.2. Open loop PWM control techniques

3.2.1. Sinusoidal PWM (SPWM)

SPWM technique is one of the most popular modulation techniques among the others applied in power switching inverters. In SPWM, a sinusoidal reference voltage waveform is compared with a triangular carrier waveform to generate gate signals for the switches of inverter. Power dissipation is one of the most important issues in high power applications. The fundamental frequency SPWM control method was proposed to minimize the switching losses. The multi-carrier SPWM control methods also have been implemented to increase the performance of multilevel inverters and have been classified according to vertical or horizontal arrangements of carrier signal. The vertical carrier distribution techniques are defined as Phase Dissipation (PD), Phase Opposition Dissipation (POD), and Alternative Phase Opposition Dissipation (APOD), while horizontal arrangement is known as phase shifted (PS) control technique. In fact PS-PWM is only useful for cascaded H-bridges and flying capacitors, while PD-PWM is more useful for NPC [18,42,46].

Each of the mentioned multi-carrier SPWM control techniques have been illustrated in Fig. 9, respectively. The sinusoidal SPWM is the most widely used PWM control method due to many advantages including easy implementation, lower harmonic outputs according to other techniques, and low switching losses. In SPWM control, a high frequency triangular carrier signal is compared with a low frequency sinusoidal modulating signal in an analog or logic comparator devices. The frequency of modulating sinusoidal signal defines the desired line voltage frequency at the inverter output [63–66].

A three-phase full bridge inverter and the SPWM modulator that has been designed to generate switching signals for three-phase full bridge inverter is depicted in Fig. 10a and Fig. 10b [67]. In the designed three-level inverter, modulated SPWM signals have been used to control Mosfet switches of the inverter, and THD analysis of output voltage and current have been performed as seen in Table 3.

The design parameters were as follows;

DC voltage (V_{DC}) = 300 V
Modulation index (m_i) = 0.6 < m_i < 1.4
Switching frequency (f_{sw}) = 1 kHz < f_{sw} < 10 kHz
Load resistance (RL) = 5 Ω
Load impedance (L) = 5 mH
Rated power = 10 kV A

In the harmonic analyses of SPWM controlled inverter designed using Simulink; the lowest THD for current has been measured as 0.88% while modulation index is 0.6 and switching frequency at 10 kHz. The THD for line voltage has been measured as 5.36% for the same operating conditions [67]. The line voltage has increased

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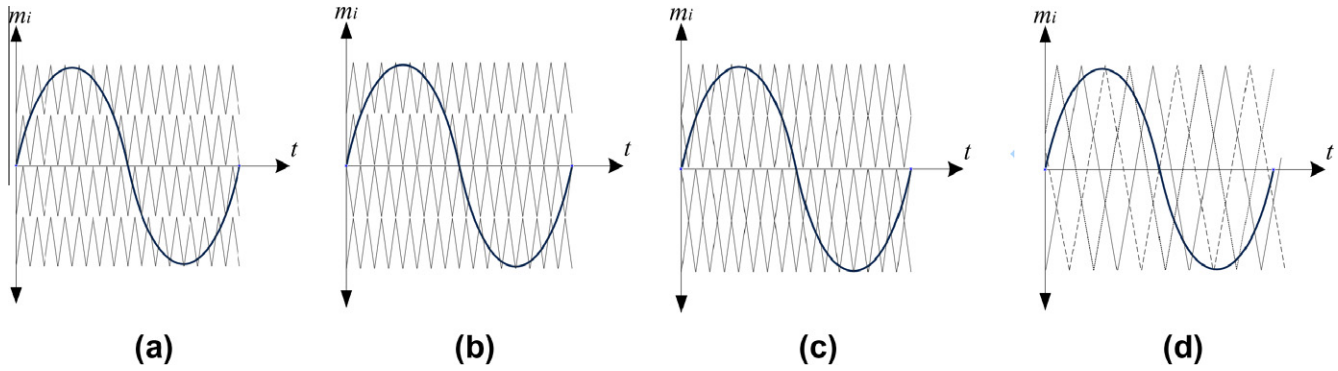

Fig. 9. Multi-carrier SPWM control strategies: (a) PD, (b) POD, (c) APOD, (d) PS.

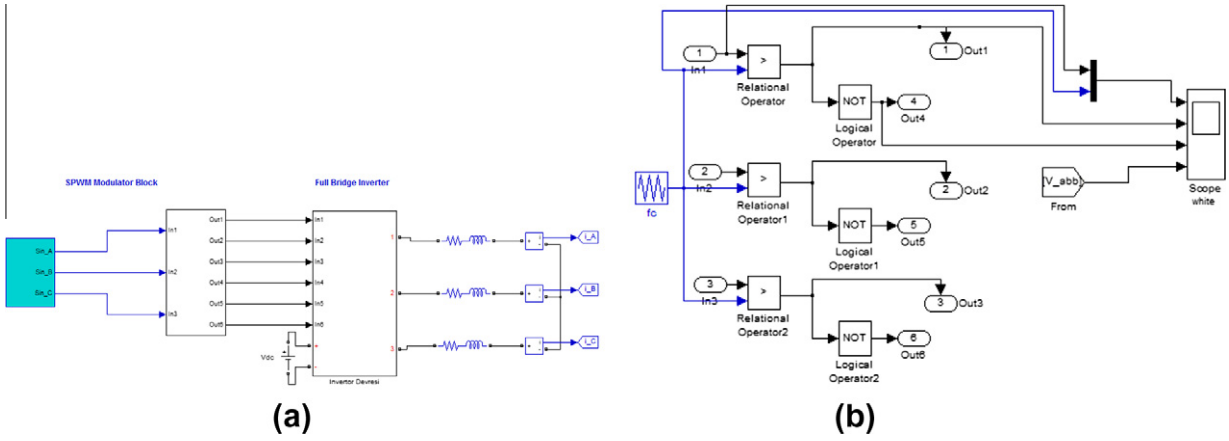

Fig. 10. An SPWM controlled inverter: (a) complete system, (b) modulator block of inverter.

almost proportional to Eq. (13) in over-modulation range, while proportional to Eq. (12) in linear modulation range.

In SPWM control technique, the output voltage is obtained in linear modulation range,

$$V_{AB} = V_{BC} = V_{CA} = m_i \frac{\sqrt{3}V_d}{2} \quad 0 < m_i \leqslant 1 \tag{12}$$

and the output voltage value is defined for the over-modulation range as seen in Eq. (13).

$$\frac{\sqrt{3}V_d}{2} < V_{AB} = V_{BC} = V_{CA} < \frac{4}{\pi}\frac{\sqrt{3}V_d}{2} \quad m_i \geqslant 1 \tag{13}$$

Another application has been implemented using SPWM technique to control a five-level CHB-MLI as seen in Fig. 11 [68]. The designed VSI is based on the topology of Fig. 5 which includes dual H-bridge cells as shown in Fig. 1c per phase to generate a five-level output voltage. The main topological calculations which are performed initially indicate the requirements of modulator and inverter blocks, and allow obtaining a well prepared modulation algorithm to increase the performance of inverter.

The proposed inverter includes six H-bridges and four SPWM switching signals to control each bridge respectively. The modulation algorithm has been performed in SPWM modulator block to generate 24 separate SPWM pulses for H-bridges. The SPWM modulator has a switching bandwidth between 0 and 40 kHz to control H-bridges. Fig. 12 shows the values which are obtained at 5 kHz switching conditions, while $m_i = 1$. Fig. 12a and b represent the FFT analysis of the current THD (THDi) and voltage THD (THDv) ratios in Simulink.

The switching frequency of SPWM modulator has been limited to 1–10 kHz, and modulation indexes are selected in $0.6 \leqslant m_i \leqslant 1.4$ ranges to analyze the effect of f_{sw} and m_i on THD of inverter.

It has been observed by the performed tests that reducing the THD of current and voltage is depended on increasing the

Table 3
Current and voltage THD analysis of full bridge inverter.

	m_a	Switching freq. (Hz)	Line voltages (V)	Line currents (A)	Switching angle	THD ratios (% THD)	
						Line current	Line voltage
1	0.6	1000	202.8	16.19	30	9.34	107.25
2	0.6	2000	212	16.19	30	4.46	92.72
3	0.6	5000	202.8	16.27	30.4	1.71	25.21
4	0.6	10,000	206.3	16.28	29.89	0.88	5.36
5	0.8	1000	277.1	21.58	30	8.30	81.72
6	0.8	2000	295.7	22.94	29.86	5.41	64.91
7	0.8	5000	293.8	23.01	29.96	2.97	33.63
8	0.8	10,000	303.9	24.04	29.55	5.01	17.28
9	1	1000	351.6	27.31	30.14	8.28	61.21
10	1	2000	355.7	27.68	29.78	4.16	51.78
11	1	5000	377	29.23	29.67	3.78	32.66
12	1	10,000	409.1	32.1	26.62	4.82	14.23
13	1.2	1000	385.1	29.98	30.05	7.95	52.68
14	1.2	2000	387.7	30.22	29.92	4.60	48.42
15	1.2	5000	389.8	32.47	22.34	10.59	32.10
16	1.2	10,000	425.9	33.15	26.4	7.57	22.01
17	1.4	1000	399.8	31.12	30.3	7.43	49.37
18	1.4	2000	403.9	31.58	29.93	4.14	46.43
19	1.4	5000	424.4	32.47	28.23	4.83	27.75
20	1.4	10,000	441.3	33.36	23.53	7.13	15.31

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switching frequency in linear modulation range as shown in Fig. 13a and b respectively [68].

The output current and voltage values have been increased in over-modulation range since m_i is over 1, but the THD rates have been changed nonlinearly. The lowest THD for current of the designed MLI has been measured as 0.1% during 10 kHz switching frequency and $m_i = 0.8$ conditions. The THD analyses of two different inverter topologies controlled with SPWM have been depicted in Fig. 14 applying 5 kHz switching frequency while modulation index was 1.

The current THD of five-level CHB-MLI has been found 1.34%, while current THD of three-level full bridge multilevel inverter was 3.78%. The least THD of CHB-MLI has been determined as 0.1% for 10 kHz switching frequency and $m_i = 1$ conditions. The lower switching frequency in linear modulation range has caused to higher THD for current and voltage at the output of inverter.

3.2.2. Space vector PWM (SVM)

An alternative popular control method for multilevel inverters is defined as space vector PWM (SVM) that directly uses the control variable given by the control system and identifies each switching vector as a point in complex space of (α, β).

The harmonic elimination and fundamental voltage ratios in SVM schemes are obtained in better values compared to SPWM schemes. In addition to this, the maximum peak value of the output voltage is 15% greater than triangular carrier-based modulation techniques. Sector identification and look-up table requirement to determine the switching intervals for all vectors make SVM method quite complicated. Although the difficulty of determining sectors and switching sequences according to increased n-level of inverter, DSP and microprocessor implementations provide proper solution while preparing the algorithms.

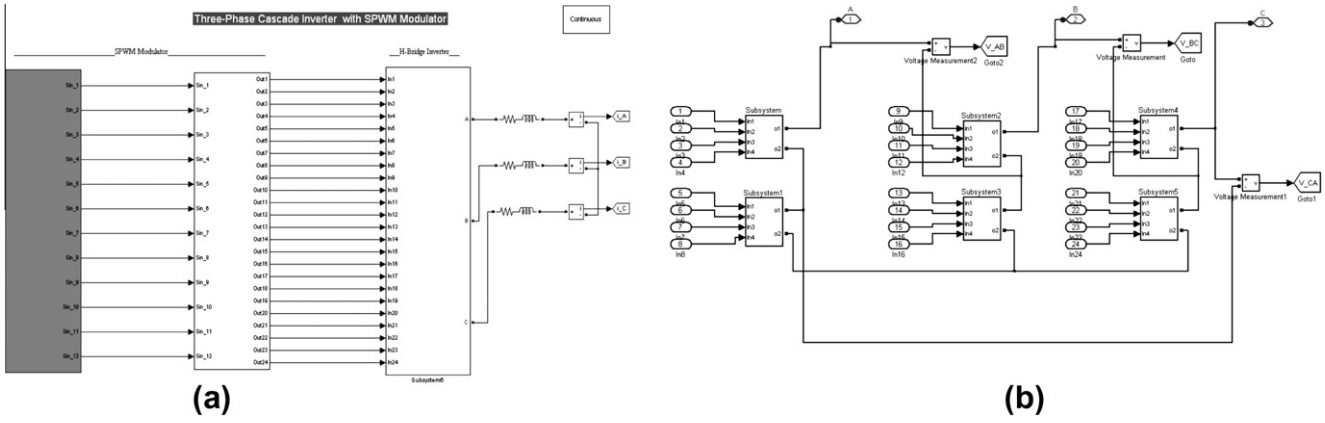

Fig. 11. An SPWM controlled five-level CHB-MLI controlled inverter: (a) complete system, (b) CHB-MLI block.

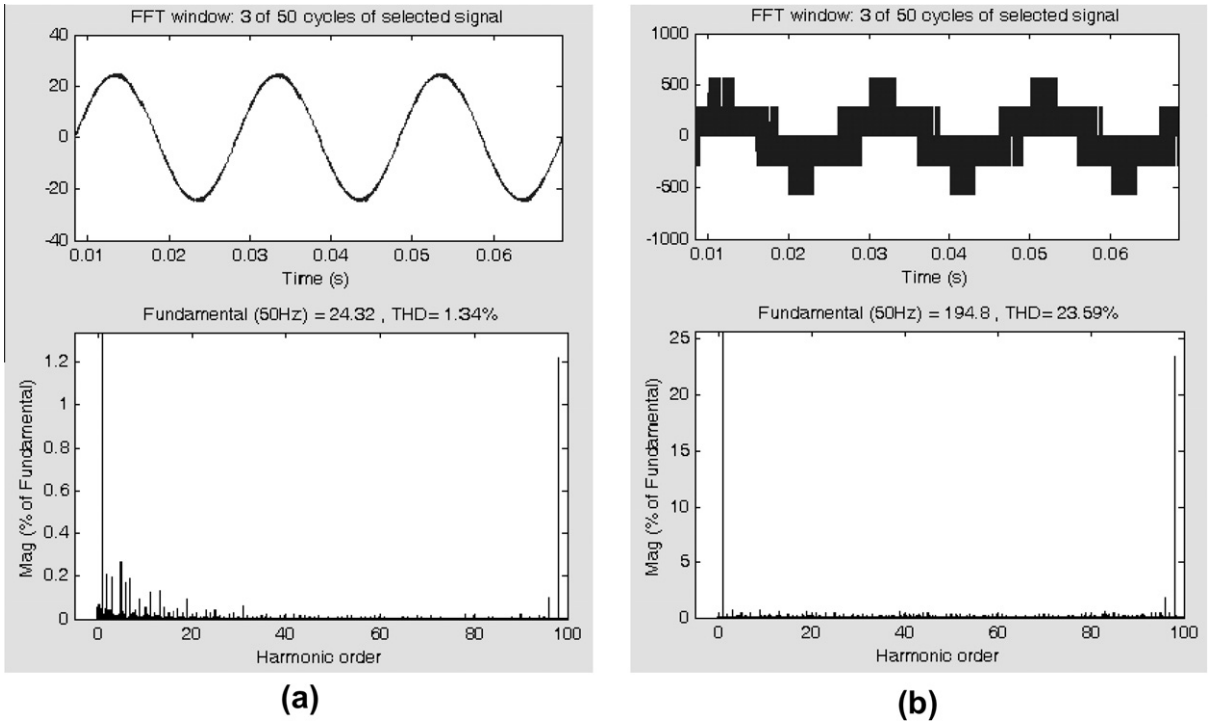

Fig. 12. THD analysis of inverter while $f_{sw} = 5$ kHz and $m_i = 1$: (a) THD for current is 1.34%, (b) THD for phase voltage is 23.59%.

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The SVM method uses a number of level-shifted carrier waves to compare with the reference phase voltage signals when applied to multilevel inverters. Any three-phase n-level space vector diagram consists of six sectors that all contains $(n-1)^2$ vector combinations per sector and n^3 switching. Fig. 15 shows the space vector diagram of a three-phase three-level DC-MLI inverter that's one phase leg is depicted in Fig. 1a. Each phase leg of inverter includes four switching devices and has three different switching states that are represented as 1, 0, or −1 to illustrate positive, zero, and negative switching sequences [39,57–58,69–76].

The switching states have been shown on vector intersections and 27 different states have been located to illustrate required switching states. The switching states and definitions for output voltage levels are given in Table 4 as referring to DC-MLI in Fig. 1a. The zero voltage vectors has three switching states as (0 0 0, 1 1 1, −1 −1 −1). The vectors given in Fig. 15 are classified into three groups that are named as small vectors ($V_1 - V_6$), middle vectors (V_8, V_{10}, V_{12}, V_{14}, V_{16}, V_{18}), and the large vectors (V_7, V_9, V_{11}, V_{13}, V_{15}, V_{17}). By assuming the reference voltage vector V_{ref} located in the 2nd region (Δ_2) of S_1 sector, it can be constituted by voltage vectors of V_1, V_2, and V_8 during the sampling period (T_s). The reference voltage also depends on the dwelling times of voltage vector. Hence, the equation for ON time of the voltage vectors that constitutes the reference voltage can be given as in Eq. (14).

$$V_{\text{ref}} \cdot T_s = V_1 \cdot t_a + V_2 \cdot t_b + V_8 \cdot t_c \tag{14}$$

ON times of voltage vectors can be determined using Eq. (14) as given in Eq. (15);

$$\left.\begin{aligned} t_a &= T_s - 2n\sin\theta \\ t_b &= 2n\sin(\tfrac{\pi}{3}+\theta) - T_s \\ t_c &= T_s - 2n\sin(\tfrac{\pi}{3}-\theta) \end{aligned}\right\} \tag{15}$$

where $n = (4\sqrt{3}/3)(V_{ref}/V_{dc})T_s$.

The calculations given above has been performed to show one of the possible V_{ref} value in a region of sectors and required to reply to determine each switching sequence. There are various studies have been realized to reduce complicated calculations of vectors, and simplify the required SVM algorithms in order to control multilevel inverters that generate five-level and above output voltage [72–81].

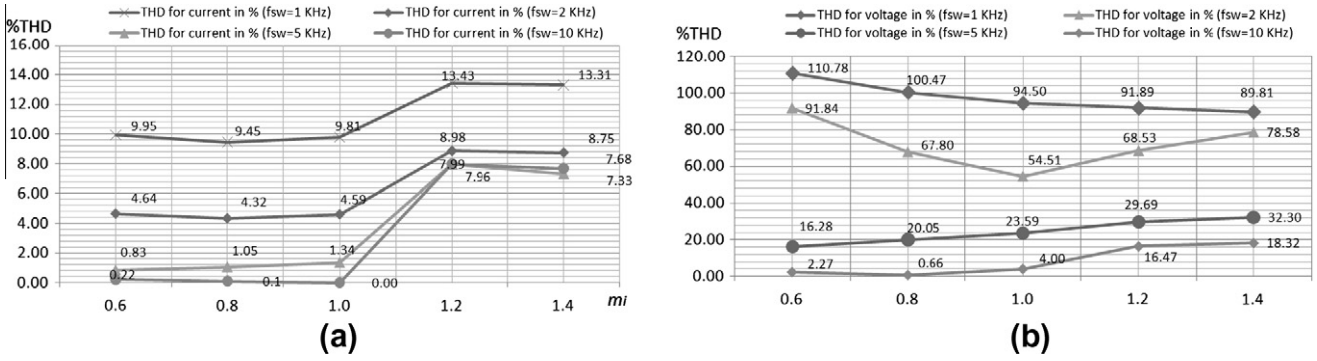

Fig. 13. THD analysis of inverter at various switching frequencies and modulation indexes: (a) THD for current in %, (b) THD for phase voltages in %.

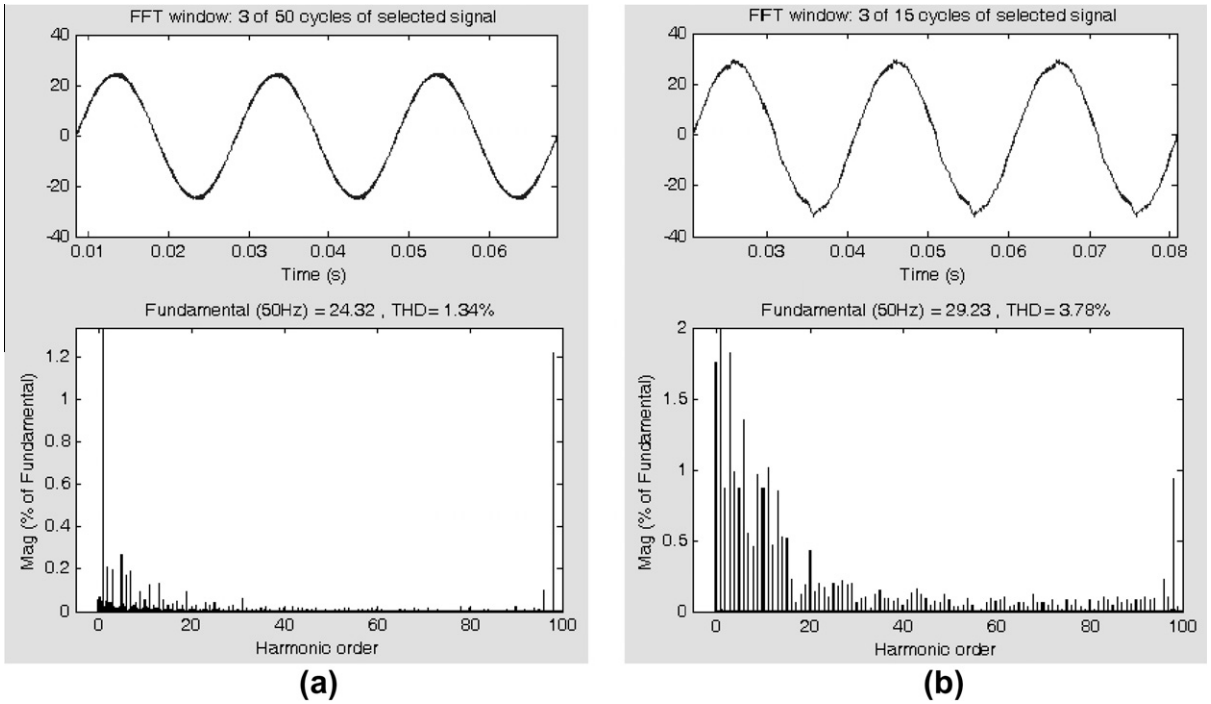

Fig. 14. Current THD comparison of topologies, while $m_i = 1$ $f_{sw} = 5$ kHz: (a) five-level CHB-MLI inverter output, (b) three-level full bridge inverter output.

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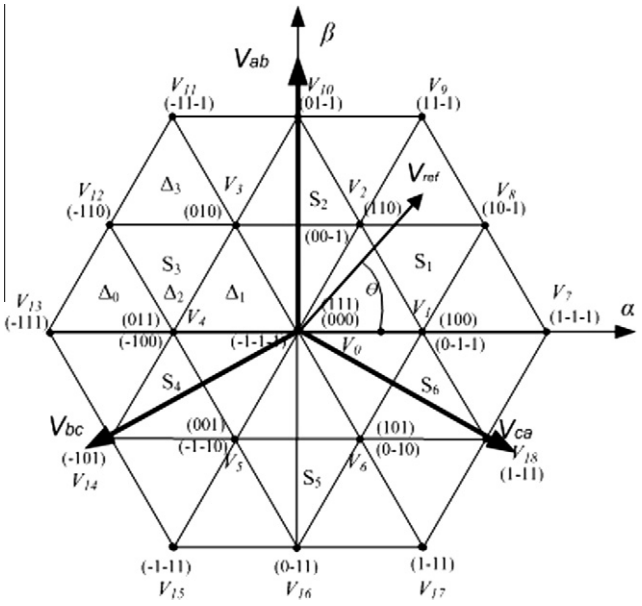

Fig. 15. Space vector diagram of a three-level inverter with sector and subsectors.

3.2.3. Sigma delta PWM (SDM)

The delta modulation (DM) technique was firstly introduced as a 1-bit coding method of pulse code modulation (PCM) by Jager in 1952. One-bit coding application was achieved using an integrator feedback block to pulse modulator that is a component of encoding process as seen in Fig. 16a [82–83]. Originally the DM was proposed as a 1-bit audio and video signal encoding method in digital modulating and control techniques issues. The sigma–delta modulation (SDM) has been described with [84] in order to prevent the decreasing on power density of modulated signal according to increased sampling frequency. A SDM system was obtained adding a sample and hold block to a basic DM modulator as depicted in Fig. 16b.

The SDM has adapted to power conversion processes using analog to digital (ADC) and digital to analog converters (DAC) that are widely used in several applications due to development of semiconductor technologies. The utilization of resonant DC-link inverters (RDCLI) allows the soft switching applications instead of hard switching of conventional PWM. This kind of inverters is mostly known with their zero switching losses obtained by switching at predetermined times of a sampler clock and this method can be appropriately adapted to SDM. In the Fig. 16b, the output of modulator changes between $+V_o$, 0, and $-V_o$ according to sampling period of f_s and the output is compared with input amplitudes. The comparison result (e) is integrated (E) and the quantizer determines the output sign opposite to E. A multilevel SDM generates multi-bit data sequence and decoding the output yields several output states which can be used to control on/off states of the switches of multilevel inverter. Fig. 17 depicts the block diagram of an SDM controlled multilevel inverter. The interaction of SDM modulator and inverter is managed using a multilevel decode logic block that adopts the quantized SDM signals and decodes to switching signals for inverter [85–91].

The researches show that although it has been developed to control DC-link inverters, the sigma–delta modulators can be developed to control multilevel inverters using logic interfaces. For a SDM controlled multilevel inverter, the output errors such as irregular voltage distribution and system nonlinearity can be reduced in high frequency switching up to 200 kHz.

3.3. Closed loop PWM control techniques

Most applications of three-phase voltage source PWM inverters such as motor drives, active filters, and static VAR compensators require a control structure comprising an internal current feedback loop. Multilevel inverter systems also utilizes photovoltaic (PV) sources or wind generators to integrate renewable energy sources to grid. The performance of the inverter systems which are supplied with DC sources mentioned before largely depends on the quality of the applied current control strategy. Numerous studies have been performed to reduce harmonic contents using current control for active power filter or PV and wind generator interconnection to grid applications of MLIs. The applied current control techniques are mostly focused on hysteresis current control (HCC) and linear current control (LCC) [90–96].

The hysteresis modulation is a feedback current control method where the load current tracks the reference current within a

Table 4
Switching states and definitions.

Switching symbol	Switching states						Phase voltage
	S_1	S_2	$S_1{}^1$	$S_2{}^1$	D_1	D_2	
1	ON	ON	OFF	OFF	OFF	OFF	$V_{dc}/2$
0	OFF	ON	ON	OFF	Depend on polarity of load voltage		0
−1	OFF	OFF	ON	ON	OFF	OFF	$V_{dc}/2$

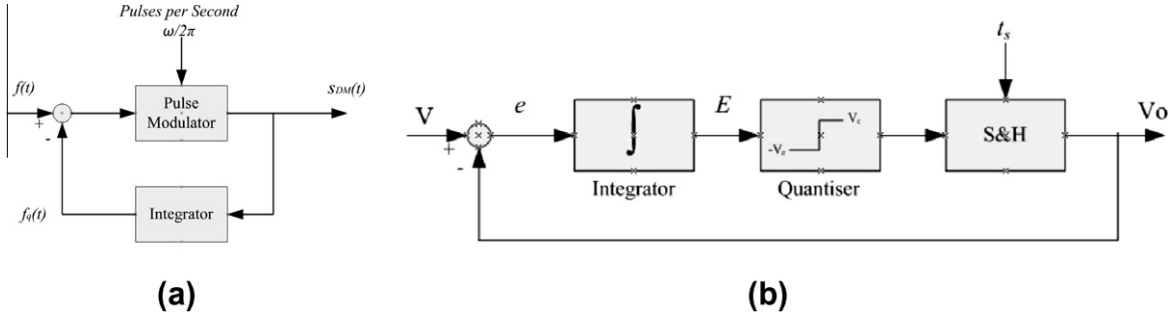

Fig. 16. Block diagrams of delta modulation: (a) simple delta modulator, (b) sigma–delta modulator.

hysteresis band in nonlinear load application of an MLI. Fig. 18a shows the block diagram of a hysteresis control of an H-bridge and Fig. 18b shows the operation principle of the hysteresis modulation. The controller generates the sinusoidal reference current of desired magnitude and frequency that is compared with the actual line current. If the current exceeds the upper limit of the hysteresis band, the next higher voltage level should be selected to attempt to force the current error towards zero. However, the new inverter voltage level may not be sufficient to return the current error to zero and inverter should switch to next higher voltage level until the correct voltage level is selected. As a result, the current gets back into the hysteresis band, and the actual current is forced to track the reference current within the hysteresis band. Three hysteresis controllers which are used to implement the correct voltage level selection are defined as double offset band three level, double band three level, and time-based three level hysteresis controllers [93–101].

As an alternative approach of MLI applications, the grid interconnection with inverter also requires current control schemes. Linear current controllers are classified as ramp comparison controller, stationary vector controller, and synchronous vector controller. The ramp comparison current controller utilizes the output-current ripple and feedback to control the switching instants. In the three-phase isolated neutral-load topology, the three-phase current should have a sum of zero. Therefore, two linear compensators are required and the three-phase inverter reference voltage signals can be established algebraically using two-to-three-phase conversion αβ/abc blocks as seen in Fig. 19.

The basic linear current controller consists of a tracking regulator with a proportional-integrator compensator for PV inverters. Several harmonics compensator schemes can be found in the literature based on repetitive control and linear resonant harmonic compensators [101–107].

4. Comparison of the topologies and control scheme

The most common multilevel inverter topologies and control schemes have been reviewed in this paper. As mentioned in Section 1, the multilevel concept has been introduced with a diode clamped topology in 1980s by Nabae. MLIs are increasingly being used in medium voltage and high power applications owing to numerous advantages such as low power dissipation due to reducing the voltage stress on switching devices and minimizing the harmonic contents at the output of the inverter. The selected control scheme for an MLI determines the affectivity on harmonic elimination, while generating the ideal output voltage. The applications of MLIs including induction machine and motor drives, active filters, renewable energy sources interconnection to grid, flexible AC transmission systems (FACTS), and static compensators (STATCOM) have been widely used in industrial applications. Although the variety of MLI applications, there are several limitations have

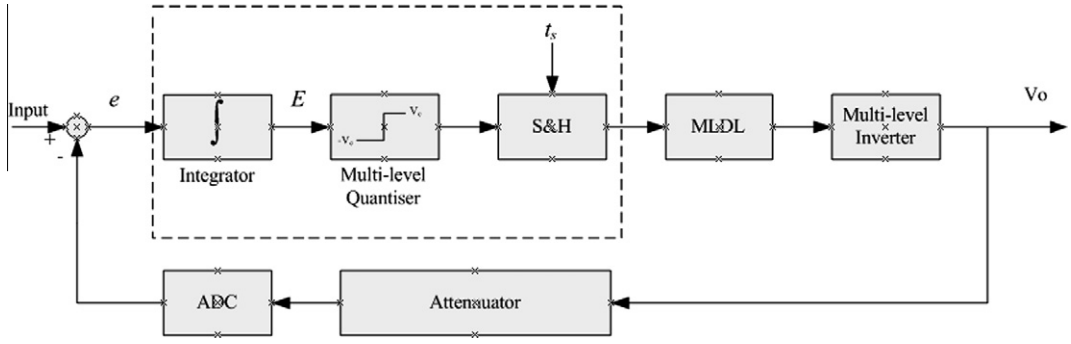

Fig. 17. SDM control of a multilevel inverter.

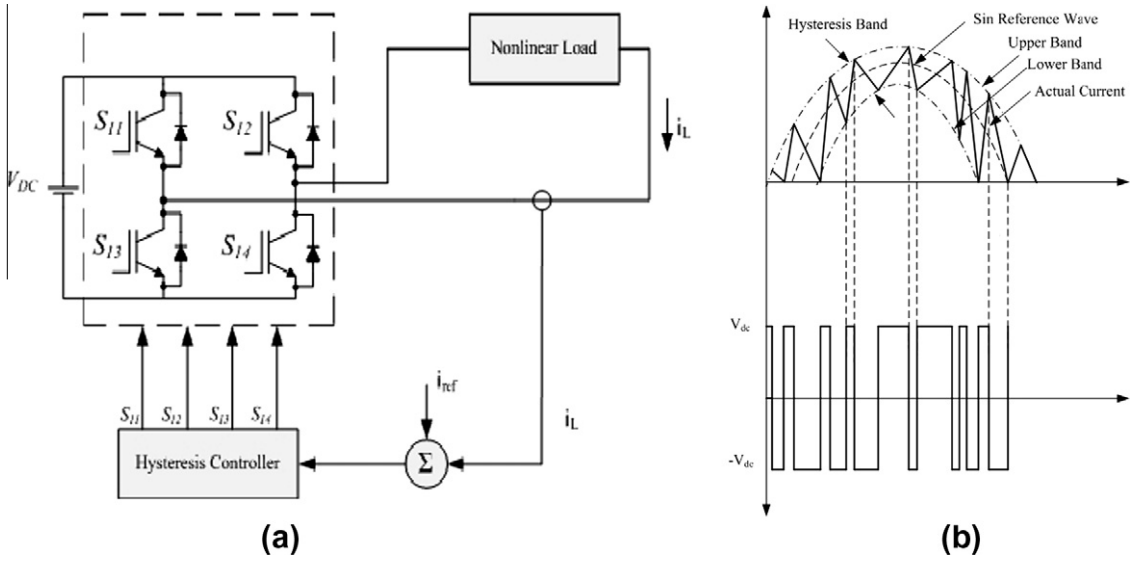

Fig. 18. Hysteresis current control: (a) block diagram of a H-bridge cell with hysteresis controller, (b) hysteresis current band and voltage curves of load feedback.

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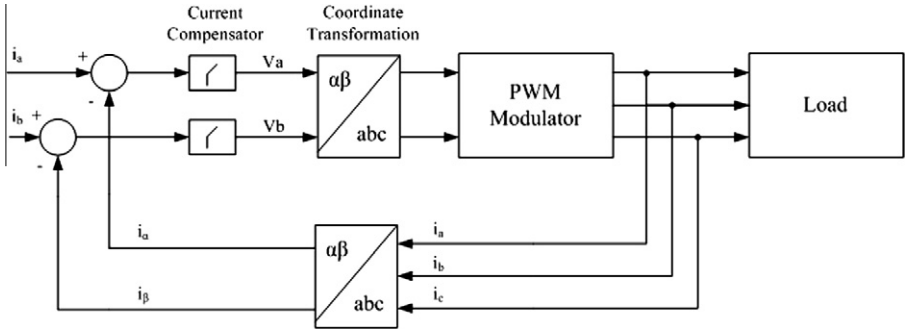

Fig. 19. The block diagram of stationary linear current controller.

Table 5
The most appropriate control scheme and application matching diagram according to topologies.

Topology	Control scheme			Application			
	SHE-PWM	SPWM	SVM	Motor drive	Active filters	PV, fuel cells	STAT COM
DC-MLI	✓✓	✓	✓	✓✓	✓	✓	✓
FC-MLI	✓	✓	×	✓	✓	×	×
CHB-MLI	×	✓✓	✓	✓✓	✓✓	✓✓	✓✓
H-MLI	×	✓✓	×	✓	✓	✓	✓
AH-MLI	×	✓✓	✓	✓✓	✓	✓✓	✓

been discussed for topologies and control schemes. DC-MLIs, especially three-level structure, have a wide popularity in motor drive applications besides other multilevel topologies due to reducing THD with robust control of SHE-PWM control scheme. However, it would be a restriction of complexity and pre-defined switching angles when the level exceeds the three. The SPWM and SVM modulation techniques succeed this limitation of DC-MLI for higher level topologies. Other applications of DC-MLI can be defined as active filters and STATCOM in high voltage grid interconnections. Table 5 illustrates the most appropriate control schemes with application matching according to selected multilevel inverter topology.

The sign of bolded check means the proper matching between topology and control scheme or topology and application. The plain checks have been used to emphasize that there are some studies given in the literature about these applications but does not provide proper solutions. The bolded double check shows the most appropriate selection, while the cross defines the undesirable matching about harmonic reducing or affectivity issues. The DC-MLIs are efficient in fundamental frequency switching applications such SHE-PWM and SVM, but the SVM will cause to an increment on voltage and current THD in the increased number of clamping diode conditions. The FC-MLI topology that has been introduced in 1992 is similar to DC-MLI except utilizing DC side capacitors instead of clamping diodes in a ladder form.

The FC-MLI is the unique topology that requires the most switching and auxiliary devices to generate a staircase output voltage. The increment of level will cause to increase auxiliary capacitor number and restrain the accurate charging and discharging control of capacitors, hence designer will be encountered with the requirement of a pre-charge controller system. Although these disadvantages, the most important advantages of FC-MLI topology are preventing the filter demand, and controlling the active and reactive power flow besides phase redundancies. The FC-MLI topology is mostly used in motor drive and active filter applications with SHE-PWM or phase shifted PWM control methods.

The CHB-MLI has the least components for a given number of levels according to topologies discussed before. The CHB-MLI topology consists of a series of H-bridge cells to synthesize a desired voltage from SDCSs which may be obtained from batteries or fuel cells. All these properties of cascade inverters allow using various pulse width modulation (PWM) strategies to control the inverter accurately. CHB-MLIs have been previously designed for static VAR compensators and motor drives, but the topology has been prepared an interface with renewable energy sources due to using separate DC sources. There are numerous studies have been performed on CHB-MLIs for connecting renewable energy sources with grid and power factor correction. The SPWM control scheme is mostly being used in the control of CHB-MLI due to simplified design considerations according to SVM.

5. Conclusions

Based on the survey of conventional multilevel inverter topologies given in the previous sections, general and asymmetrically constituted H-MLIs have been also reviewed in this paper. Many new hybrid topologies can be designed through the combinations of three main MLI topologies. Besides the combination of topologies, the trade-offs in MLI structures can be dealt by using AH-MLIs that is formed using different DC source levels in inverter cells. Nevertheless, conventional PWM strategies that generate switching frequency at fundamental frequency are not appropriate for AH-MLIs due to switching devices of the higher voltage modules would have to operate at high frequencies only during some inverting instants. To achieve this control strategy, hybrid modulation methods have been proposed that provide to get higher power cells switched at low frequency and low power cells switched with high frequency. The detailed researches show that the general idea of modulation strategies based on multi-carrier SPWM such as PD, POD, and APOD can be utilized for hybrid topologies.

Due to numerous applications of conventional MLIs and flexibility to design the hybrid MLI topologies, this paper cannot cover all utilizations with MLIs, but the authors intend to provide a useful basis to define the most proper control schemes and applications as depicted in Table 5. In addition to these, the fundamental design and control principles of MLIs have been introduced as a result of a detailed literature survey. This paper has been destined to provide

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a reference to readers and the results given in this paper can also be extended with experimental studies.

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