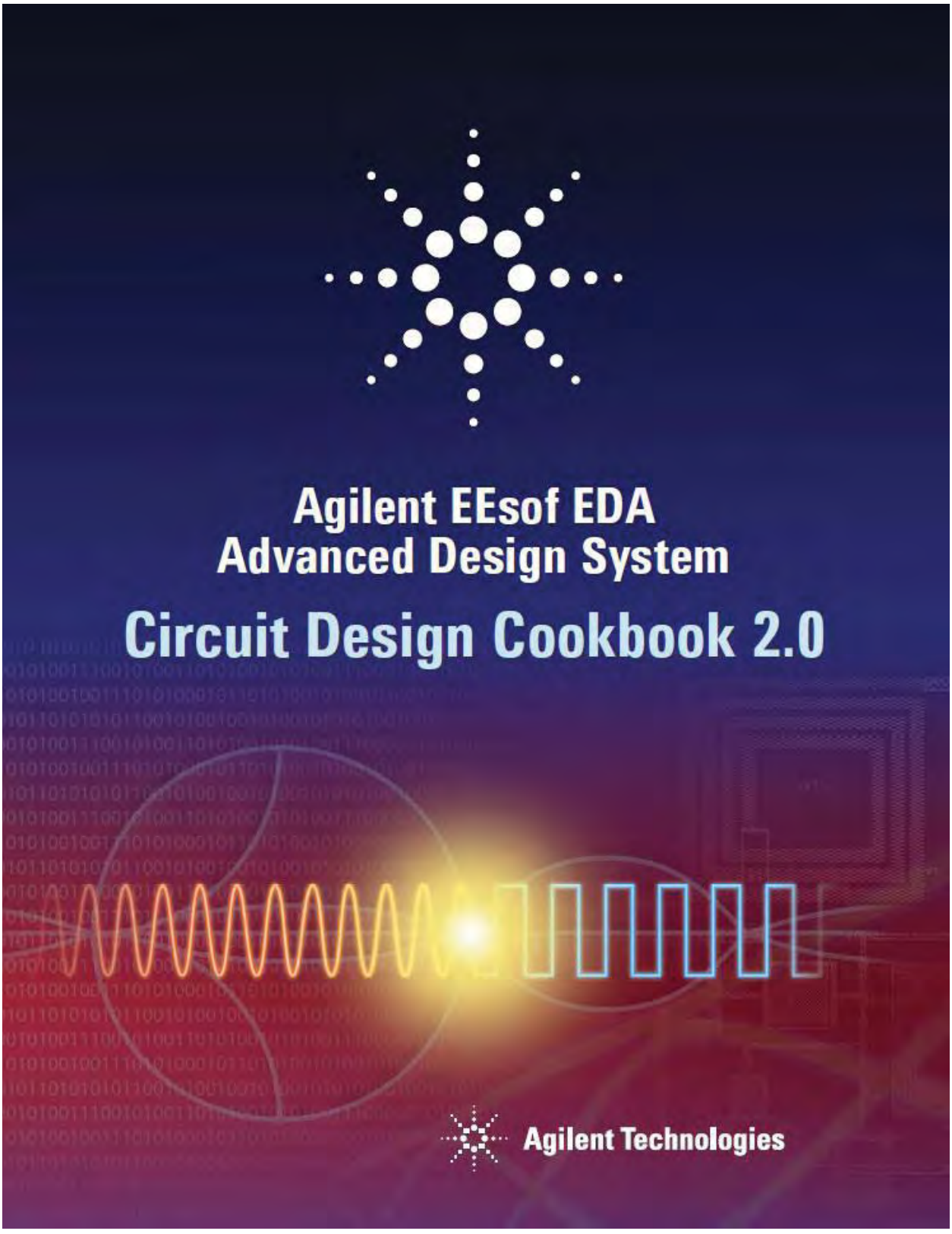

Agilent EEsof EDA
Advanced Design System
Circuit Design Cookbook 2.0
Agilent Technologies

ADS Circuit Design Cookbook 2.0

Contents:

Chapter 1: Getting Started with ADS 2011

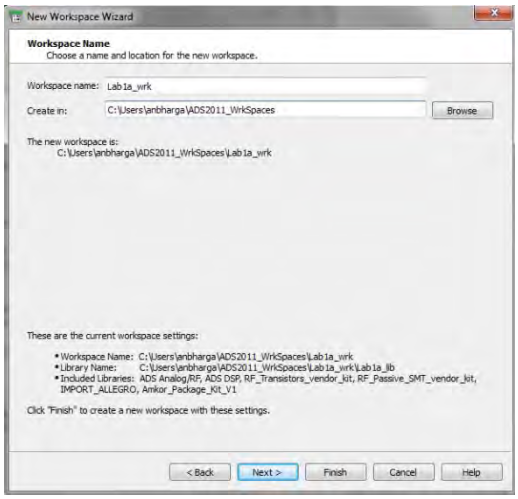
ADS Licenses Used:

- **Linear Simulation**

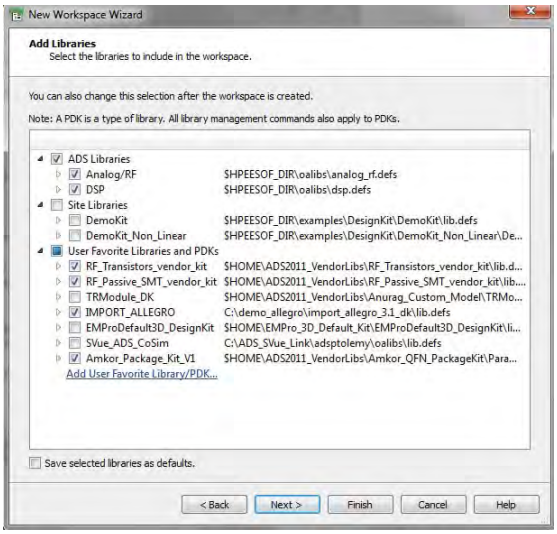
Chapter 1: Getting Started with ADS 2011

This tutorial provided getting started details to new users of ADS2011. ADS2011 organizes the design work in the form of workspace and we need to create a new workspace to begin the design work.

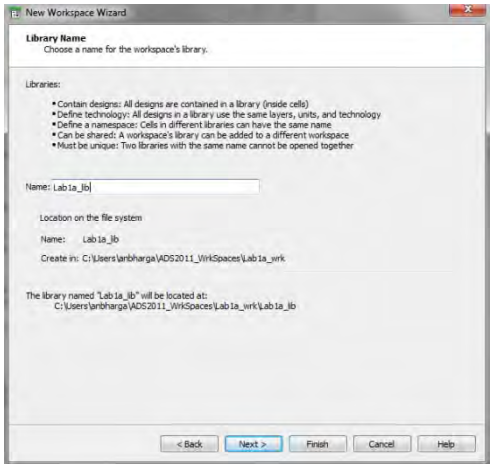
Step 1 - Creating Workspace:



1. Launch ADS2011 and from the main window select File->New-Workspace. Enter workspace name as desired, please note that workspace name and path to the workspace location should not contain any spaces. Click Next…

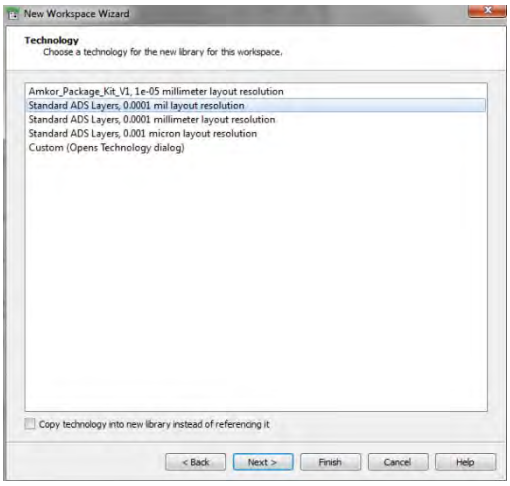


2. Select the libraries to be included in the workspace. ADS natively provide Analog/RF and DSP components library and it can be selected as needed in actual design work under the workspace. Component libraries provided in ADS can be added by clicking on the link Add User Favourite Library/PDK (all vendor component libraries are provided in zipped format under: **<ADS_install_dir>/oalibs/componentLib/ folder**)



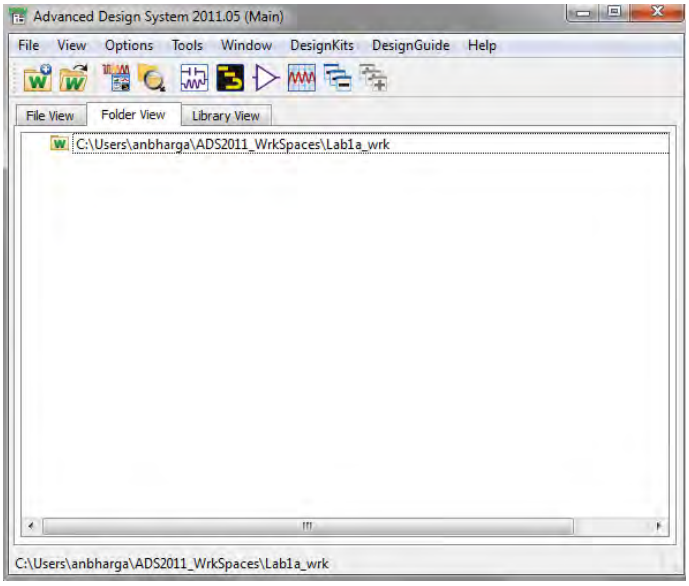
3. Provide the library name under which user would like to organize the work. This library is not to be confused with component vendor or 3rd party libraries. This is new way in which ADS2011 organizes the design schematics/layouts in a workspace and every workspace can contain multiple libraries in which we can organize our work consisting of multiple technologies e.g. GaAs, GaN, InP, SiGe etc. While we keep 1 library for each technology ADS2011 provides the capability to use these designs under a single main design to perform Multi-Technology designs. It may be noted that in ADS2011, schematic and layout units are also considered to different technologies and it is

recommended not to mix the units which we use in design. i.e. mil, mm, um etc. Click on Next.



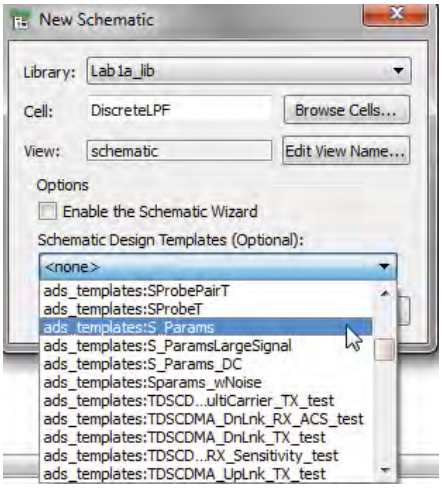
4. Select the preferred units to be used during the design. In present example we select mil with 0.0001 mil layout resolution.

5. Click on Next and see the summary of the workspace and click on Finish and blank workspace as shown below will appear and we are ready to create our schematic or layout designs in the newly created workspace.



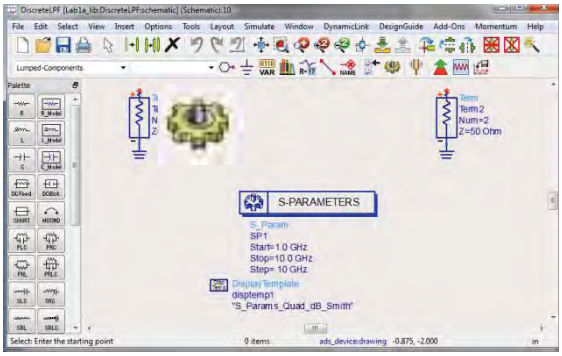
Step 2: Creating Schematic Design

Usually circuit design will start from the schematic entry. To start the schematic design we can begin from File->New->Schematic or by clicking on the Schematic icon on the main window toolbar.

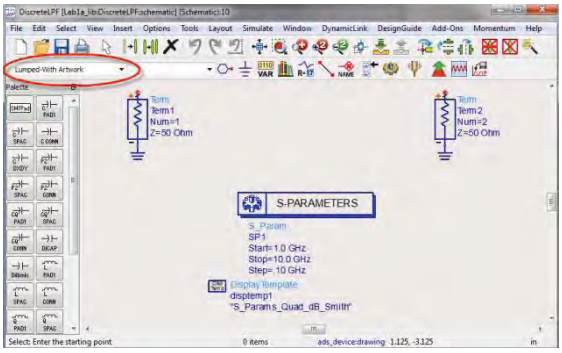


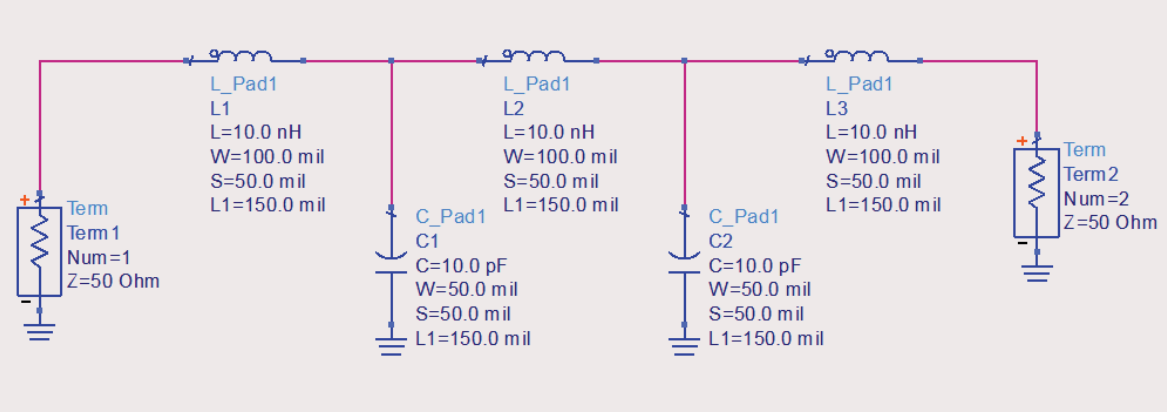
1. Enter the desired cell name (e.g. Discrete LPF) and select the Schematic Design Template as ads_templates: S_Params (for S-Parameter simulation). Selecting template is an optional step but it is good feature to have because it saves our effort of setting up the design for the simulation. Click OK…

2. A new schematic page with two 50-ohm terminations and a S-parameter controller placed on it with default frequency settings should be visible. If template was not selected during new schematic creation then we can placed required components for SP simulation by going to appropriate Simulation category e.g. Simulation-S_Param, Simulation-HB etc



3. Now let's start creating a circuit, go to **Lumped with Artwork** library as shown here, place **L_Pad** and **C_Pad** components on the schematic to form a Low Pass Filter Topology as shown in the figure below. L_Pad and C_Pad are normal inductor and capacitors but it also includes footprint information and designers can enter desired width, spacing and length of the component as per the component which might be used for actual PCB design.





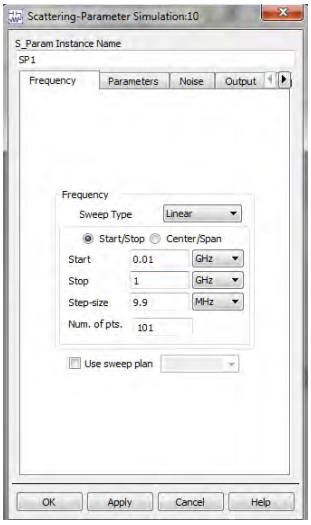
4. Double click on the S-Parameter controller and set the parameter as following:

   Start = 0.01 GHz

   Stop = 1 GHz

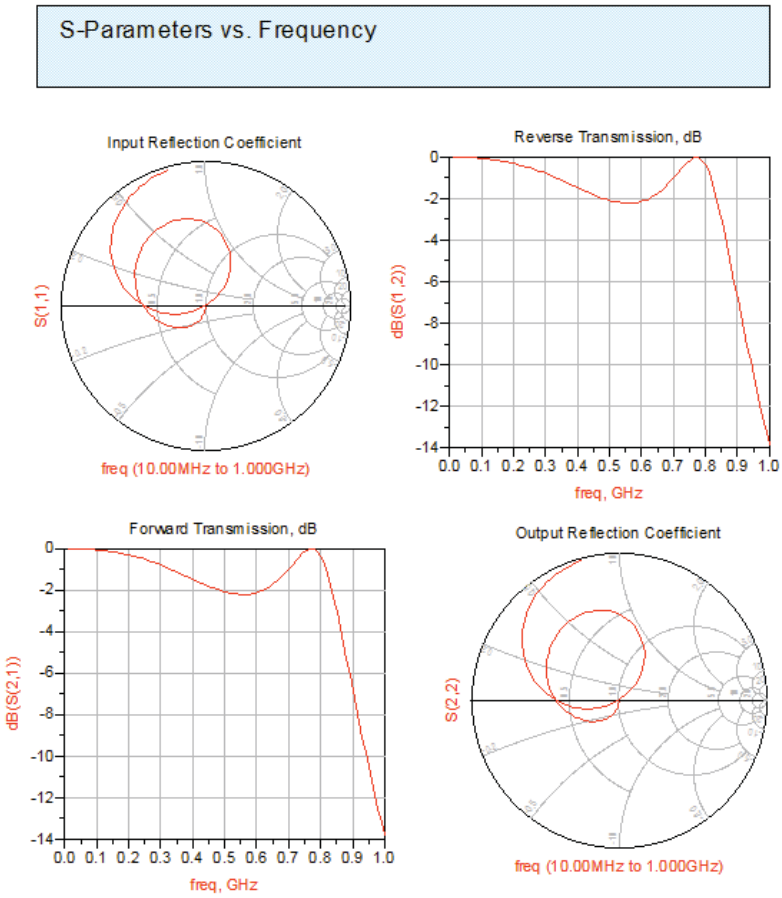
   Num. of points = 101 (step size will be automatically calculated)

   Click OK…

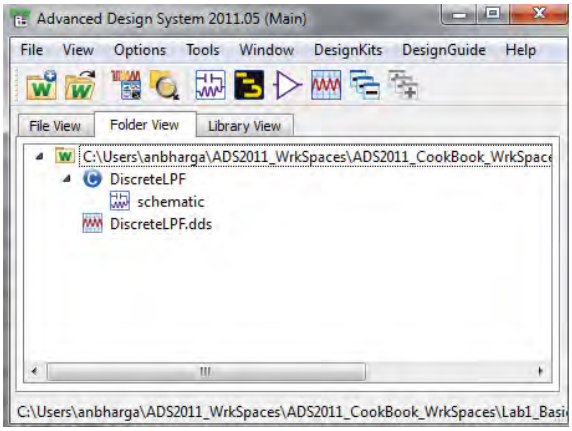


5. Click on Simulate icon (or press F7) to start the simulation

6. Once done, data display showing the simulation results as shown below



7. Save the design to save all the work and inspect the main window to notice the schematic cell and data display.



Chapter 2: Tuning and Optimization

ADS Licenses Used:

- **Linear Simulation**

Chapter 2: Tuning and Optimization

It is often the case that our manually calculated values do not provide the most optimum performance and it is needed to change the component values. This can be done in two ways: Tuning or Optimization

What is Tuning?

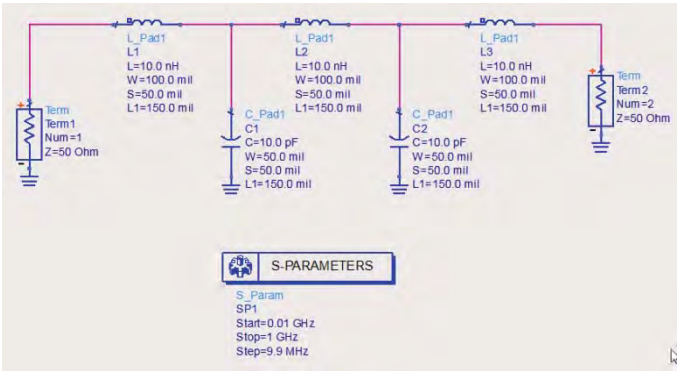
Tuning is a way in which we can change the component values and see the impact of the same on circuit performance. This is a manual way of achieving the required performance from a circuit which works well in certain cases

What is Optimization?

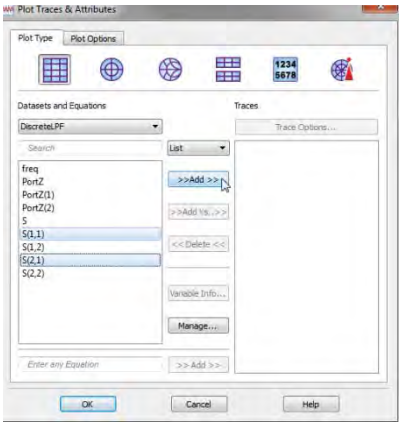
Optimization is an automated procedure of achieving the circuit performance in which ADS can modify the circuit component values in order to meet the specific optimization goals. Please note that care should be taken while setting up the goals to be achieved and it should be practically possible else it will not be possible to meet the goals. Also the component values which are being optimized should be within the practical limits and this needs to be decided by designers considering the practical limitations.

Performing Tuning in ADS 2011

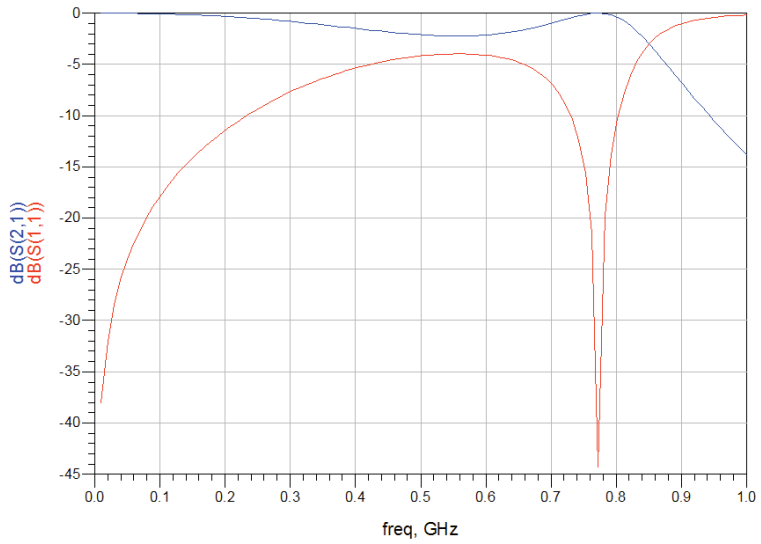
Let us take the LPF circuit example which we designed in Chapter 1 and tune the component values in order to improve the circuit performance



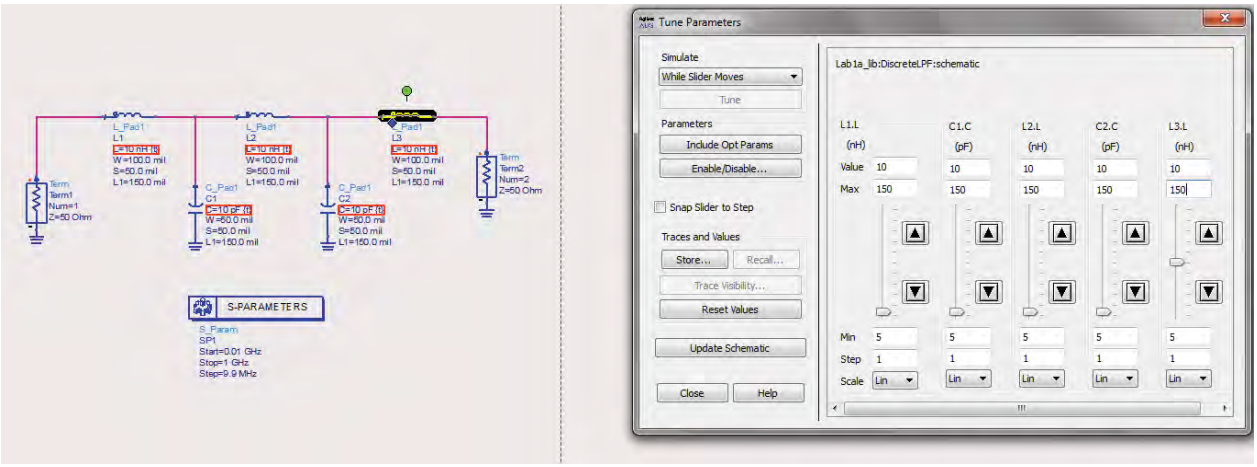
1. Open the LPF circuit as shown here. Delete the Display Template component and simulate it.
2. In the data display, delete all the plots and insert a new rectangular plot



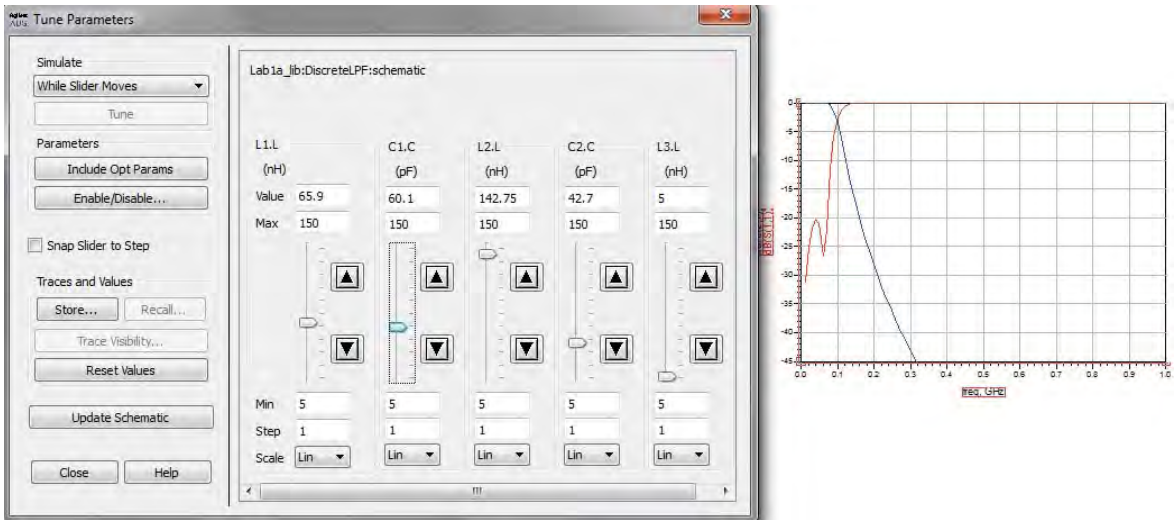
3. Click on the data display page and select S(1,1) and S(2,1) from the pop-up window and click on Add>> and select units as dB when prompted.
4. Click OK to see the data display as shown below



5. Click on the Tune Parameter icon in the schematic page 
6. We need to make component values tunable in order to see their impact on circuit performance. Click on inductance and capacitance **values of the components** in LPF circuit and it will added into the Tune wizard. If you click on component then you will get option to select "L" or "C" etc for tuning. Change the max values for all components to be 150 so that we have some decent range to tune the component values.



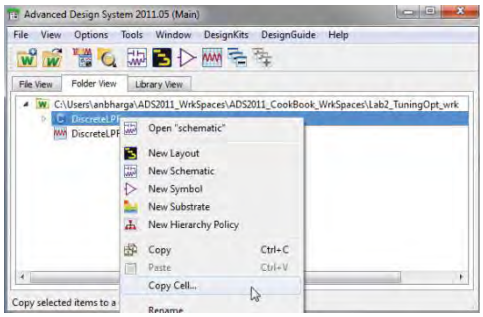
7. Put Tuning slider window and data display side by side and start to move the slider of component values and see the corresponding graph changing with the component values.



Please note there are many other features of Tuning wizard:

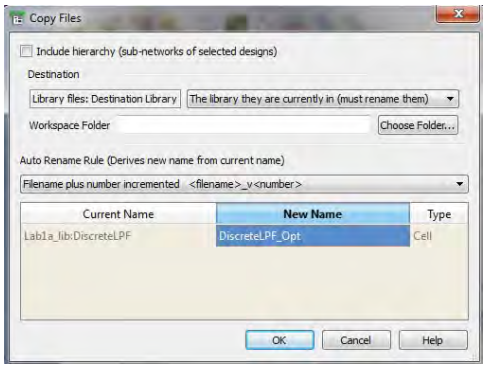
a. We can store temporary tuning states by clicking on Store icon so that we can save intermediate tuning conditions and revert back to any of the saved states by clicking on Recall button. These states will vanish once we close the wizard. Each saved state will result a freezed trace in the graph window
b. We can select “Snap Slider to Step” so that the slider changes in finite step size as mentioned in Step field below the sliders
c. Parameter values can be swept in Linear or Log format
d. We can Enable/Disable parameter to tune by clicking on Enable/Disable button.
e. If we have stored lot of intermediate states we can turn on/off few graphs for better visibility.

8. Once we have achieved the desired or best possible results we can click on **Update Schematic** button to update these tuning values on design schematic. If you accidentally click on Close the pop up window will appear checking whether you would like to update your Schematic or not.
9. Click Close button once you are done with the tuning and observe the component values in schematic and data display window for tuned response.



Performing Optimization in ADS 2011

Let us now see how optimization can be performed on this LPF circuit to achieve the desired performance without us needing to do manual work.

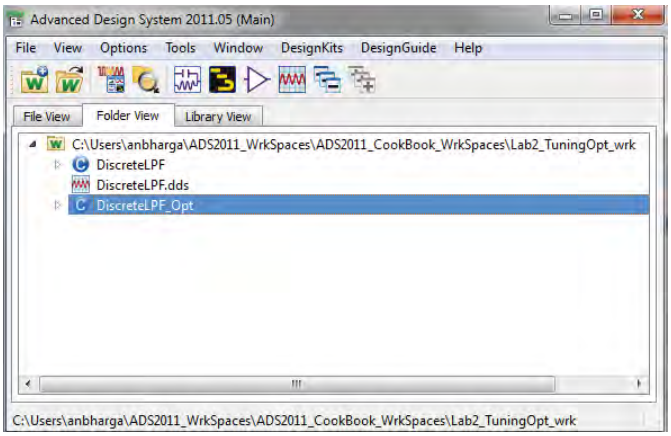


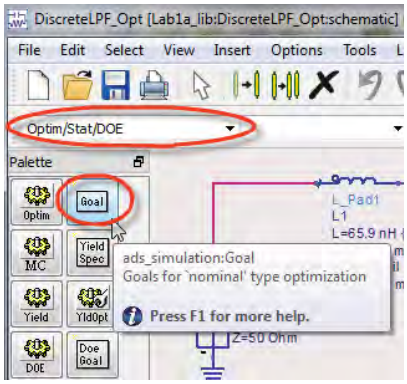
Optimization in ADS is a 3 step process:

a. Setting up Optimization Goals
b. Placing Optimization Controller and select type of optimizer and number of iterations
c. Make component values to be optimizable

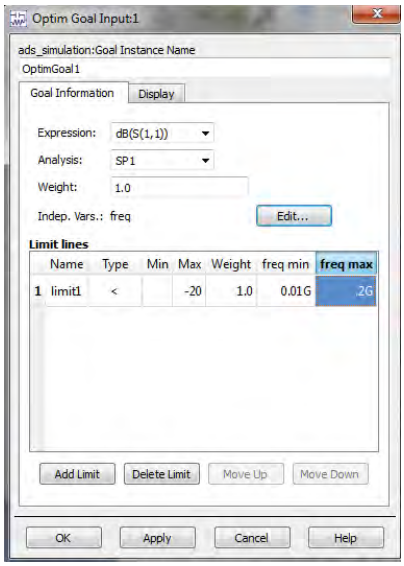
Let's make a copy of the tuning schematic cell so that we can perform optimization on the same and also compare the responses of our manually tuned schematic and ADS optimized schematic.

1. Go to the Main Window and right click on the Cell to be copied and select "Copy Cell".
2. A new pop window will appear and we can provide new name for this copied cell, let's call it DiscreteLPF_Opt. Please note that if the cell which is being copied is a hierarchal then we should option "Include Hierarchy…" and if our workspace has folders then we can place this copied into the specific folder by clicking on "Choose Folder". Click OK after you done with actions mentioned above.
3. Come back to the Main Window and observe that the cell is now copied and appears in the list with new name as we provided during copy process.





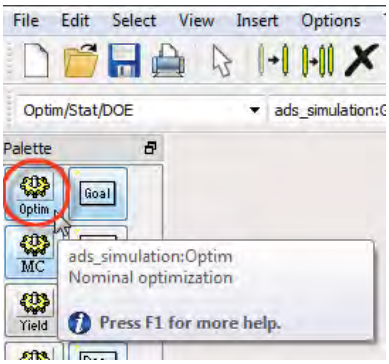
4. Open the schematic view of this newly copied cell.



A. Setting Optimization Goals:

1. Go to **Opt/Stat/DOE library palette** and place **Goal** component on Schematic as shown here
2. Double click on the Goal component and enter parameters as follows:
   a. Expression = dB(S(1,1)) (same as what is available on the Y-axis of the graph)
   b. Analysis = SP1 (name of the S-Parameter controller available in our schematic)
   c. Click on **Edit** in front of **Indep. Var** and click on **Add Variable** in the pop up window and enter **freq** as the variable name. ***freq*** *is the keyword for frequency which is our X-axis of the graph over which we will define this optimization goal.*
   d. Select **Limits->Type** as less than **(<)** and enter **-20**, this is to set dB(S(1,1)) to be better than -20 (dB is already defined in S(1,1) definition hence we don't need to define it again with -20
   e. Enter freq min as 0.01G (which is the start frequency as we set in the S-Parameter controller), Enter freq max as 0.2G (max freq upto which we would like to achieve this S11 goal)

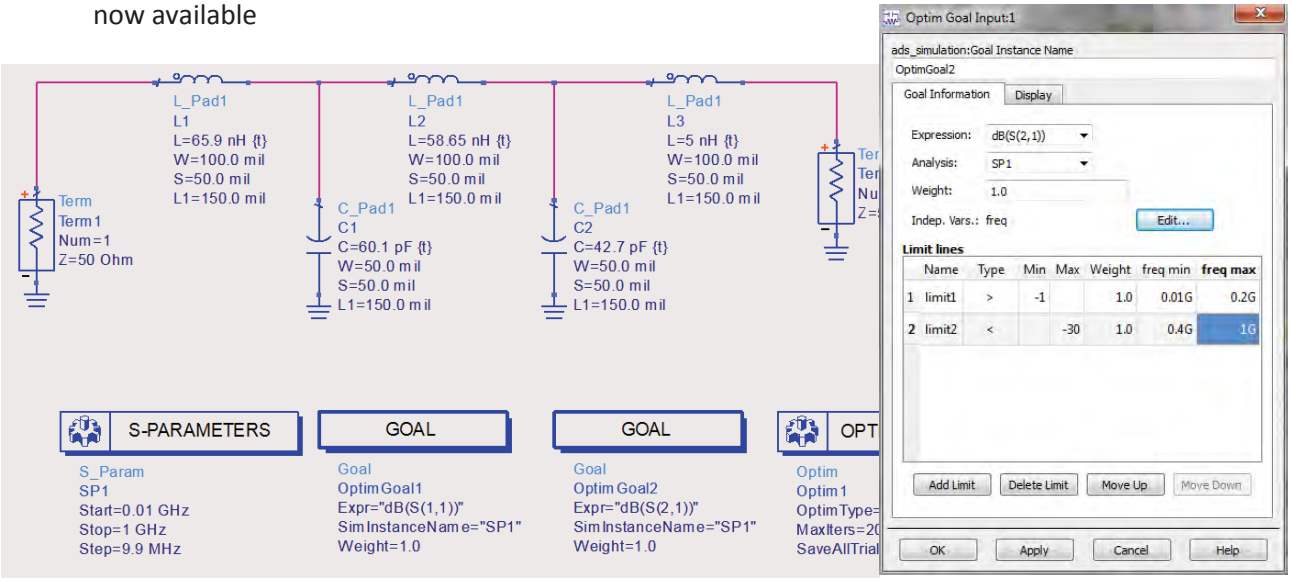
3. Place another Goal and let's define dB(S(2,1)) i.e. Transmission response to be optimized.



   a. Repeat the same steps as done in defining S(1,1) goal except for the fact that we can click on **Add limit** to define stop band criteria as well.
   b. In the **1st limit** (limit1) define the passband criteria as >-1 from freq min=0.01G to freq max=0.2G.
   c. In the 2nd limit (limit2) enter Type to be less than (**<**)-30 from **freq min=0.4G & freq max=1G** (max simulation frequency, should not be more than what is defined in S-Parameter controller)
   d. We can add more limits as may be desired for the circuit response, e.g. for a typical band pass filter we will have three limits for S(2,1) and that is 1st for the lower stop band condition, 2nd for the upper stop band and 3rd for the main pass band.
   e. Once done S(2,1) goal window will look like as shown here.

B. Setting up Optimization Controller

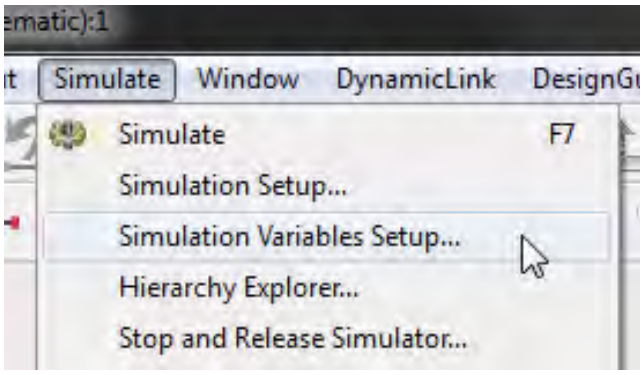
a. Place Optimization controller on the schematic from **Opt/Stat/DOE** library as shown here
b. Double click on the Optimization controller and set parameters as below:
   a. Optimization Type = Gradient
   b. Number of Iterations = 2000
c. Go to the **Display** tab and select "Clear All" which will make all options to be unchecked.
d. Select Optim Type and Max. Iteration options so that we will see only required options with this component in the schematic.
e. Click OK once done and schematic as shown below should be now available



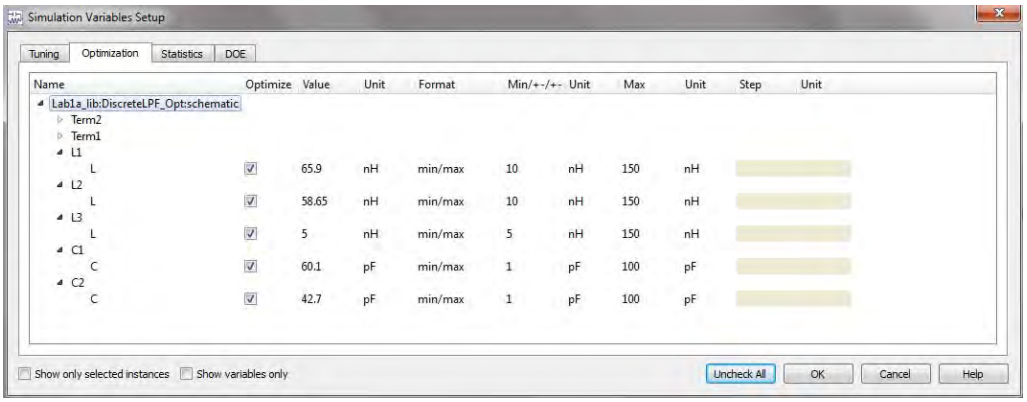
C. Defining Component Values as Optimizable

Last step remaining for us to start the optimization is to set the component values as optimizable which will be changed by ADS during the optimization process.

1. Go to Simulate->Simulation Variables Setup…



2. Click on Optimization Tab in the variable setup window (this variable window is a single place where we define components to be tunable, optimizable or set their tolerances for Statistical analysis)



3. Select all the “L” and “C” values to Optimize and set their min and max as per your own convenience (make sure that the value limits are realistic). We can also choose other Formats for defining range of component values as shown below. **Click OK….**

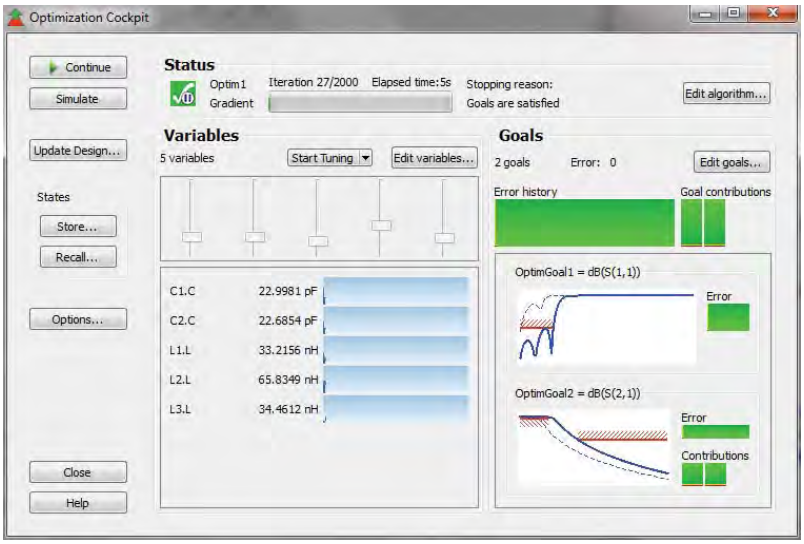
Optimizing the Design

1. Click on the Optimize button  on the schematic toolbar (next to Tune icon)

2. Optimization Cockpit window will open and we can see the circuit being optimized and component values are being changed in order to meet the required goals which we have set on schematic. Optimization takes 27 iterations (your case may be different as it depends on

what was the response of your circuit from where you started optimization) to meet the goals as we desired and optimization process will stop as soon as our goals are met else it will continue until we reach max iteration limits. If we reach the max iteration limits before we meet the goals we should inspect following:

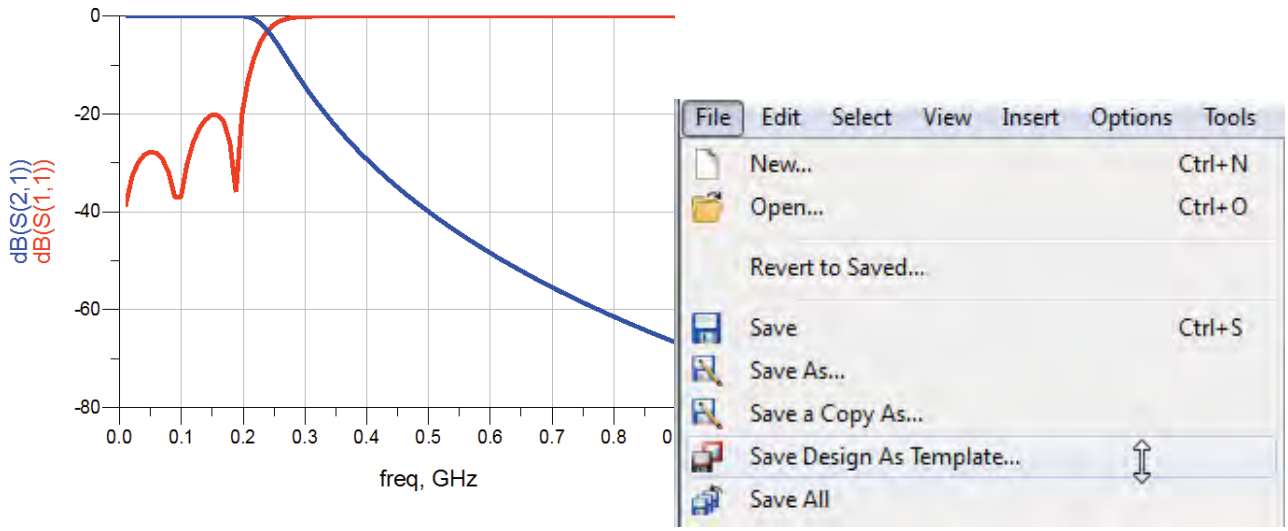
a. Whether Goals are realistic?
b. Are we close to the components min or max value (sliders will indicate that)?
c. If we are reaching min and max limits of component values then we can click on Edit variable and change the min/max if possible.
d. We can increase number of iterations by clicking on Edit Algorithm
e. We can modify the goals setting by clicking on Edit goals….



There are many other exciting features in this optimization cockpit as mentioned earlier whereby we can pause the optimization, tune the values ourselves, Edit Goals on the fly etc…..try exploring these options at your convenience.

3. Click Close and select “Update the Design” option when prompted.
4. Plot the graph for S11 and S21 on the data display and check the circuit performance against our goals. We can place markers on these traces using either the Marker toolbar on data display or by going to Marker menu.

Marker Toolbar: 



5. Save all your work by going to **File->Save All** from the ADS Main Window.

Note:

Optimization Goals setup involving Optimization Goals and Controller can be placed on a new blank schematic and then we can save it as our own template by going **to File->Save Design as Template** so that we can save our effort in setting up these things in future designs.

This template can be inserted to any new design and under any workspace by going to **Insert->Template** and then selecting the template which we might have saved earlier.

Please note that optimization variables will be different in every design hence we need to redefine the component values to be optimizable and set their limits.

Also, the goals specifications may need to be altered as per the desired specs.

Just remember that each and every setup can be saved as template for future use in ADS including the data display (which can be inserted in the data display page using Insert->Template option).

Chapter 3: Harmonic Balance Simulation

ADS Licenses Used:

- **Non-Linear Simulation (HB)**

Chapter 3: Harmonic Balance (HB) Simulation

Harmonic Balance Basics:

Harmonic balance is a frequency-domain analysis technique for simulating distortion in nonlinear circuits and systems. It is well-suited for simulating analog RF and microwave problems, since these are most naturally handled in the frequency domain. You can analyze power amplifiers, frequency multipliers, mixers, and modulators etc, under large-signal sinusoidal drive.

Harmonic balance simulation enables the multi-tone simulation of circuits that exhibit inter-modulation frequency conversion. This includes frequency conversion between harmonics. Not only can the circuit itself produce harmonics, but each signal source (stimulus) can also produce harmonics or small-signal sidebands. The stimulus can consist of up to 12 non-harmonically related sources. The total number of frequencies in the system is limited only by such practical considerations as memory, swap space, and simulation speed.

The harmonic balance method is iterative. It is based on the assumption that for a given sinusoidal excitation there exist a steady-state solution that can be approximated to satisfactory accuracy by means of a finite Fourier series. Consequently, the circuit node voltages take on a set of amplitudes and phases for all frequency components. The currents flowing from nodes into linear elements, including all distributed elements, are calculated by means of a straightforward frequency-domain linear analysis. Currents from nodes into nonlinear elements are calculated in the time-domain. Generalized Fourier analysis is used to transform from the time-domain to the frequency-domain.

The Harmonic Balance solution is approximated by truncated Fourier series and this method is inherently incapable of representing transient behavior. The time-derivative can be computed exactly with boundary conditions, v(0)=v(t), automatically satisfied for all iterates.

The truncated Fourier approximation + N circuit equations results in a residual function that is minimized.

N x M nonlinear algebraic equations are solved for the Fourier coefficients using Newton's method and the inner linear problem is solved by:

- Direct method (Gaussian elimination) for small problems.
- Krylov-subspace method (e.g. GMRES) for larger problems.

Nonlinear devices (transistors, diodes, etc.) in Harmonic Balance are evaluated (sampled) in the time-domain and converted to frequency-domain via the FFT.

How to Use Harmonic Balance Simulation:

For a successful HB analysis:

1. Add the *HarmonicBalance* simulation component to the schematic and double-click to edit it. Fill in the fields under the Freq tab:

- Enter at least one fundamental frequency and the number (order) of harmonics to be considered in the simulation.

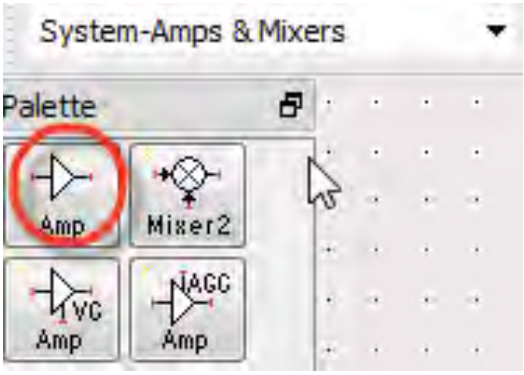
Make sure that frequency definitions are established for all of the fundamentals of interest in a design. For example, mixers should include definitions for RF and LO frequencies.

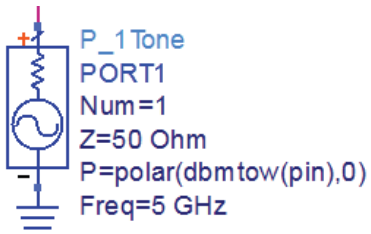
- *If more than one fundamental is entered, set the maximum mixing order. This limits the number of mixing products to be considered in the simulation. For more information on this parameter, see "Harmonics and Maximum Mixing Order" section under ADS HB Simulation documentation.*

- You can use previous simulation solutions to speed the simulation process. For more information, see "Reusing Simulation Solutions" under ADS documentation of Harmonic Balance.
- You can perform budget calculations as part of the simulation. For information on budget analysis, see the chapter "Using Circuit Simulators for RF System Analysis" in the *Using Circuit Simulators* documentation.
- You can perform small-signal analysis. Enable the *Small-signal* option and fill in the fields under the Small-Sig tab. For details, see Harmonic Balance for Mixers.
- You can perform nonlinear noise analysis. Select the *Noise* tab, enable the *Nonlinear noise* option, and fill in the fields in the Noise(1) and Noise(2) dialog boxes.
- If your design includes NoiseCon components, select the *Noise* tab, enable the *NoiseCons* option and fill in the fields.
- If your design includes an OscPort component, enable Oscillator and fill in the fields under the Osc tab. Harmonic Balance for Oscillator Simulation focuses specifically on simulating oscillator designs.

Lab: HB Simulation Flow

1. Create a new workspace with name Lab2_HBSimulation_wrk.
2. Create a new Schematic Cell (name it as SystemAmp) and place **Amp** model from **System-Amps and Mixers** library on the schematic.
3. Double click on the Amp component and set the Amplifier model parameters as below:
   - S21 = dbpolar(20,0)
   - S11 = dbpolar(-20,0)
   - S22 = dbpolar(-20,180)
   - S12 = dbpolar(-35,0)
   - TOI = 20
4. Place P_1Tone source from **Sources-Freq Domain** library and set its parameters as below;
   - P = polar(dbmtow(pin),0)
   - Freq = 5 GHz

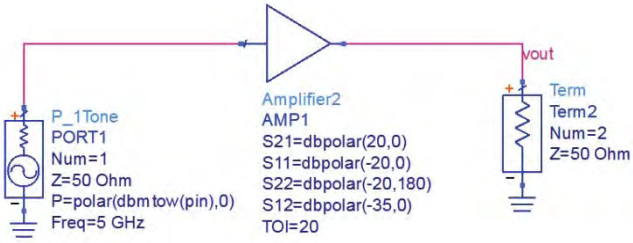


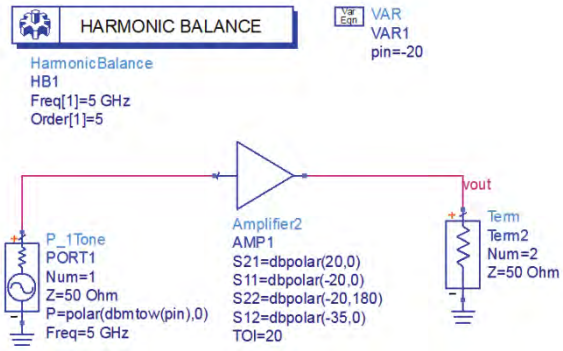


dbmtow() is a function which converts the dBm power which we enter in the source to watts for internal calculation purposes.

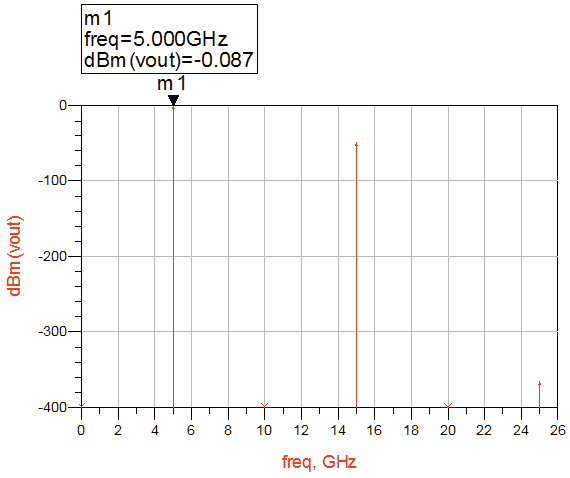
5. Place **Term** component from **Simulation-HB** palette library after the Amplifier and make connections as shown.
6. Click on **Wire Label** 

icon, enter the name as **vout** and click on the Term component's "+" pin as shown in the snapshot here.
7. Place HB simulation controller from **Simulation-HB** library palette and set Freq = 5GHz (same as defined in the 1-Tone source)
8. Click on **VAR** icon on the toolbar and define new variable as **pin** and its value as -**20**
9. Once done, schematic will look as shown below





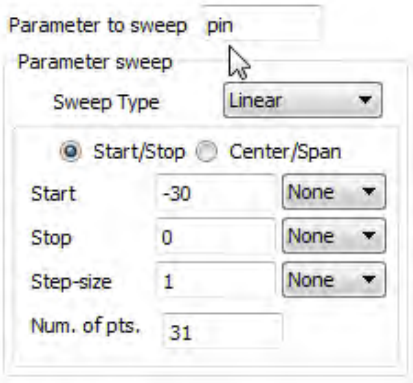
10. Run simulation and plot a graph in data display and select vout from the available list and select units as "Spectrum in dBm" and observe the data display as shown below



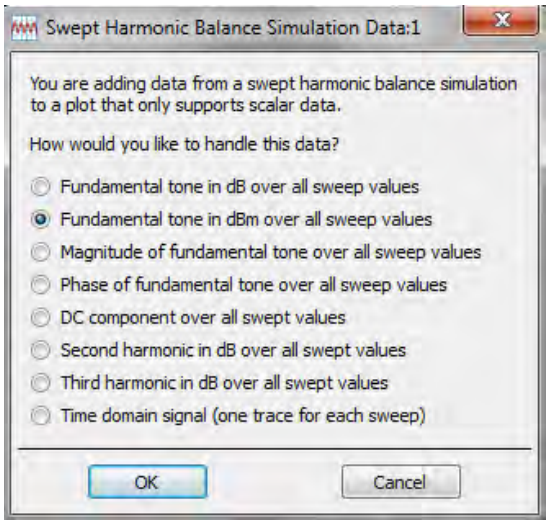
Lab: Power Sweep Simulation

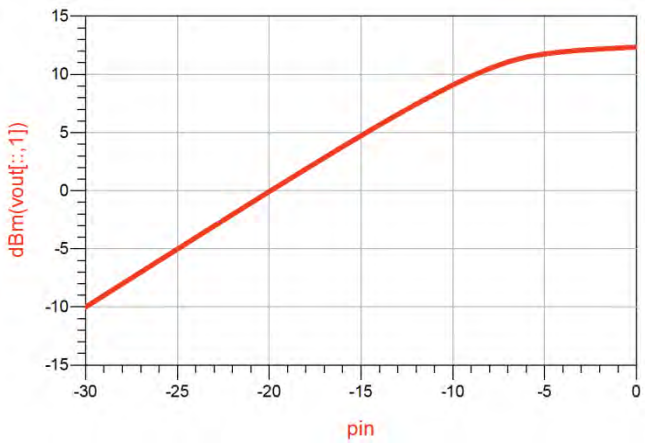
1. Make a copy of the cell, by right clicking on the existing cell and select Copy Cell.
2. Give a new name, e.g. SystemAmp_PSweep
3. Open the schematic of this copied cell and double click on the HB Simulation controller
4. Go to Sweep Tab and enter Parameter to Sweep = **pin**
    - **Start = -30**
    - **Stop = 0**
    - **Step-size = 1**

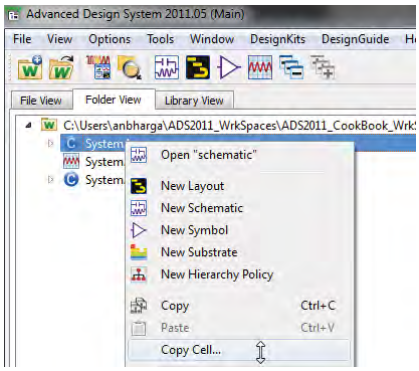
This setting states that we will sweep pin (input power) from -30 dBm to 0 dBm in a step of 1 dBm



5. Run simulation and insert a new Rectangular plot and select “vout” to be plotted, select “Fundamental tone in dBm over all sweep values”. Observe the data display as shown here

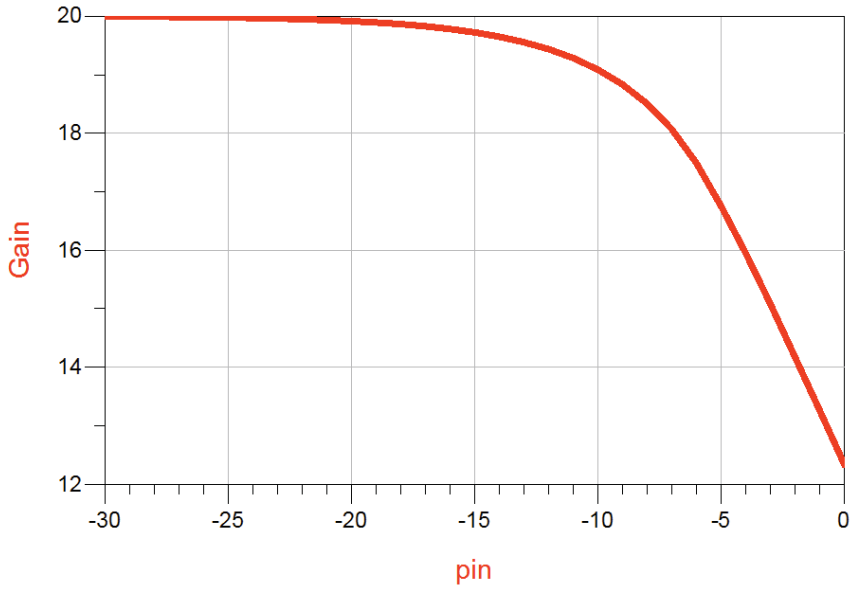






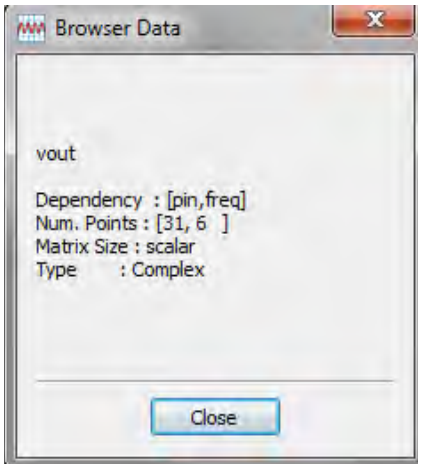
6. Insert a Eqn on data display and enter a equation for calculating gain curve of the amplifier:
   - Gain = dBm(vout[::,1]) – pin
   - Insert a new rectangular plot and click on Datasets and Equations drop down menu, select Equations
   - Select Gain (or whatever name was given in equations)
   - Click OK to plot the Gain response as shown below

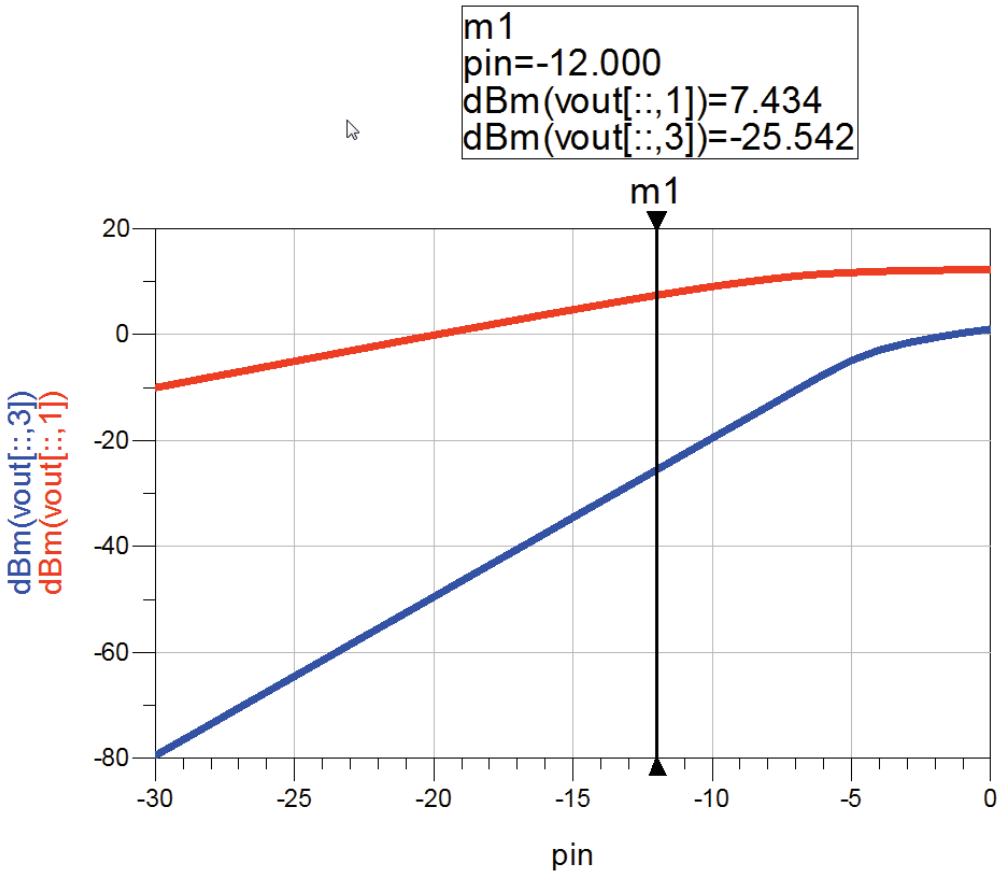
Eqn Gain=dBm(vout[::,1])-pin



Notes:

1. Spare some time to think about Y-axis value dBm(vout[::,1]). Data available at vout is 2-dimensional array, with 1st argument being swept power (pin) and 2nd argument being frequency tones (5 harmonics as selected in HB controller i.e. Order=5).
2. In order to get more clarity on the array indexing, double click on the graph and select **vout** and click on Variable Info button to see details of the data available at **"vout"** node as shown here
3. Add vout on the graph like we did earlier and select the same option of adding fundamental tone in dBm on all sweep values…
4. Now 2 traces should be visible on the graph, click on the Y-axis label for one of the graphs and it will turn editable, change the label as dBm(vout[::,3]) to see traces of fundamental frequency and 3rd harmonic alongwith fundamental.
5. Place a Line Marker to see values of the traces. Note the slope of the fundamental and 3rd harmonic (3 times higher than fundamental)





Chapter 4: Planar Electromagnetic (EM) Simulation in ADS 2011

ADS Licenses Used:

- **Linear Simulation**
- **Momentum Simulation**

Chapter 4: Planar Electromagnetic (EM) Simulation in ADS

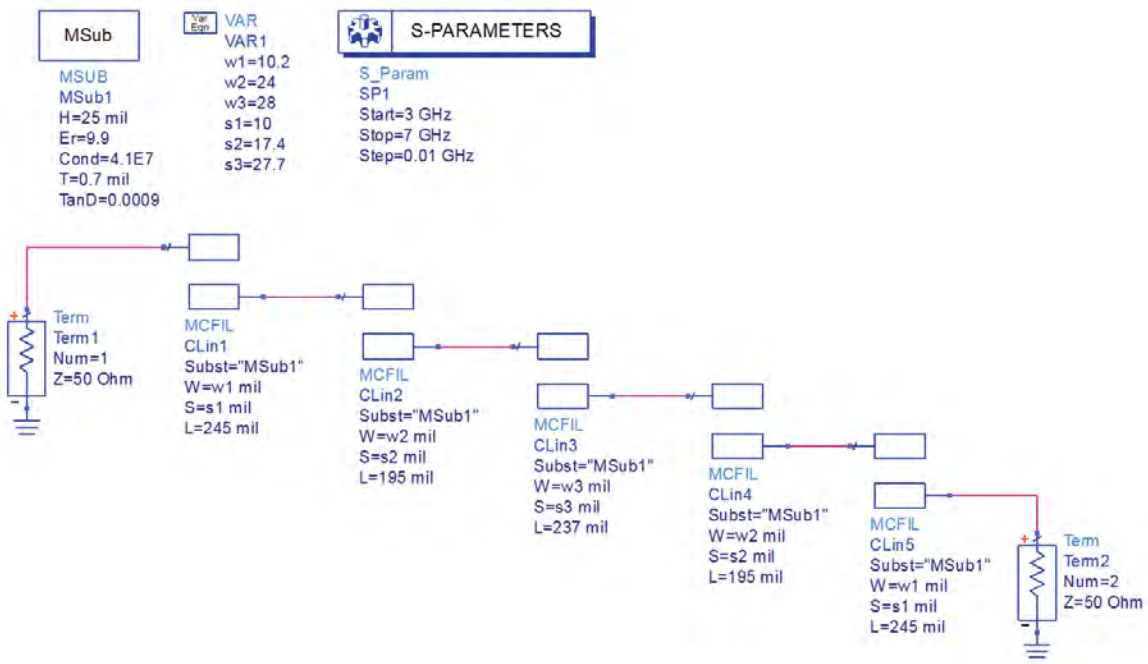
Agilent ADS provides two key electromagnetic simulators integrated within its environment making it convenient for designers to perform EM simulations on their designs. Unlike circuit simulators, EM simulators are used from layout.

This chapter illustrates the flow which can be used to perform EM simulations as needed by designers using ADS2011 (& beyond) release.

Case Study 1: Microstrip Bandpass Filter

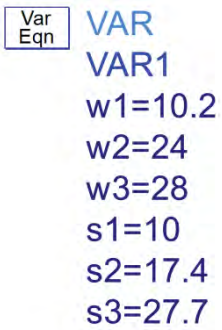
Step 1: Creating the Schematic Design for BPF

Create a new workspace and select units as **"mil"**. Create a new schematic cell and place components for coupled line bandpass filter topology as shown below.



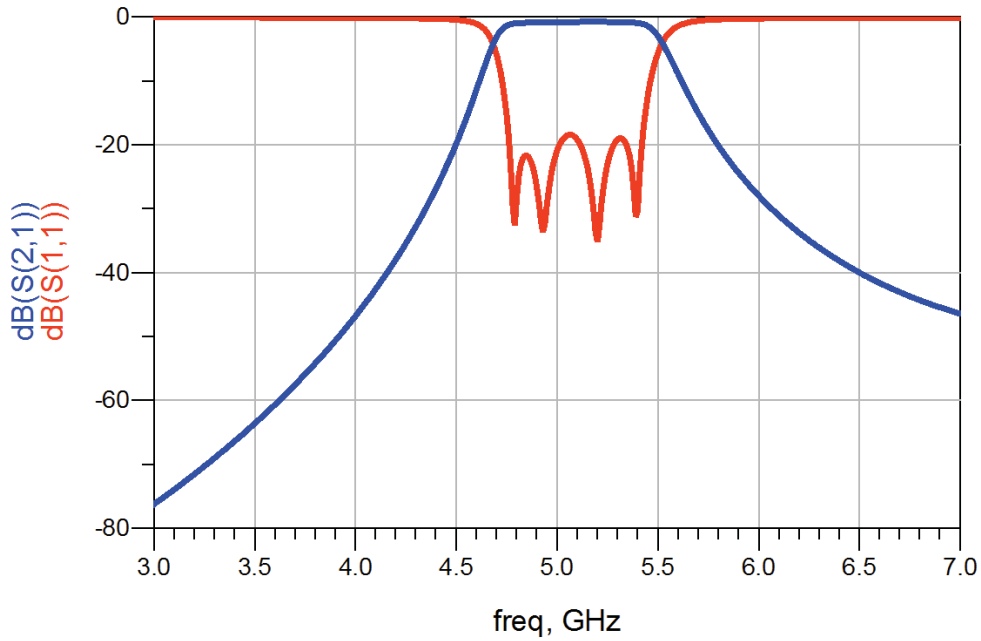
In order to prepare this 5-section Coupled Line BPF, do following:

1. Place **MCFIL** (Coupled Filter Section) from **TLines-Microstrip** library palette.
2. Place a **VAR** block and enter w1, w2, w3, s1, s2, s3 variables with values as shown here.
3. Modify the values in MCFIL components to reflect these variable values for W and S parameters (please note that units are in mil)
4. Define lengths for MCFIL components as below:
    a. 1st and 5th section: 245 mils
    b. 2nd and 4th section: 195 mil
    c. 3rd (center) section: 237 mil



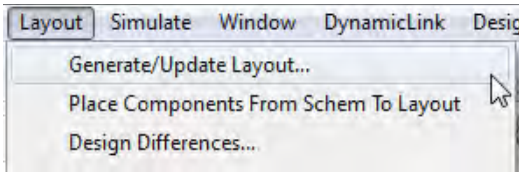
5. Define a microstrip substrate(MSUB) with following values:
    a. H=25 mil (Height of the dielectric)
    b. Er=9.9 (Relative Dielectric constant)
    c. Cond=4.1E7 (Metal Conductivity, in this case it is set for Gold)
    d. T=0.7 mil (Metal Thickness)
    e. TanD=0.0009 (Loss Tangent)

6. Place two 50-ohm terminations (**Term**) components at input and output from **Simulation-S_Param** library palette
7. Place SP controller from **Simulation-S_Param** library palette and its frequency as **3 GHz – 7 GHz with step size of 0.01 GHz**
8. Run simulation and observe the results and it should be similar to the one shown below

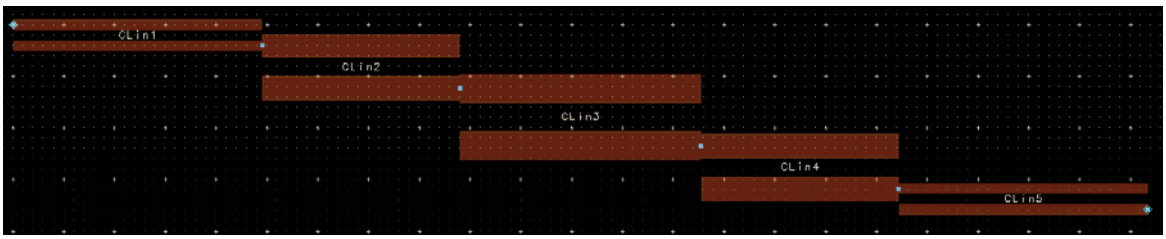


Step2: Creating the Layout from Schematic

Create the layout from schematic by going to **Layout->Create/Update Layout** and click OK on the pop-up window



Once done, layout as shown below should be available and layout view will be added in the view list under the cell name and same can be verified the ADS Main Window.



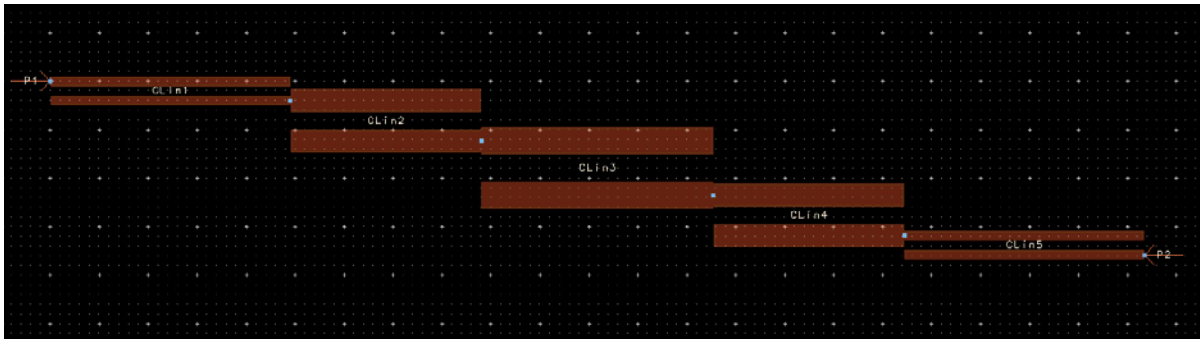
Step3: Setup and run EM simulation

To run EM simulation it is need to setup the required things properly. Basic steps involved in running proper EM simulation are as below:

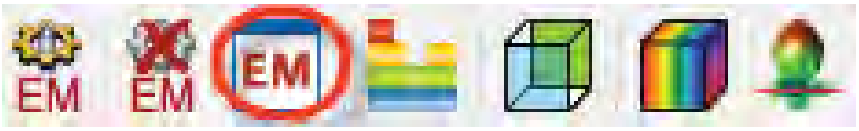
1. Connect Pins in layout which then will be defined as Ports in the EM setup window (please note that we don't need to convert Pins to Ports where we don't need to see the results to reduce the simulation dataset size)
2. Selecting the right simulator – Momentum (Method of Moments) or FEM (Finite Element Method)
3. Define the proper substrate definition
4. Define the simulation frequency plan
5. Define the conductor meshing properties
6. Create EM Model & symbol – This is an optional step and it can be left out if it is not needed to run EM-Circuit cosimulation i.e. to combine discrete components along with layout (this feature is explained in subsequent text)

Let us now begin the EM simulation setup as described above:

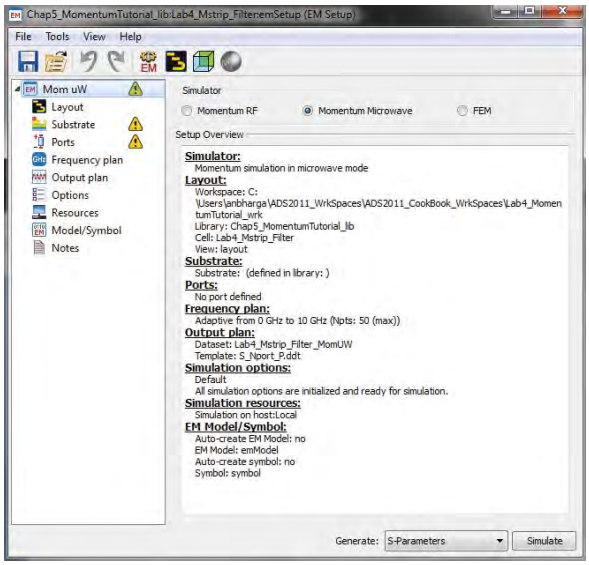
1. Connect the Pins at input and output side of the filter structure



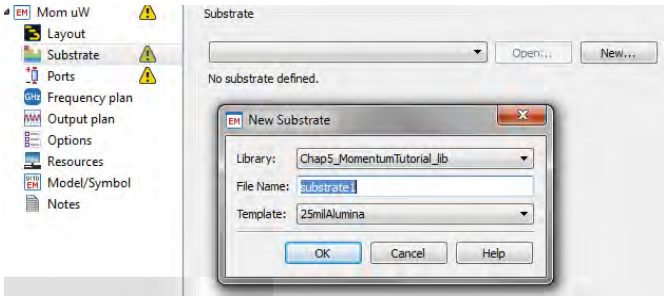
2. Click on the **EM setup** from the EM simulation toolbar on layout page as shown below



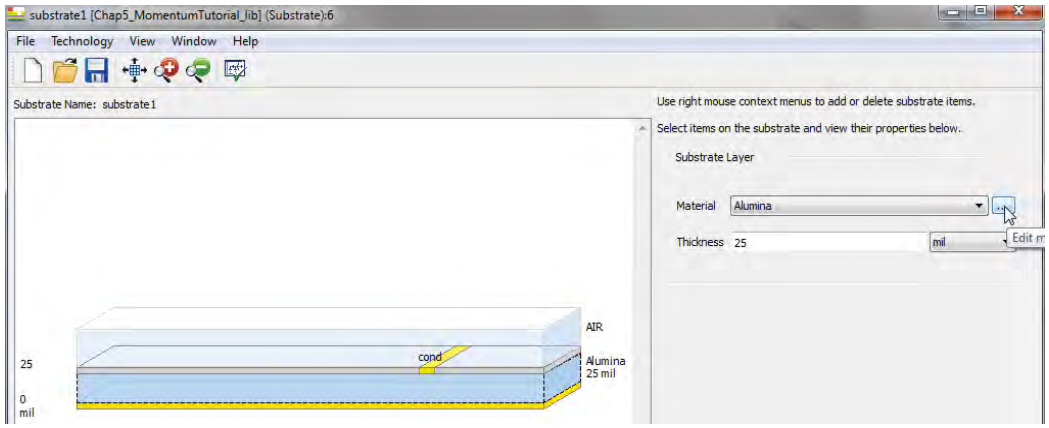
   a. EM setup window as shown below would appear and you can note the ⚠ indicating that there is something missing from the setup and you hover the mouse over it will complain about the substrate because we haven't defined the substrate yet.



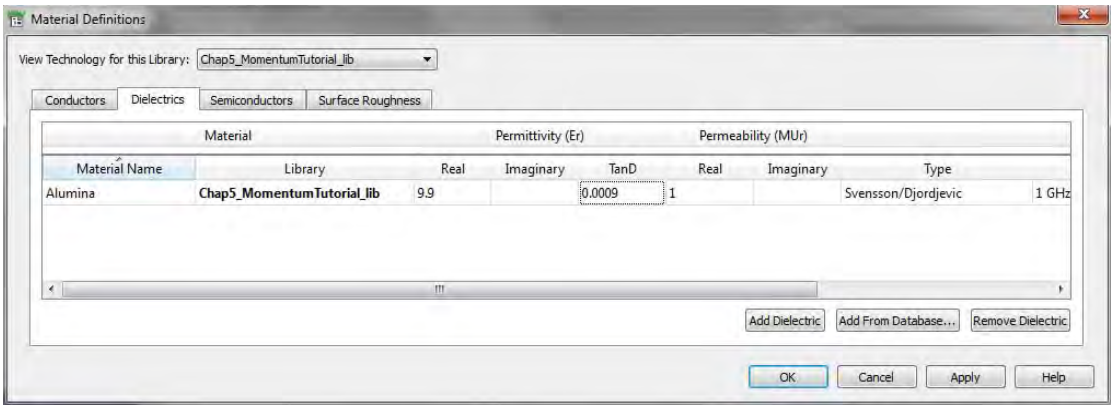
b. Click on the **Substrate option** and click on New and click OK to accept **25 mil Alumina template** and we can modify the properties of the same to suit our applications.



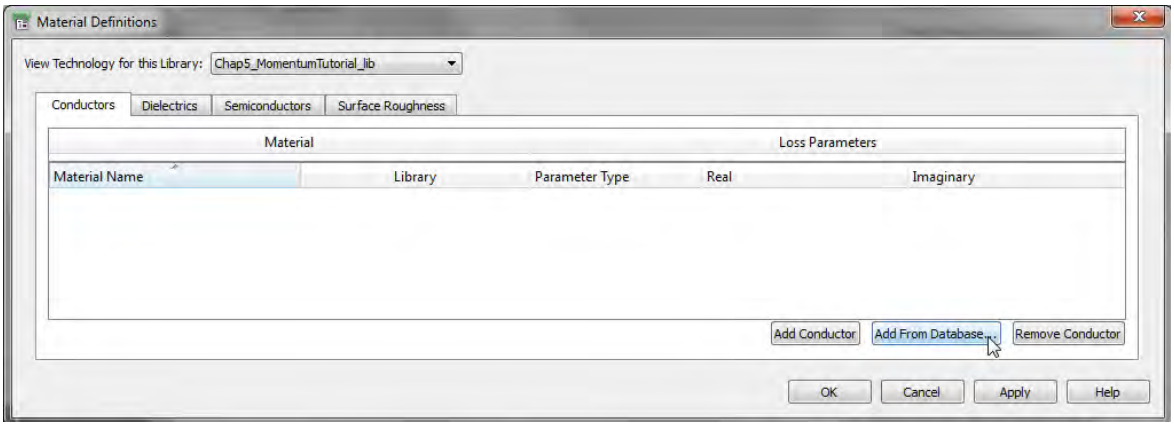
c. Once we click OK substrate editor as shown below will be opened, click on the Alumina dielectric and click on the **…. button** as indicated by the mouse cursor in snapshot below



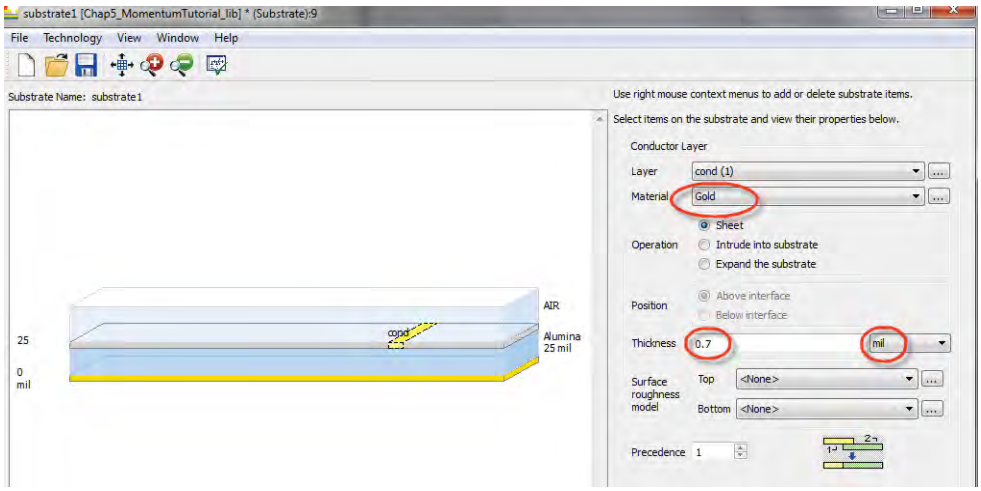
d. In the pop window, modify the Alumina characteristic to have Er=9.9 and TanD=0.0009 which is same as we used in schematic design



e. Click on the Conductors tab, go to Add from Database and select Gold from the list and click OK.



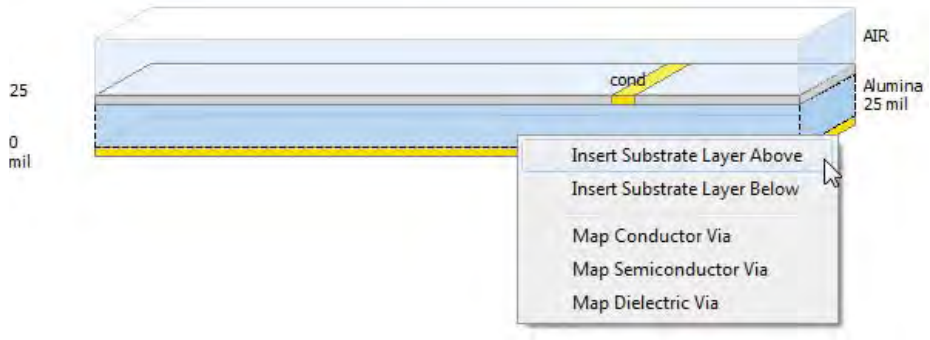
f. Click **OK** once done defining the dielectric and conductor properties, from the main substrate definition window, click on **cond** from the graphic window and select **Gold** from the Material list and define the thickness as **0.7 mil**



Please note: cond is defined as Sheet for Thick conductor you can select Intrude into substrate or Expand the substrate. If it is defined as Sheet then we need to use Edge Mesh as defined in point (5) later. Edge Mesh can be ignored if we are defined conductor as Thick conductor.

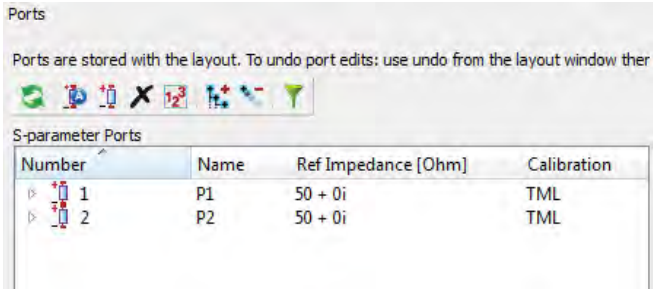
g. Click **Save** and close the substrate editor window once substrate is defined properly.

Note: ***Please note that we can add more dielectric layers, Via etc by right click on the graphics in the substrate editor window***

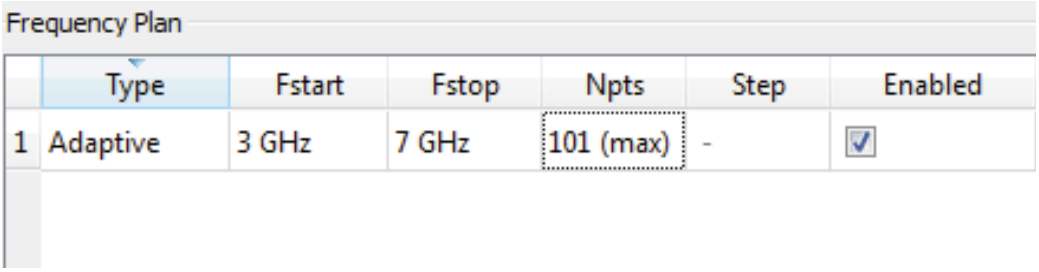


h. **Now the EM setup window should not have any** ⚠ mark visible. If you still see it, try hovering the mouse over it to see what mistake was done while following the steps above.

3. Click on **Ports** in the **EM setup** window to inspect that there are 2 ports defined (1 for each pin placed in layout) as shown below



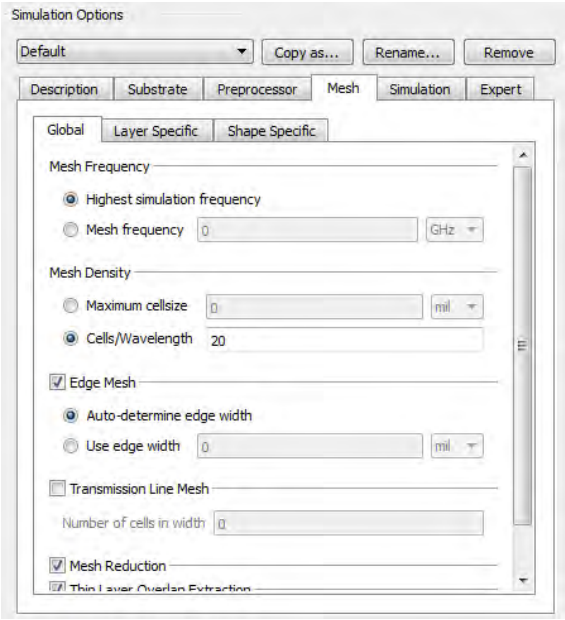
4. Click on the **Frequency Plan** and define the Sweep Type to be Adaptive, Fstart=3 GHz, Fstop=7 GHz and Npts=101



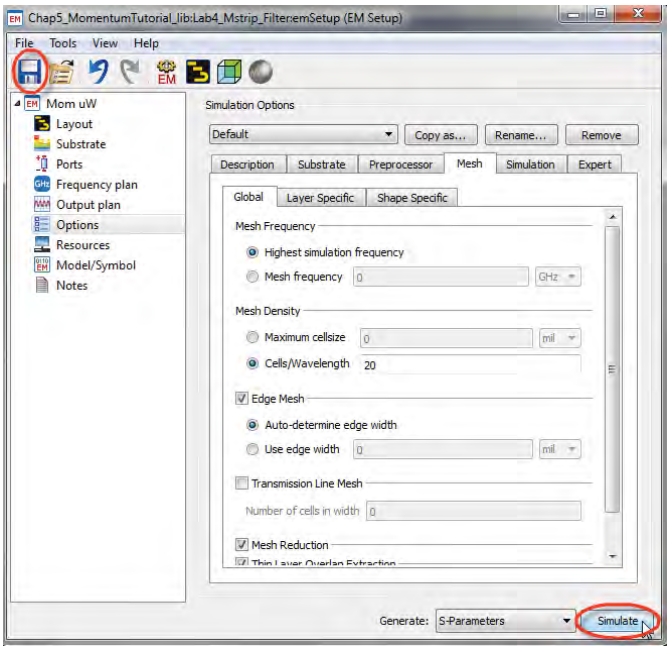
Please note:

1. ***Adaptive is the preferred mode of sweep in EM simulation and not Linear as in case of Schematic simulation.***
2. ***You can add more segments by clicking on the Add button***

5. Click on **Options** and go to **Mesh tab** and select **Edge Mesh** and leave the other fields as default.

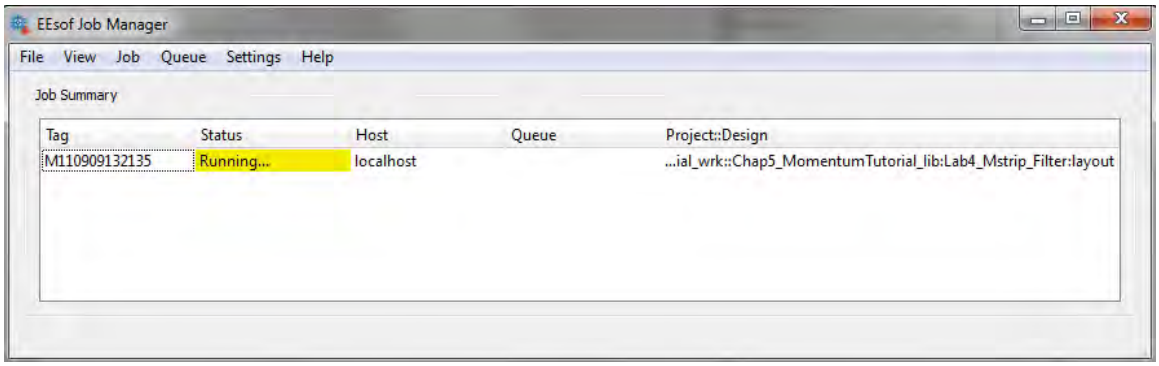


6. Now we are done with the EM setup, click on Save button and click on Simulate button and the bottom right hand side of the EM setup window.

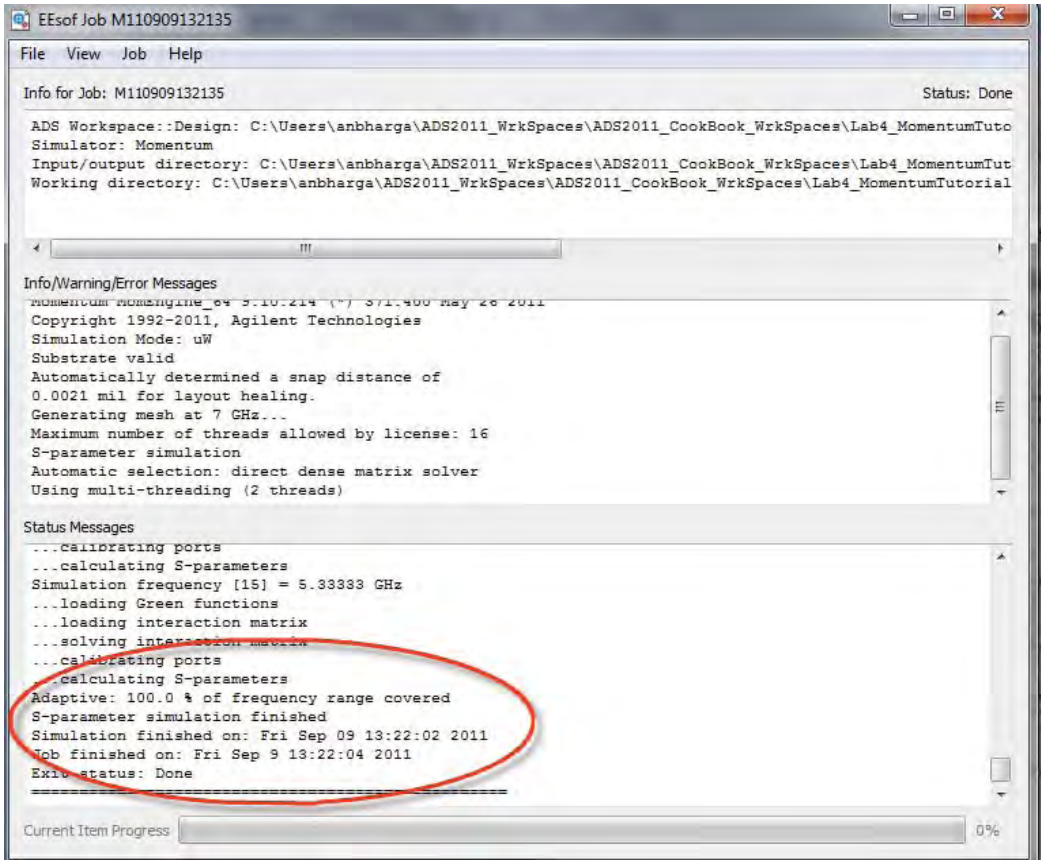


7. This will bring out 2 windows: Job Manager and Momentum Simulation window as shown below:

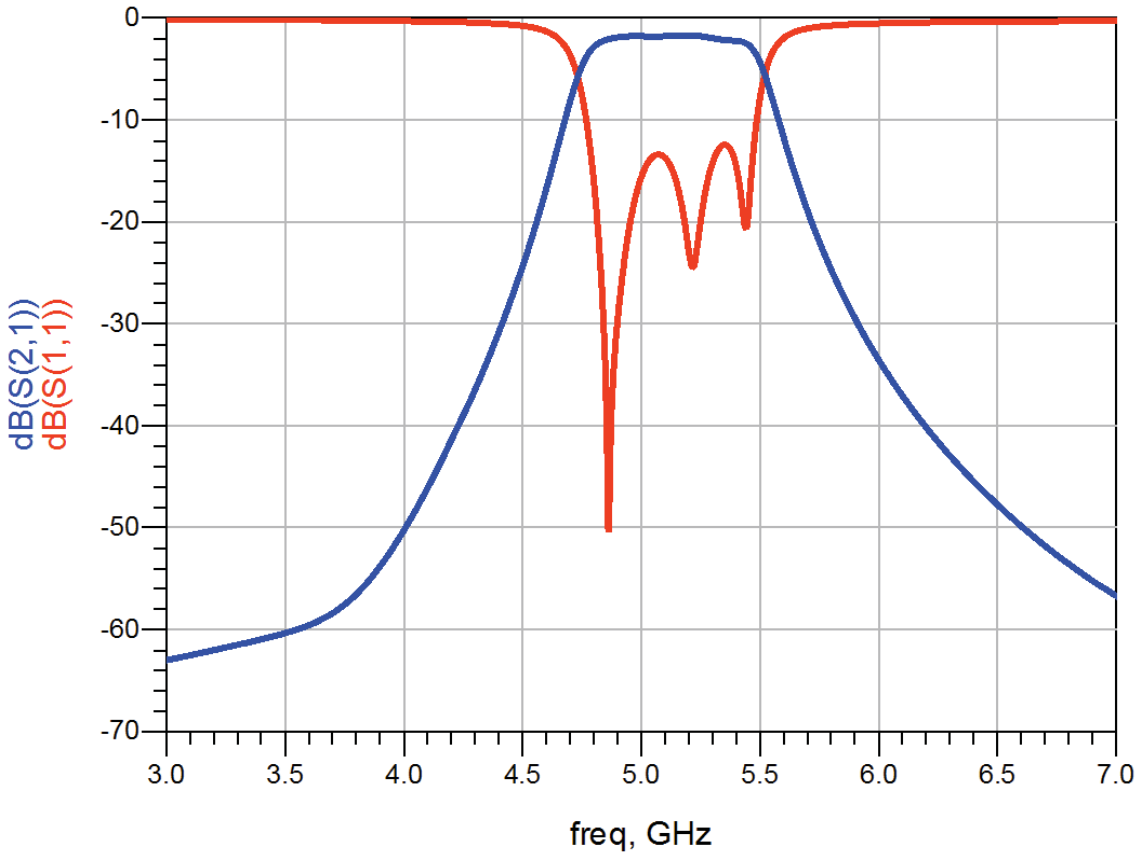
Job Manager window showing that simulation job is running and status will turn to "Done" once simulation is finished.



Momentum Simulation Status window showing that simulation is finished and it took 15 frequency points to achieve the converged results for the sweep we performed. This happened because we selected sweep type as Adaptive and it automatically stops once we have the converged results.



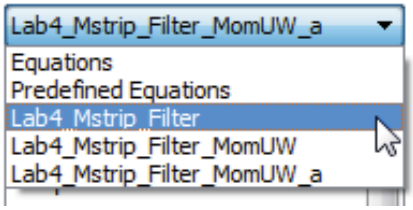
8. Momentum simulation data display with open automatically, delete all the graphs and insert a new rectangular graph and select S(1,1) and S(2,1) to be plotted in dB scale (when prompted)

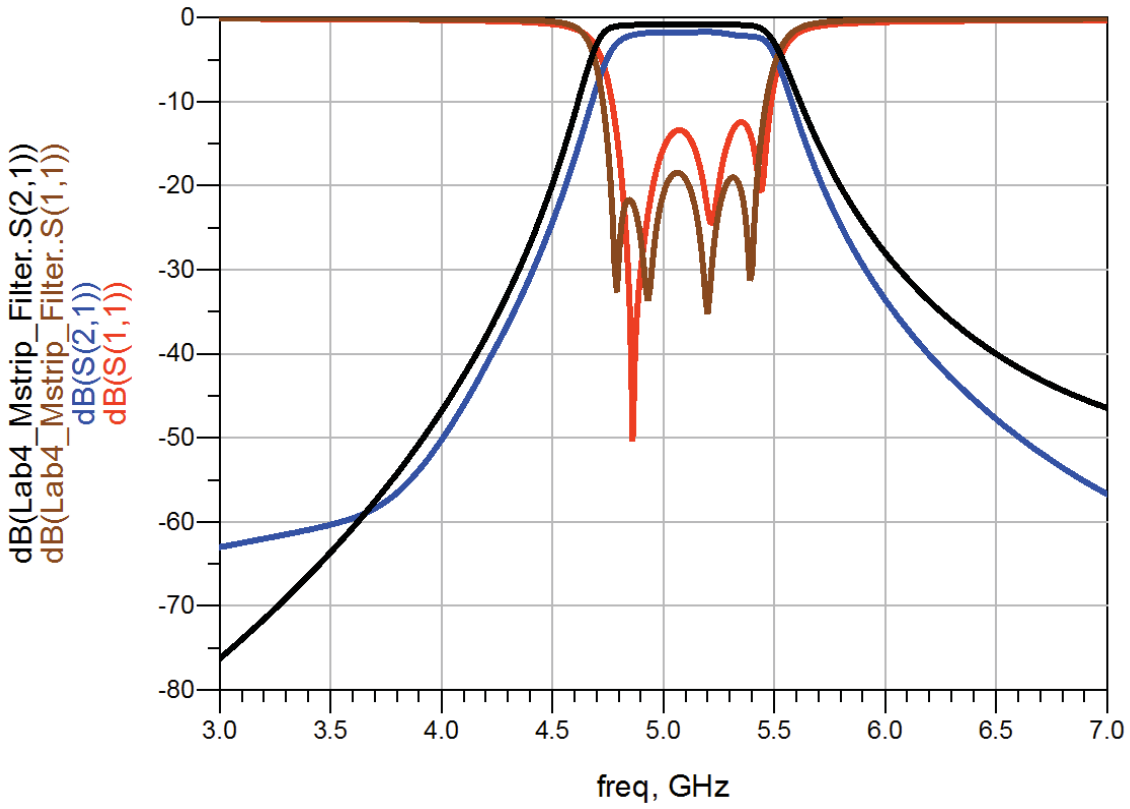


Note: When we perform Adaptive frequency sweep ADS generates 2 dataset files, one for the points which are simulated (in our case: 15 freq points) and the other one with "_a" suffix indicating the adaptive rational polynomial fitted curve as shown below. Dataset with _a suffix is recommended to be used for display purposes….

Step4: Comparison of EM and Schematic Results

Last setup remaining is to compare the EM and schematic results. In order to see both the results on the same graph, double click on the Momentum graph and click on the drop down list to locate the dataset for the circuit which should be with the same name as the cell name (e.g. Lab4_Mstrip_Filter) and select S(1,1) and S(2,1) in dB and observe the response with both circuit simulation as well as Momentum simulation response to compare their performance.





Case Study 2: Design and Simulation of Patch Antenna

Theory:

A microstrip antenna in its simplest configuration consists of a radiating patch on one side of a dielectric substrate, which has a ground plane on the other side. The patch conductors usually made of copper or gold can be virtually assumed to be of any shape. However, conventional shapes are normally used to simplify analysis and performance prediction. The radiating elements and the feed lines are usually photo etched on the dielectric substrate. The basic configuration of a microstrip patch antenna is shown in figure1

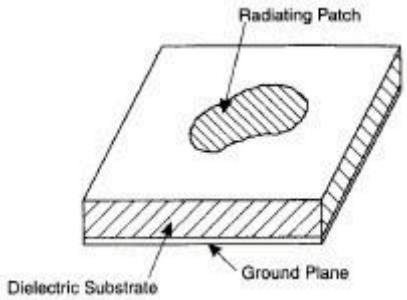


Fig. 1 Basic configuration of Microstrip Antenna

The radiating patch may be square, rectangular, circular elliptical or any other configuration. Square, rectangular and circular shapes are the most common because of ease of analysis and fabrication. Some of the advantages of the microstrip antennas compared to conventional microwave antennas are

- Low weight, low volume
- Low fabrication cost,
- Easy mass production,
- Linear and circular polarization are possible with simple feed,
- Easily integrated with MIC,
- Feed lines and matching networks can be fabricated simultaneously with antenna structures

Patch antennas find various applications stating from military to commercial, because of their ease of design and fabrication. Patch arrays are extensively used in phased array radar applications and in applications requiring high directivity and narrow beamwidth.

Objective:

To design a Patch antenna at 2.4 GHz and simulate the performance using ADS 2011 (or later)

Step1: Calculating Patch Antenna Dimensions

1. Select an appropriate substrate of thickness (h) and dielectric constant (ε_r) for the design of the patch antenna. In present case, we shall use following Dielectric for design:

    a. Height: 1.6 mm
    b. Metal Thickness: 0.7 mil (1/2 oz. Copper)
    c. Er: 4.6
    d. TanD: 0.001
    e. Conductivity: 5.8E7 S/m

2. Calculate the physical parameters of the patch antenna as shown in the geometry in Figure 2 using the given formula.

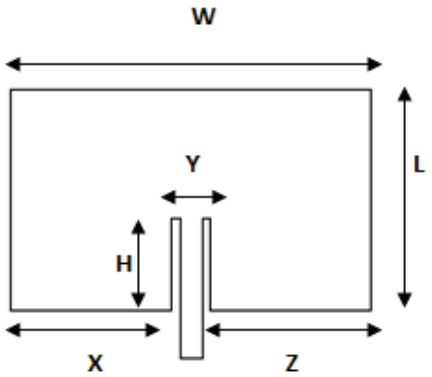


Fig. 2 Geometry of the Square Patch Antenna

The width and length of the radiating surface is given by,

$$W=L=\frac{c}{(2f\sqrt{\varepsilon_r})} = 29.2mm$$

where,

velocity of light c = 3 X 10^8 m/s^2

Frequency, f = 2.4 GHz

Relative Permittivity ε_r = 4.6

The depth of the feed line in to the patch is given by,

$$H=0.822*L/2 \quad = 12 \text{ mm}$$

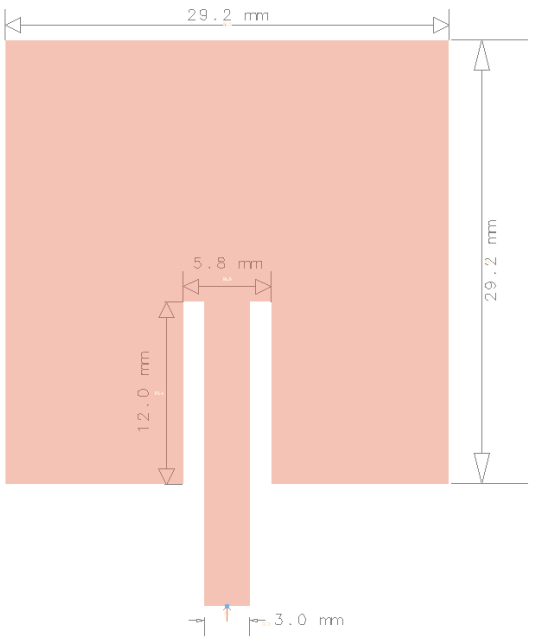
The other dimensions are,

$$Y= W/5 \quad = 5.8 \text{ mm}$$

$$X = Z = 2W/5 \quad = 11.7 \text{ mm}$$

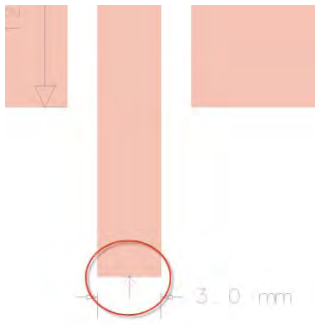
Step2: Creating Patch Antenna Geometry:

1. Create a new workspace, name it as **Lab5_PatchAntenna_wrk**
2. Open the new layout cell and name it as **Patch_Antenna**
3. Use **Insert ->Polygon** and use **Insert->Coordinate Entry** command to enter (X,Y) coordinates to enter required points to construct Patch Antenna geometry as per our calculations:

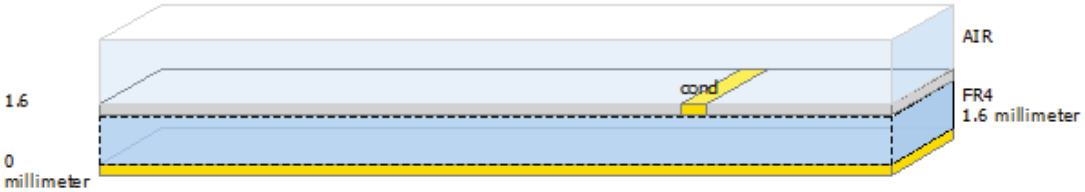


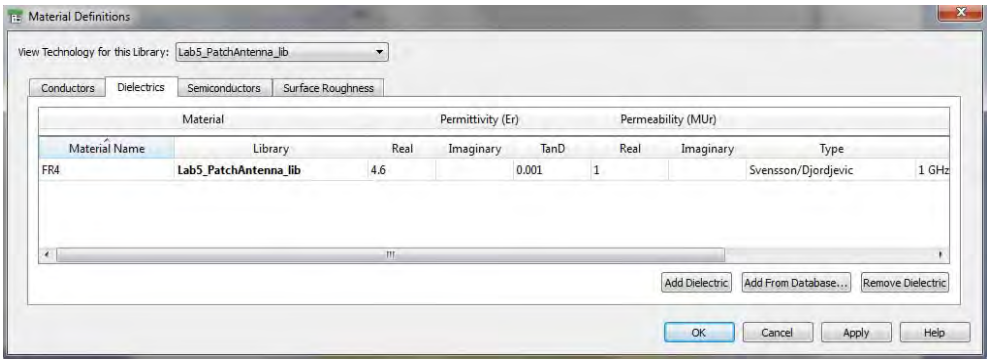
Step3: Antenna Simulation

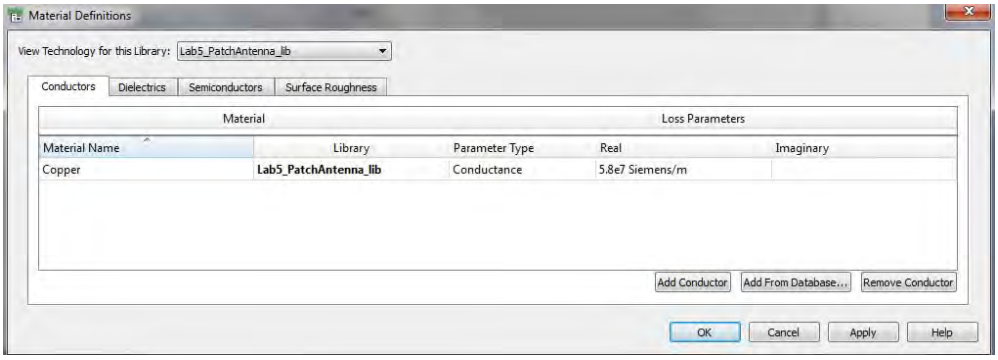
1. Connect a pin at the feed point of the antenna as shown below



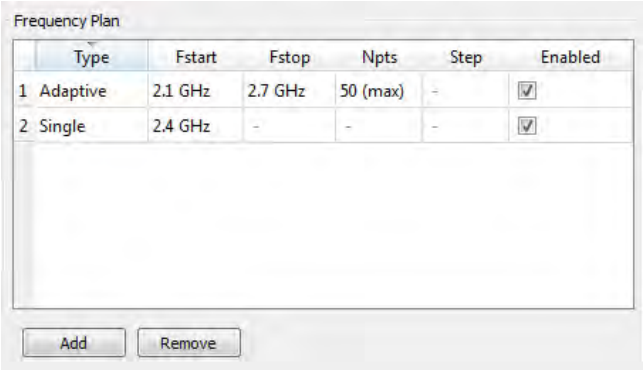
2. Go to the **EM setup** window and click on **Substrate** and click on **New** to accept the 25 mil Alumina template. Define the substrate as below, modify the default substrate height, Er, TanD and conductor height and define it as Copper (select it from Add from Database list). Changing name of the dielectric is optional as it has no bearing on the simulation.



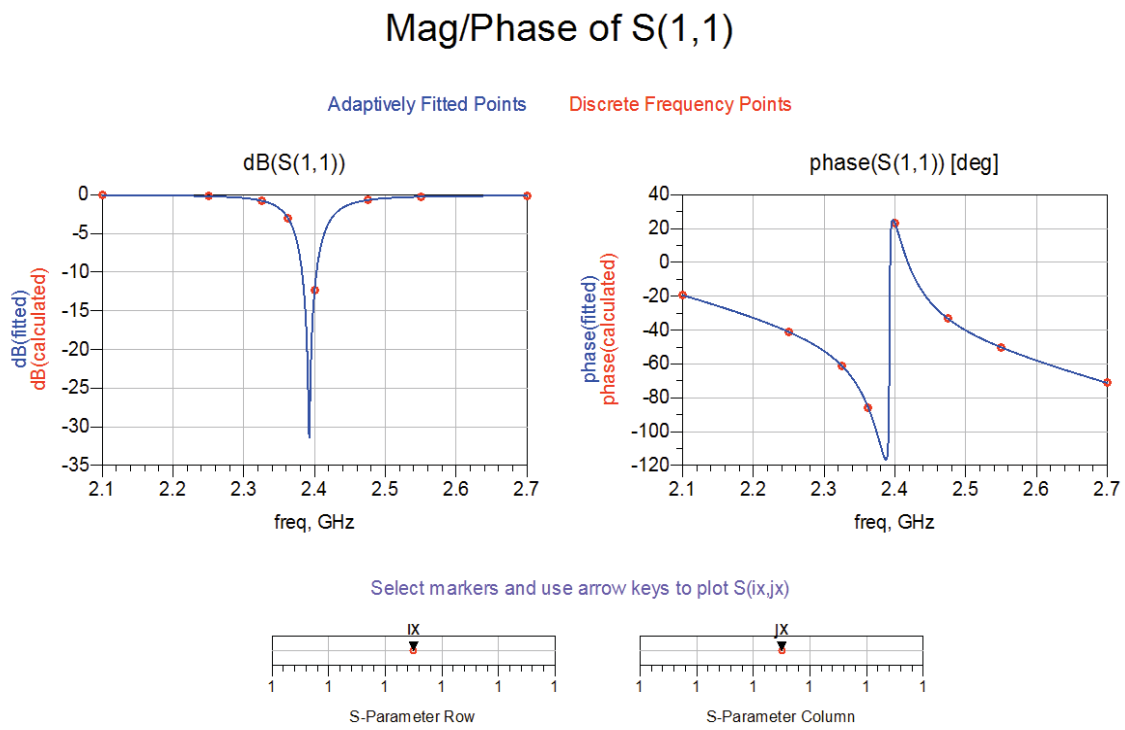




3. Set the **Simulation Frequency range** as 2.1GHz – 2.7GHz (adaptive sweep) and Add a new Single Point of 2.4GHz as shown below

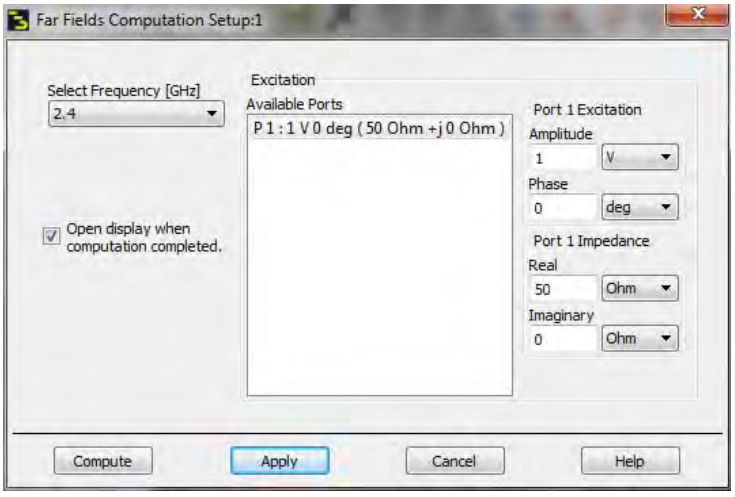


4. Click on Simulate and observe the simulation results in data display

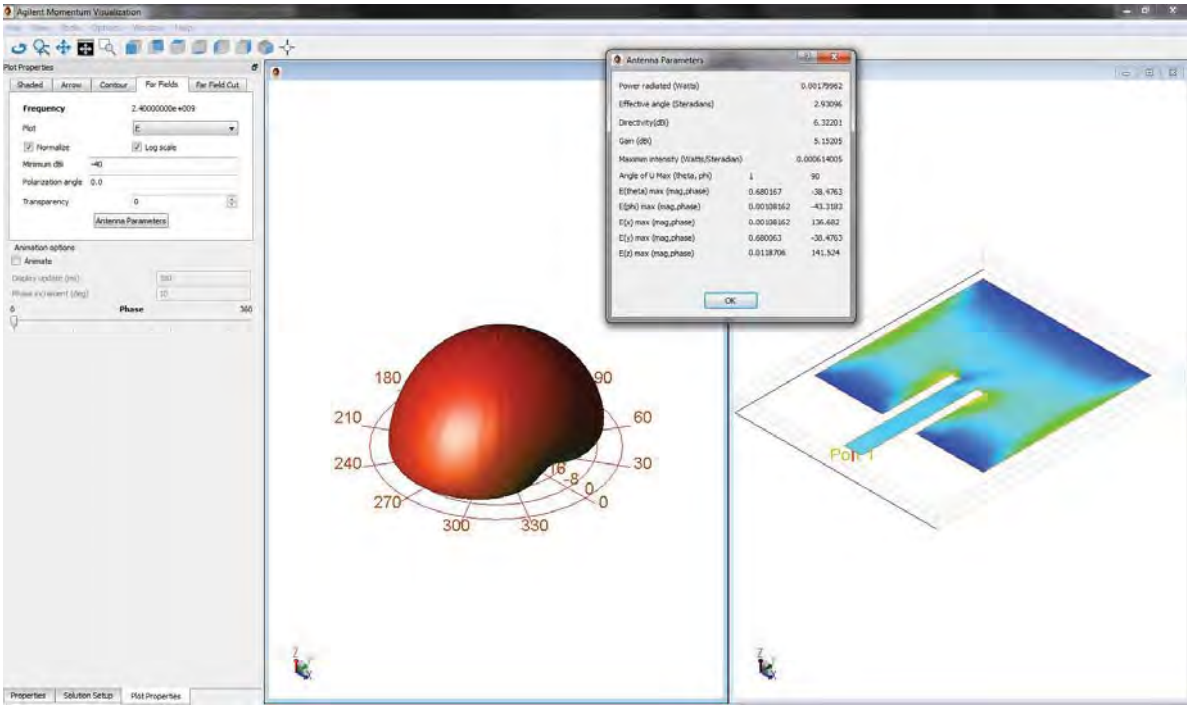


Step4: Antenna Radiation Pattern

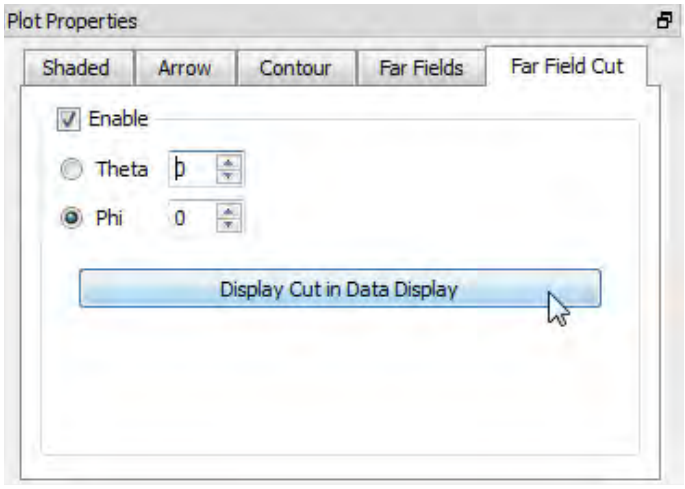
1. For Far-Field Antenna Pattern, go to **EM->Post Processing->Far Field** and select the desired frequency (e.g. 2.4 GHz) and click on Compute.



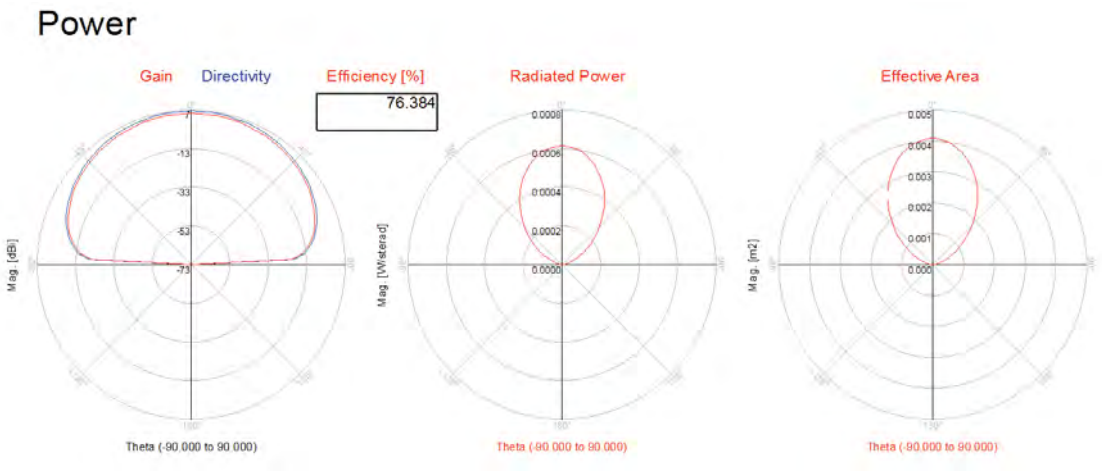
2. Far field computation will be done and results will be displayed in the post processing window as shown below. We can use **Window->Tile** and then go to **Plot Properties** (from the bottom tabs) and then select **Far Field->Antenna Parameters** to see all the required data.



3. Goto **Far Field Cut** tab and select the Phi and click on **Display Cut in data display** button



4. Once done, we will be able to see far field cut in the regular data display as shown below



Case Study 3: EM / Circuit Co-simulation

What is EM / Circuit co-simulation?

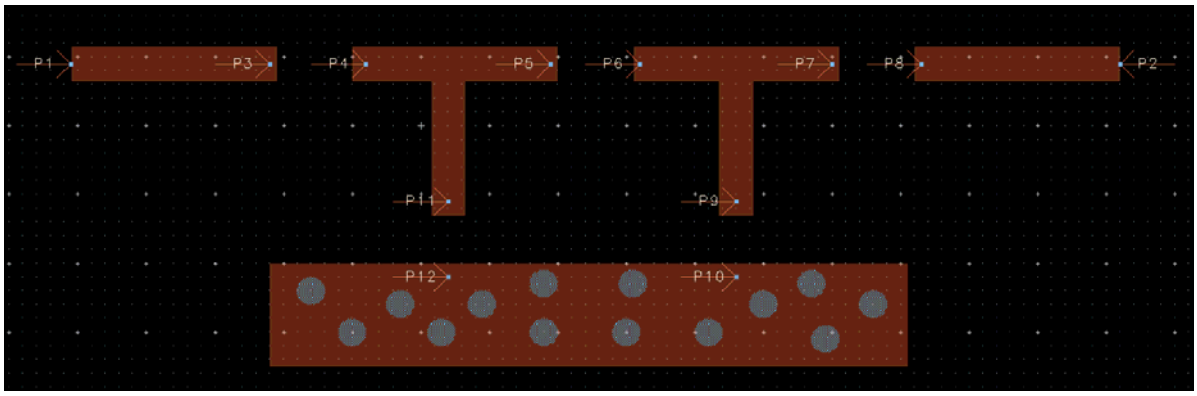
Often there is a requirement of having discrete components such as R, L, C, Transistor, Diodes etc in the layout but EM solvers cannot simulate these discrete components directly hence we use co-simulation whereby we create a layout component and then place it into the schematic for assembly of discrete components.

Typical process for EM / Circuit co-simulation:

1. Connect Pins in the layout where we need to make connections for discrete components
2. Define the stackup and other regular EM settings like Mesh, Simulation Frequency range etc
3. Create a EM Model and Symbol for this layout component
4. Place this layout component in Schematic and connect the required discrete components
5. Set up the appropriate simulation in schematic. Momentum/FEM simulation will be performed if it is already not done else the same data will be reused.

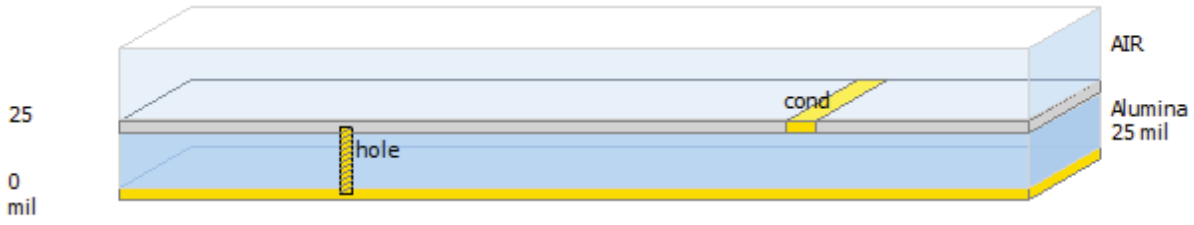
Step1: Create a layout where co-simulation needs to be performed

1. Create layout manually or generate it from the schematic as described in earlier sections.
2. Place Pins wherever we need to make connections or assemble discrete parts alongwith layout
3. In this case we have used “cond” layer for conductors and “hole” layer for VIA to provide a path to ground.



4. Create a substrate with 25 mil Alumina substrate having Er=9.9, TanD=0.0009 and cond layer as Gold with conductivity of 4.1E7 and thickness of 0.7 mil. “hole” layer mapped as VIA will also have Gold conductivity as shown in graphics.

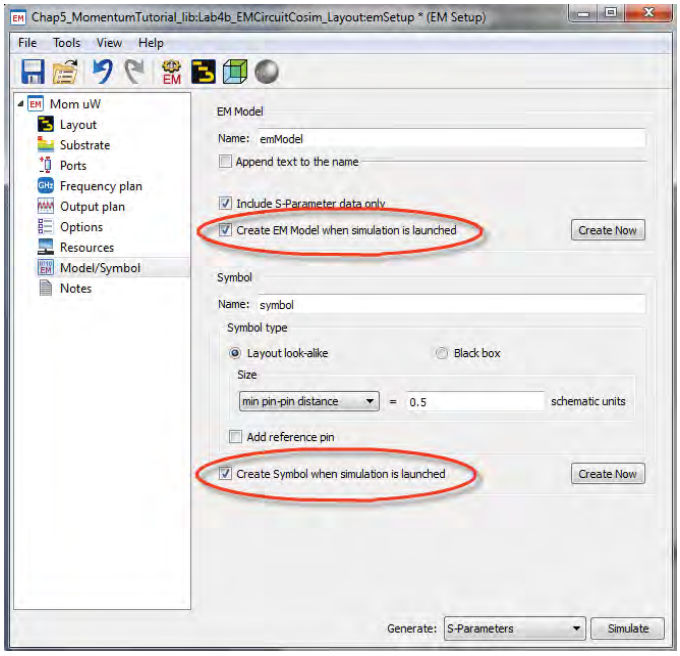
   Tip: To include a VIA in substrate, right click on Alumina in the graphics shown on the substrate window and click on Map Conductor VIA



5. Setup the frequency plan as needed for schematic simulation, e.g. in these case we will keep it from 0.01GHz to 1 GHz with 101 points.

Note: If we need to assemble non-linear component such as Transistor which need to DC biased then Momentum simulation should start from 0 Hz so that DC component can be taken into account accurately.

Step2: Create EM / Circuit co-simulation component and symbol



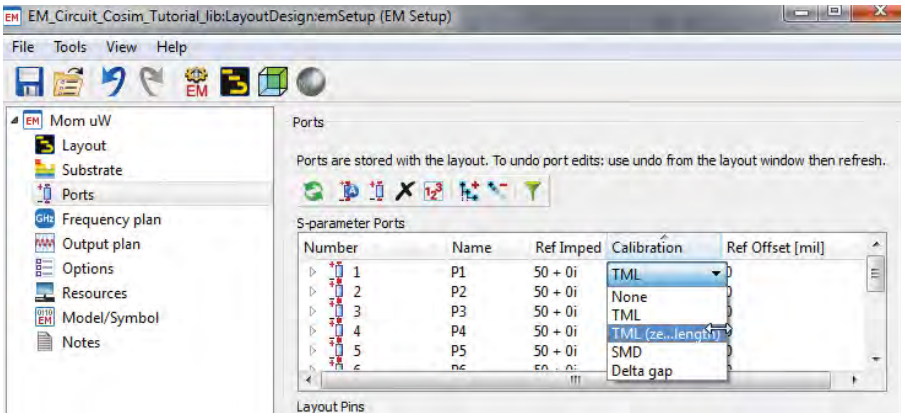
1. For EM / Circuit co-simulation setup, go to Model/Symbol option and select the **"Create EM Model when…"** and **"Create Symbol when……."** as shown in the snapshot
2. These options will create a EM database and symbol which can then be used during the EM/Circuit co-simulation
3. Symbol size can be adjusted by setting **Size->min pin-pin distance** options and by setting the Schematic unit to be 0.1, 0.2 etc…., for this case we set it to 0.5 to keep it reasonably sized symbol when placed in schematic
4. If you want to perform EM simulation along with circuit simulation then click on **Create Now** button for emModel and symbol **or else** click on Simulate icon first to perform Momentum simulation…either way should be fine…
5. Click on **Simulate** button to begin Momentum simulation

Step3: Simulation and database generation process

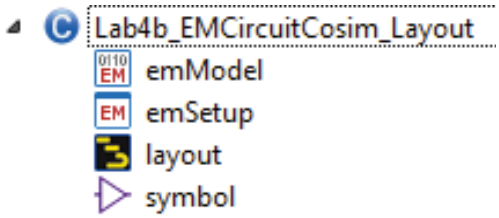
1. When we perform Momentum simulation, warning as below can be noticed in the status window:

```
The port setup needed to be corrected:
Calibration will not be used for port "P11" (pin
"P11" is not on the edge between a conductive
and a nonconductive region).
```

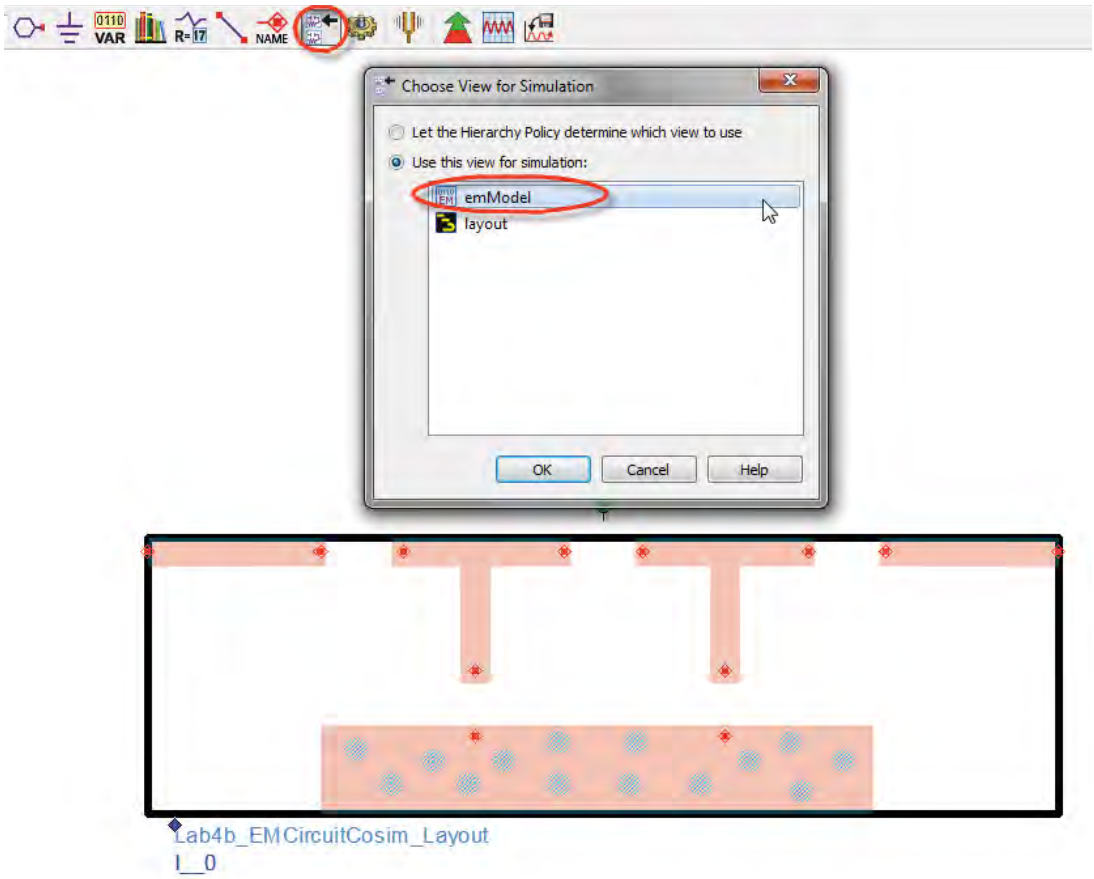
2. This message is simply stating that calibration cannot be done for ports which are placed inside the structure and normally we can ignore them..
3. If specific type of calibration is needed same can be done in the Ports option of EM setup window as shown in snapshot below



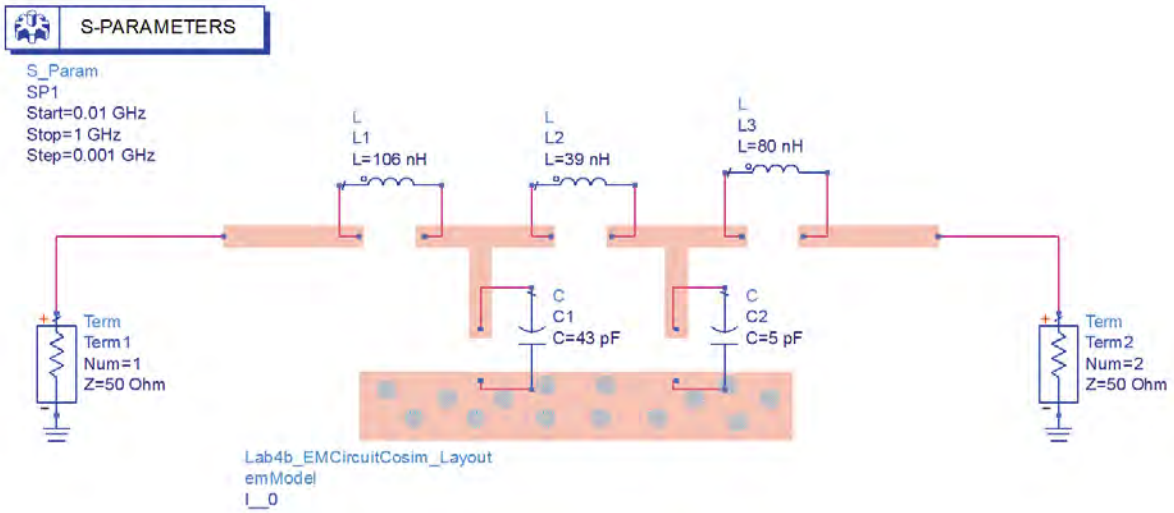
4. When simulation is finished Momentum data display will be opened but we do not need to see it right now as the discrete components are not yet assembled with the layout but sometime it is good to observe the results to see what kind of cross-coupling exists between the different sections of the layout without the components being mounted because due to wrong layout sometimes we end up having unnecessary coupling between the sections causing our performance to degrade.



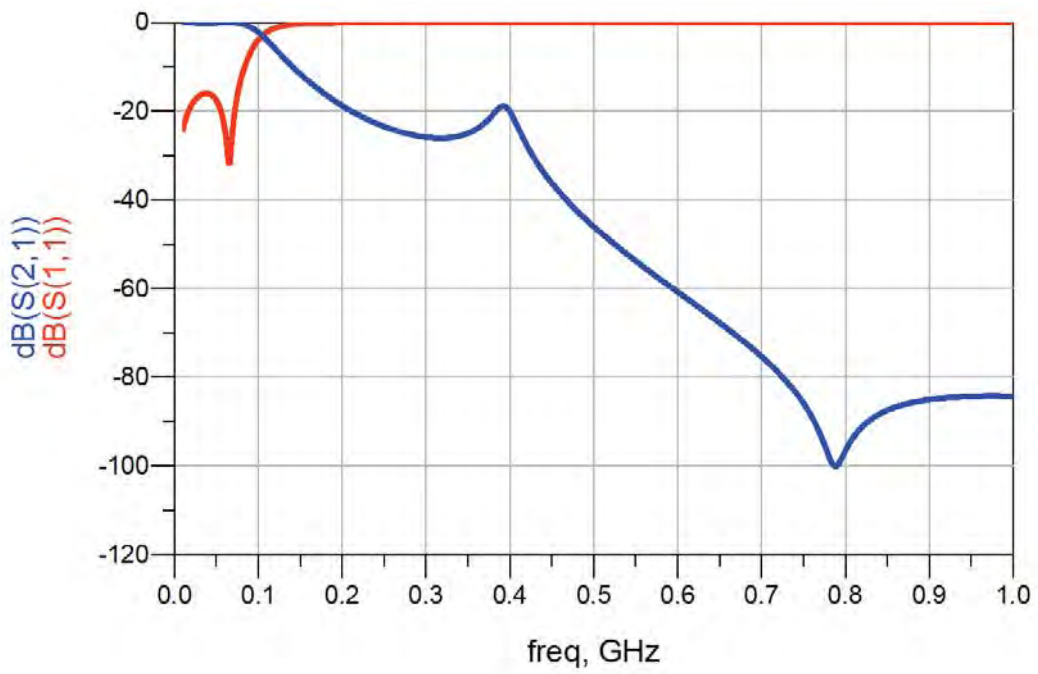
5. Observe the ADS main window and we will notice **"emmodel"** and **"symbol"** now appearing under the cell on which simulation is being performed…we shall use **"emmodel"** for EM / Circuit co-simulation
6. Open a new schematic cell, drag & drop **emmodel** view from the Main Window on this schematic cell. Select the layout symbol and click on **"Choose view for simulation"** and select **emmodel** from the list as shown below.



7. Place the desired discrete components on the schematic and connect them to the layout component as shown in the snapshot below.



8. Click on Simulate icon on schematic and insert the rectangular plot to observe S(1,1) & S(2,1) as shown below



Chapter 5: Using FEM Simulator in ADS

ADS Licenses Used:

- **Layout**
- **FEM Simulator**

Chapter 5: Using FEM Simulator in ADS

Introduction:

FEM simulator provides a complete solution for electromagnetic simulation of arbitrarily-shaped and passive three-dimensional structures. FEM simulators create full 3D EM simulation an attractive option for designers working with RF circuits, MMICs, PC boards, modules, and Signal Integrity applications. It provides fully automated meshing and convergence capabilities for modeling arbitrary 3D shapes such as bond wires and finite dielectric substrates. Along with Momentum, FEM simulator in ADS provide RF and microwave engineers access to some of the most comprehensive EM simulation tools in the industry.

Developed with the designer of high-frequency/high-speed circuits in mind, FEM Simulator offers a powerful finite-element EM simulator that solves a wide array of applications with impressive accuracy and speed.

The Finite Element Method

To generate an electromagnetic field solution from which S-parameters can be computed, FEM Simulator employs the finite element method. In general, the finite element method divides the full problem space into thousands of smaller regions and represents the field in each sub-region (element) with a local function.

In FEM Simulator, the geometric model is automatically divided into a large number of tetrahedra, where a single tetrahedron is formed by four equilateral triangles.

Representation of a Field Quantity

The value of a vector field quantity (such as the H-field or the E-field) at points inside each tetrahedron is interpolated from the vertices of the tetrahedron. At each vertex, FEM Simulator stores the components of the field that are tangential to the three edges of the tetrahedron. In addition, the component of the vector field at the midpoint of selected edges that is tangential to a face and normal to the edge can also be stored. The field inside each tetrahedron is interpolated from these nodal values.

Basis Functions

A first-order tangential element basis function interpolates field values from both nodal values at vertices and on edges. First-order tangential elements have 20 unknowns per tetrahedra.

Size of Mesh vs. Accuracy

There is a trade-off between the size of the mesh, the desired level of accuracy, and the amount of available computing resources.

On one hand, The accuracy of the solution depends on the number of the individual elements (tetrahedra) present. Solutions based on meshes that use a large number of elements are more accurate than solutions based on coarse meshes using relatively few elements. To generate a precise description of a field quantity, each tetrahedron must occupy a region that is small enough for the field to be adequately interpolated from the nodal values.

However, generating a field solution for meshes with a large number of elements requires a significant amount of computing power and memory. Therefore, it is desirable to use a mesh that is fine enough to obtain an accurate field solution but not so fine that it overwhelms the available computer memory and processing power.

To produce the optimal mesh, FEM Simulator uses an iterative process in which the mesh is automatically refined in critical regions. First, it generates a solution based on a coarse initial mesh. Then, it refines the mesh based on suitable error criteria and generates a new solution. When selected, S-parameters converge to within a desired limit, the iteration process ends.

Field Solutions

During the iterative solution process, the S-parameters typically stabilize before the full field solution. Therefore, when analyzing the field solution associated with a structure, it may be desirable to use a convergence criterion that is tighter than usual.
In addition, for any given number of adaptive iterations, the magnetic field (H-field) is less accurate than the solution for the electric field (E-field) because the H-field is computed from the E-field using the following relationship:

$$\boldsymbol{H} = \frac{\nabla \times \boldsymbol{E}}{-j\omega\mu}$$

thus, making the polynomial interpolation function an order lower than those used for the electric field.

Implementation Overview

To calculate the S-matrix associated with a structure, the following steps are performed:

1. The structure is divided into a finite element mesh.
2. The waves on each port of the structure that are supported by a transmission line having the same cross section as the port are computed.
3. The full electromagnetic field pattern inside the structure is computed, assuming that each of the ports is excited by one of the waves.
4. The generalized S-matrix is computed from the amount of reflection and transmission that occurs.

The final result is an S-matrix that allows the magnitude of transmitted and reflected signals to be computed directly from a given set of input signals, reducing the full three-dimensional electromagnetic behavior of a structure to a set of high frequency circuit values.

Setting up FEM Simulation:

Key steps to be followed for a successful FEM simulation in ADS are:

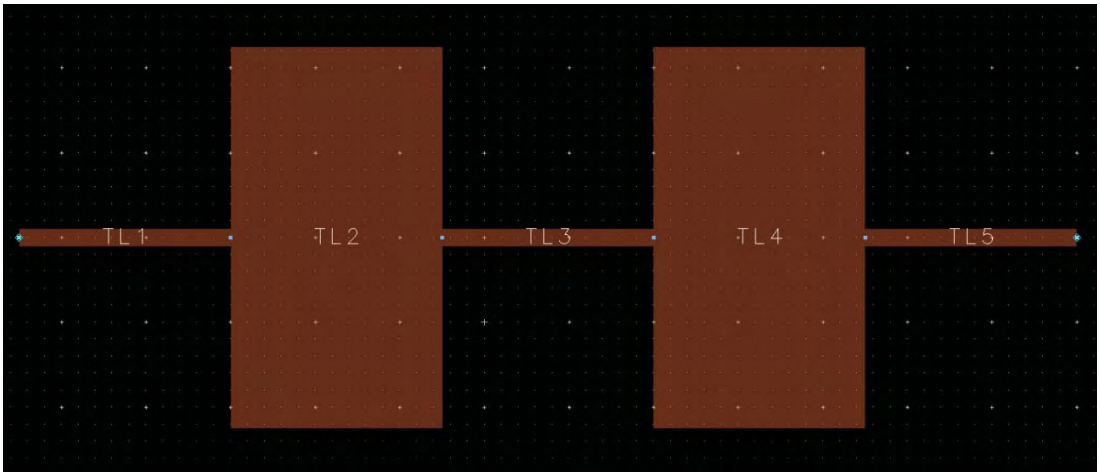
Step1: Creating a Physical design
Step2: Defining Substrates
Step3: FEM Simulation Setup:
   a. Assigning Port Properties
   b. Defining Frequency and output plan
   c. Defining Simulation Options e.g. Meshing, Solver Selection (Direct or Iterative) etc
   d. Run FEM Simulation
Step4: View the Results, Far Fields etc

Case Study: Microstrip Low Pass Filter

Let's learn FEM simulation in ADS by creating simple low pass filter circuit as shown below using MLIN components from TLines-Microstrip library in ADS layout.

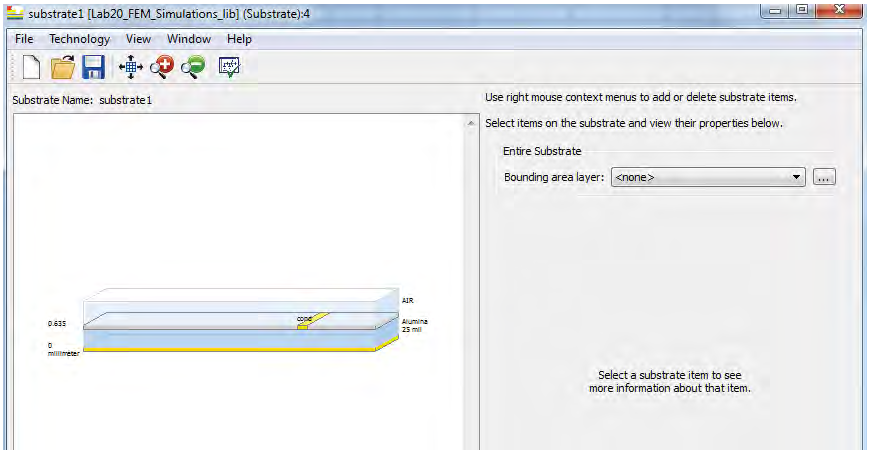
Step 1: Creating a Physical Design

1. Create a new workspace Lab20_FEM_Simulations_wrk and select units as "mm" in the workspace wizard.
2. From the TLines-Microstrip library, place 5 MLIN components with following dimensions:
    a. Line 1, 3, 5: Width = 0.2 mm, Length = 2.5 mm
    b. Line 2, 4: Width = 4.5 mm, Length = 2.5 mm

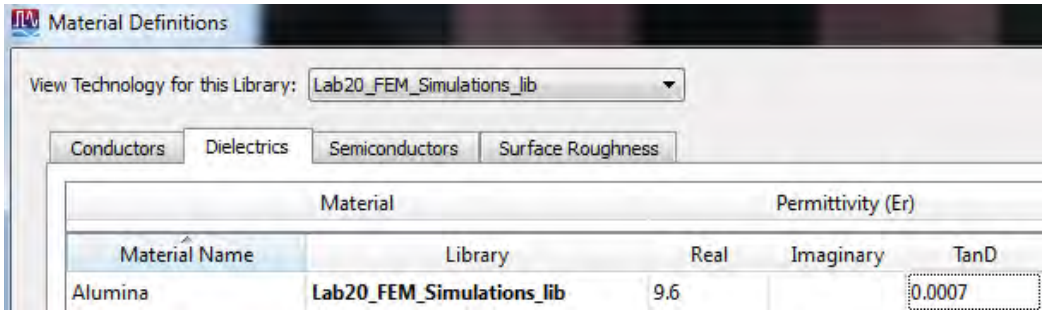


Step 2: Defining the Substrate

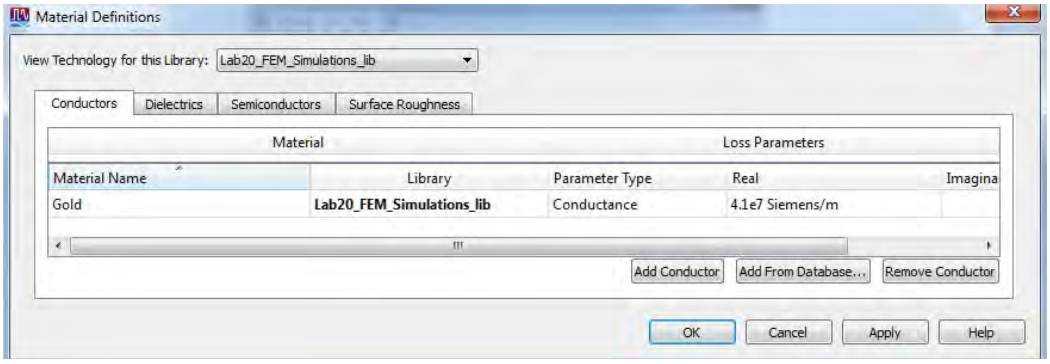
1. Click on Substrate icon as shown here to define the desired substrate for our simulation 
2. Select 25mil Alumina substrate template from the pop-up window and default substrate will be visible as shown below:



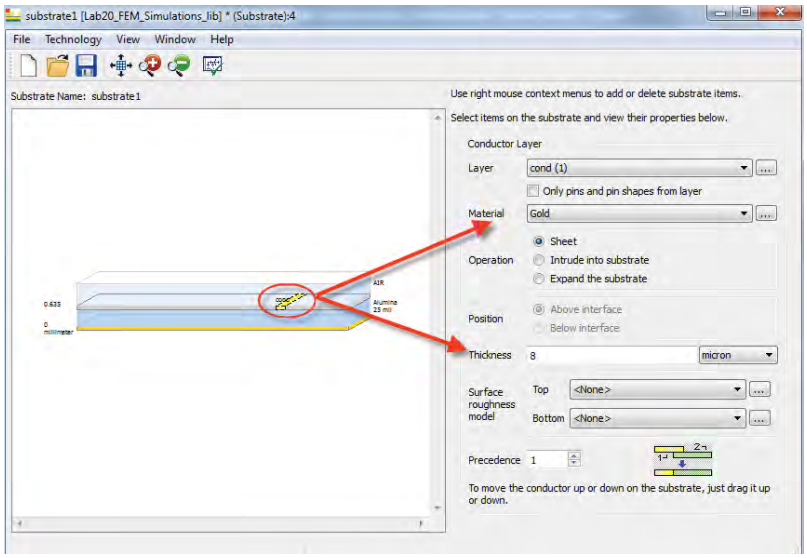
3. Go to Technology->Material Definition menu and in the Dielectric Tab modify the existing Alumina's TanD (Loss Tangent) as 0.0007. You can also add a dielectric using the "Add from Database" option.



4. Go to Conudctors Tab and click on "Add from Database" and select Gold conductor from the available list and click OK.



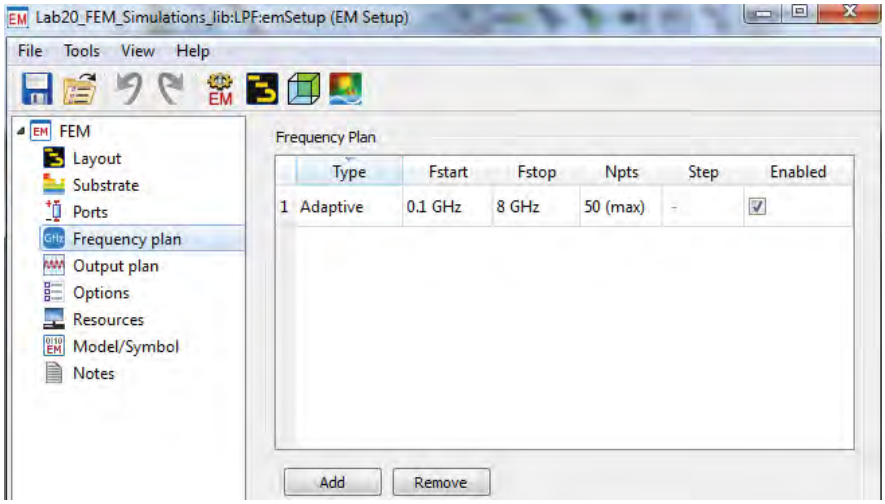
5. In the GUI of the susbtrate setup, click on cond strip and modify the Material as "Gold" and enter thickness as 8 micron



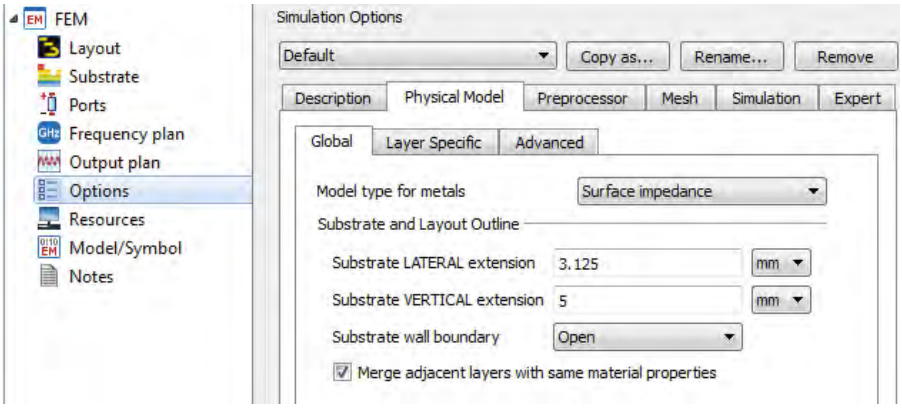
6. Click on Save and close the substrate editor.
7. Connect 2 Pins, one each at the input and output connection point using Pin icon

Step 3: FEM simulation setup

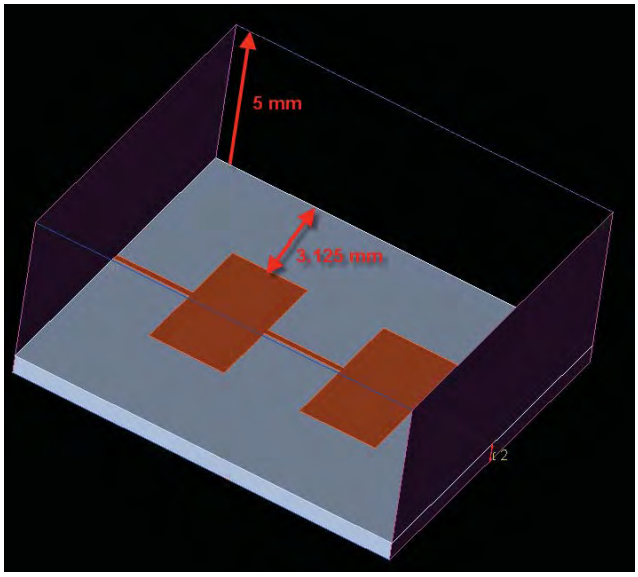
1. Click on EM setup icon to open the EM simulation setup window. Select FEM Simulator.
2. Select Frequency Plan option, and enter Fstart = 0.1 GHz Fstop = 8 GHz

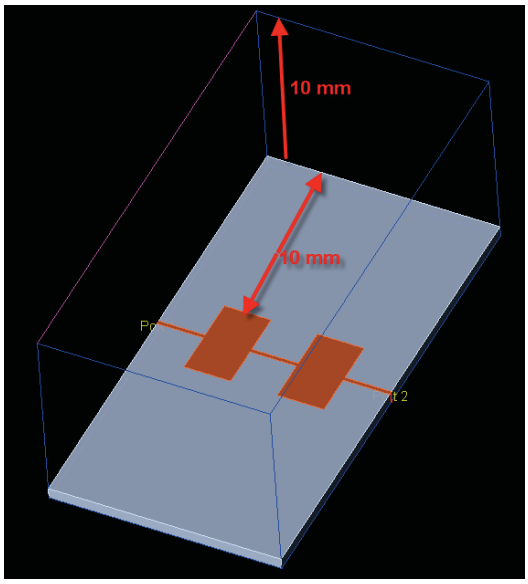


3. **Go to Options Tab** which is one of the critical step in setting up FEM simulation. Let's discuss each option in detail.
   a. **Physical Model:** As ADS possess 2D layout editor, we need to define 3D attributes of the structure which will be used for FEM simulation in this tab:
      i. **Substrate LATERAL extension:** This option lets user decide how much extra dielectric to use for finite dielectric size in from the edge on layout in all directions where Calibrated Ports (TML or TML Zero Length) are not connected.
      ii. **Substrate VERTICAL extension:** This option lets user decide the Air height on top of dielectric surface. As a general guideline the vertical extension should be @ 5-10 times of substrate height.



For our project we shall keep the default settings as shown above.





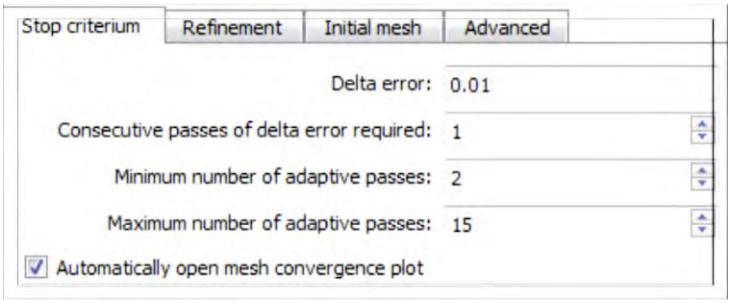
Lateral extension = 3.125 mm
Vertical extension = 5 mm

Lateral extension = 10 mm
Vertical extension = 10 mm

Snapshots above shows 3D view of the filter structure with two LATERAL extension setting.

b. Mesh:

For FEM simulation, Mesh has various settings which need to be understood properly for accurate simulations.



Stop Criterium:

i. **Delta Error:** This figure determines the Mesh convergence factor to have stabilized field as described in section Size of Mesh vs. Accuracy. This is figure of merit to check S matrix divergence from one mesh size to another and once the difference is below the delta error number then Matrix solution process is started.

ii. **Consecutive passes of delta error required:** This option let user check whether the mesh convergence achieved once was real or not.

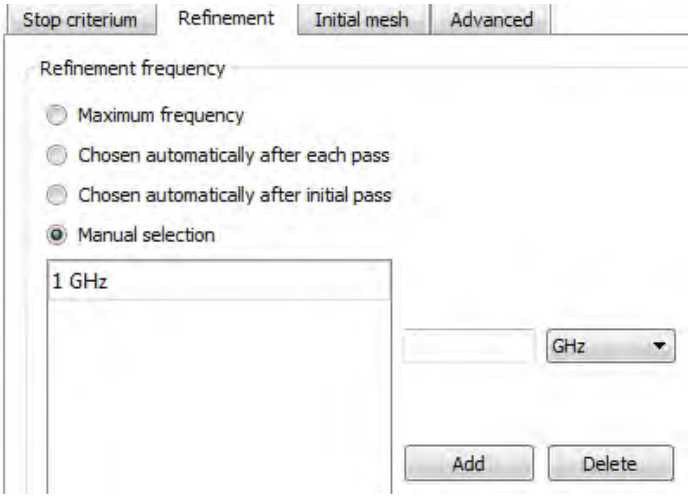
iii. **Minimum number of adaptive passes:** Number of mesh iterations to be performed even if mesh convergence is achieved earlier than the number specified.

iv. **Maximum number of adaptive passes:** Maximum limit for mesh iterations to meet delta error criteria.

Set the parameters as shown in the snapshot above.

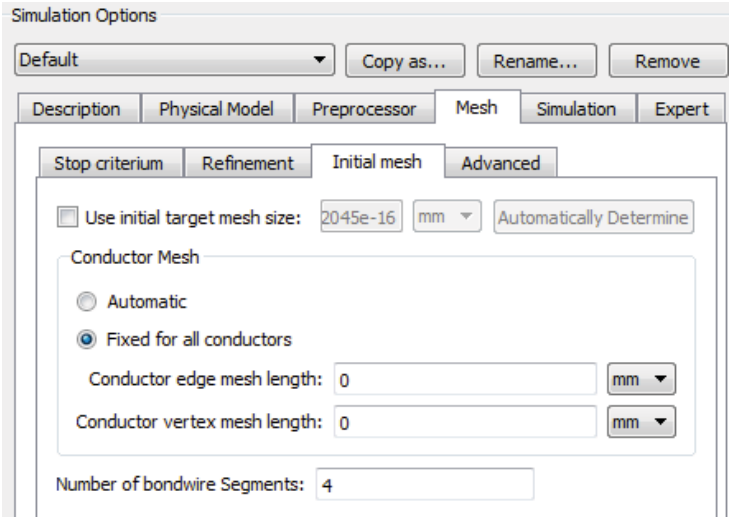
Refinement:

Under refinement tab, designers can specify the frequency on which Mesh will be generated to solve the structure. As a general guideline for better & quicker mesh convergence it is recommended to create mesh on the frequency on which structure has the good amount of energy. For filter structures it is recommended that the mesh frequency is in the passband. For our LPF, select Manual selection and enter it as 1 GHz.



Initial Mesh:

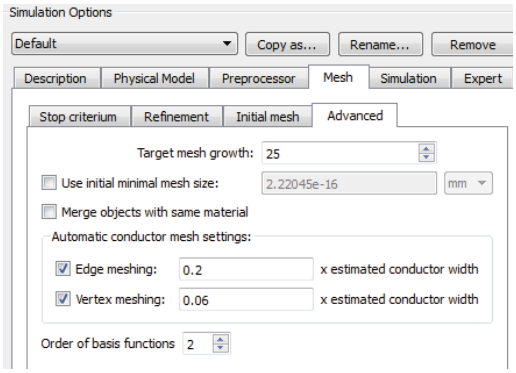
In the Initial mesh settings designer can specify good starting size for mesh which can help in getting to convergence faster.
Automatic Conductor Mesh setting enables mesher to create finer mesh along the edges of the strips for better accuracy. This feature is helpful in simulating some troublesome tightly coupled structures.



Advanced:

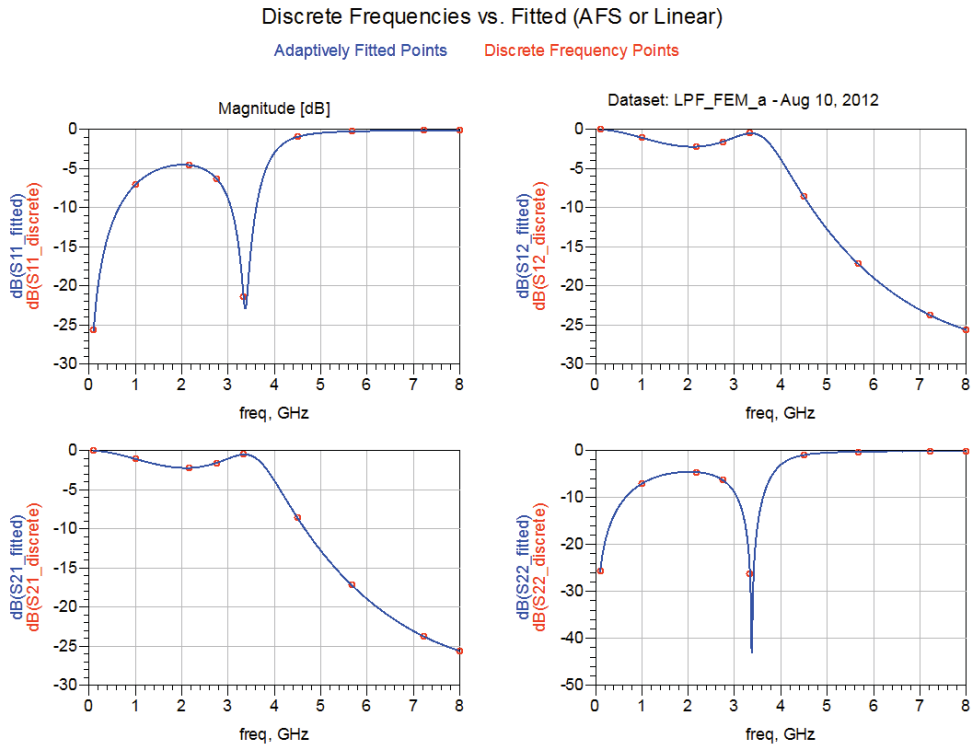
Under Advanced option tab, we can specify following:

- **Target Mesh Growth:** Percentage of Tetrahedron growth during each iteration.
- **Use Initial minimal mesh size:** This is again to set user defined size for mesh for faster convergence.
- **Merge objects with same material:** This option helps in reducing number of unknowns in a structure for faster simulation.
- **Automatic conductor mesh settings:** If Automatic setting was selected under Initial mesh then these factors will be used for finer meshing.



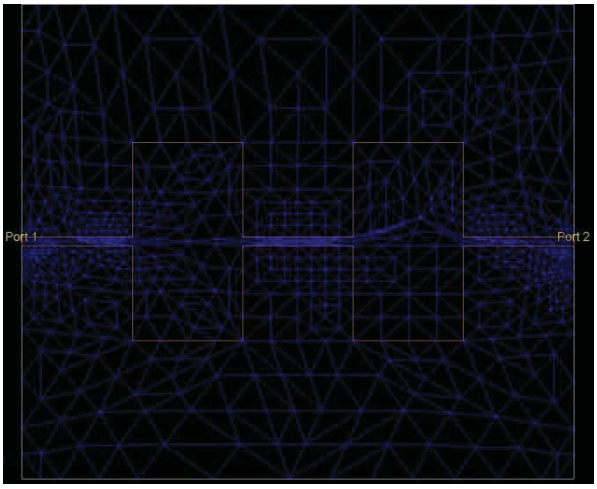
Click on Simulate icon to start FEM simulation and observe the result as shown below.

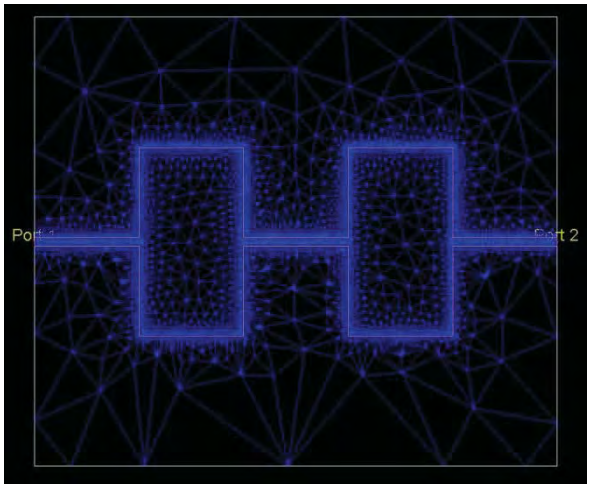
Step 4: Results



Click on field visualization to open the Field Visualization. Click View->Top View to see the top view of the filter structure.

From the Plot Properties tab, select Z: 0.635 Show button to see the Mesh as shown below.





Mesh with "Fixed for all conductors" **Mesh with "Automatic" conductor setting**

Symmetry Planes in FEM

To reduce the size of the problem and memory requirement for faster simulations, FEM simulator in ADS can utilize the symmetric boundary condition either in E-plane or H-plane so that only half of the structure is simulated thus requiring lesser systemresources.

Adding a Symmetry Plane

A symmetry plane defines the boundary on one side of the circuit substrate. Only one box, or a waveguide, or a symmetry plane can be applied to a circuit at a time. When a symmetry plane is defined, the simulation results will be equivalent to the results of a larger circuit that would be created by mirroring the circuit about the symmetry plane.
For symmetric circuits, this enables faster simulations that require less memory because only half the actual structure needs to be simulated.

To add a symmetry plane:

1. Choose **EM** > **FEM Symmetry Plane** > **Add Symmetry Plane**.
2. Select the direction of the symmetry plane. To insert the symmetry plane parallel to the x-axis, click X-axis. To insert the symmetry plane parallel to the y-axis, click Y-axis.
3. Insert the symmetry plane using one of the following two methods:
   - Position the mouse and click to define the location of the symmetry plane.
   - From the Layout menu bar, select **Insert** > **Coordinate Entry** and use the Coordinate Entry X and Coordinate Entry Y fields to specify a point on the edge of the substrate.

4. Click **Apply**.

This boundary specifies the edge of the substrate where the plane of symmetry will be applied.

Editing a Symmetry Plane

Once the symmetry plane is applied, you cannot change its location. If you want to change the location or orientation, you must delete the current symmetry plane and add a new one.

Deleting a Symmetry Plane

To delete a symmetry plane:

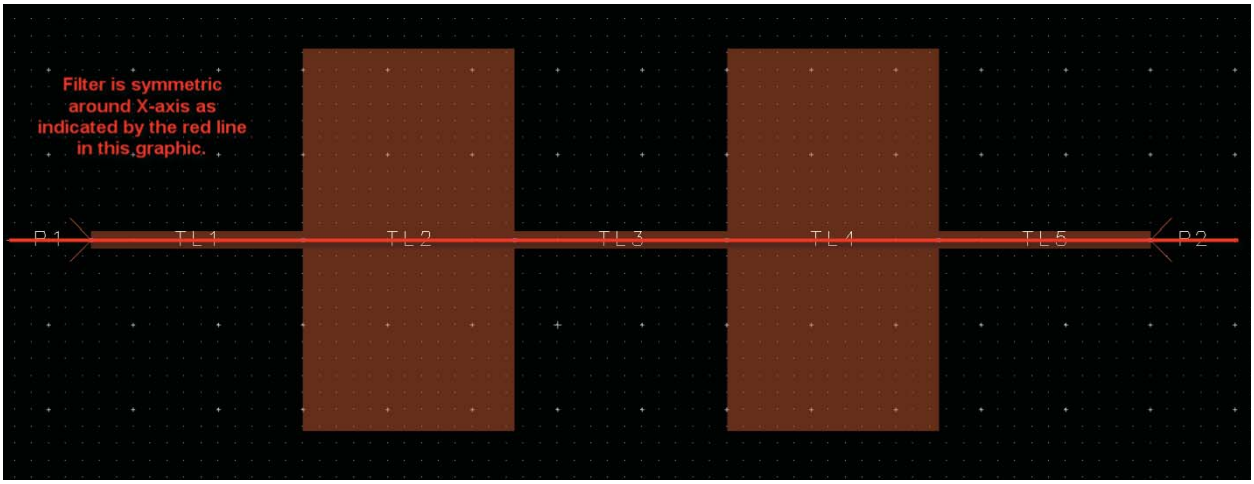
1. Select **EM** > **FEM Symmetry Plane**> **Delete Symmetry Plane**. The symmetry plane is removed from the layout.

Case Study: LPF Design with Symmetry Plane

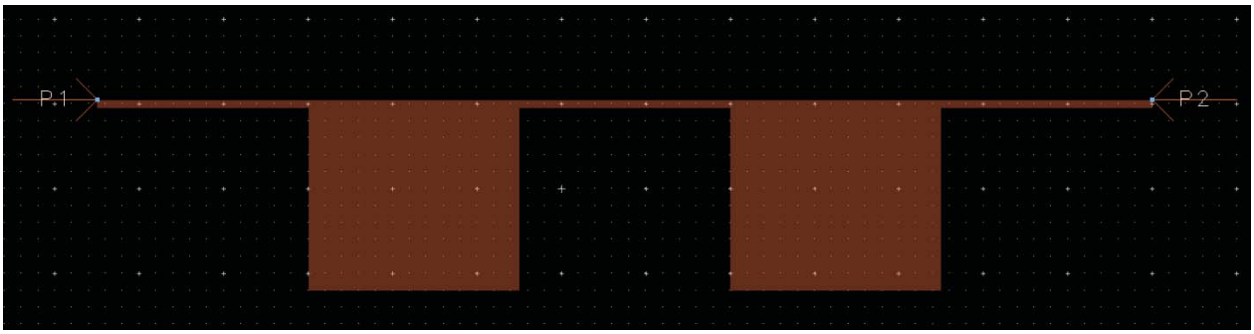
Let's simulate our LPF design using symmetry plane, follow the process below:

Step 1: Create partial design

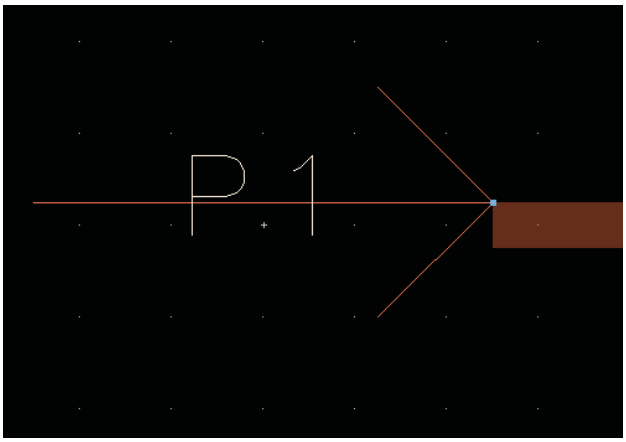
For Symmetry Plane condition we only need to create half geometry which should be symmetric around the desired X or Y axis.
If we observe our LPF design closely we shall find that it is symmetric to X-axis as shown below.



Using either MLIN or Rectangle drawing tool, create half section LPF design as shown below

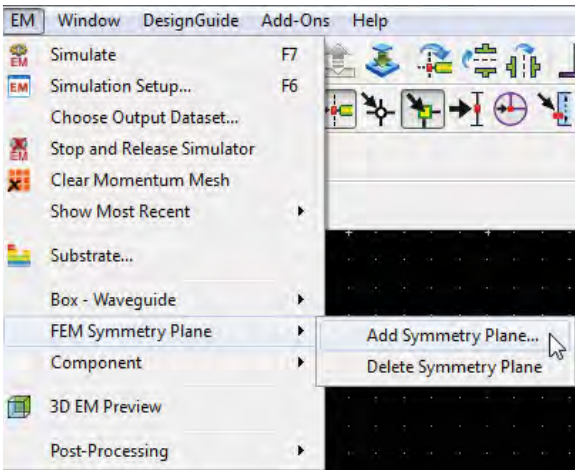


Input and Output ports will now be connected to the edge where the structure is symmetric as shown below

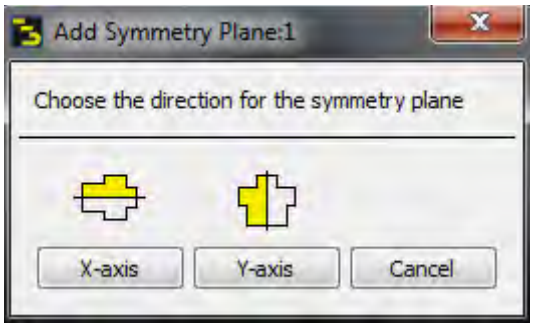


Step 2: Applying Symmetry Plane

Go to EM->FEM Symmetry Plane->Add Symmetry Plane option

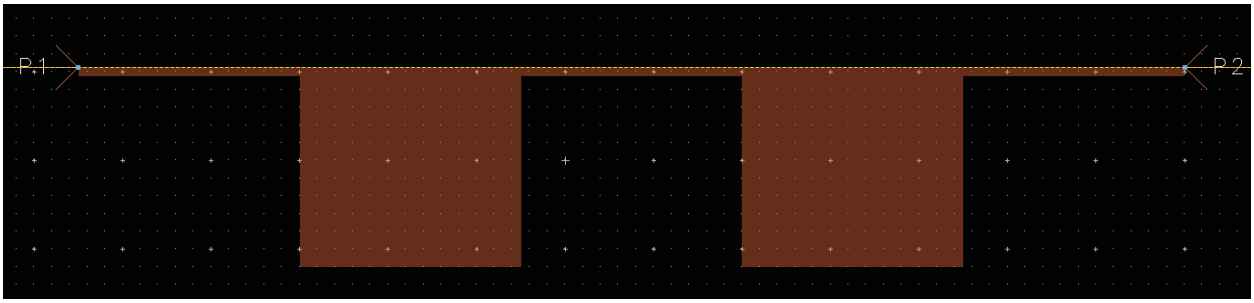


Select whether you would like to apply Symmetry Plane on X-axis or Y-axis from the Add Symmetry Plane dialog box



In our case we will select X-axis, click on X-axis button

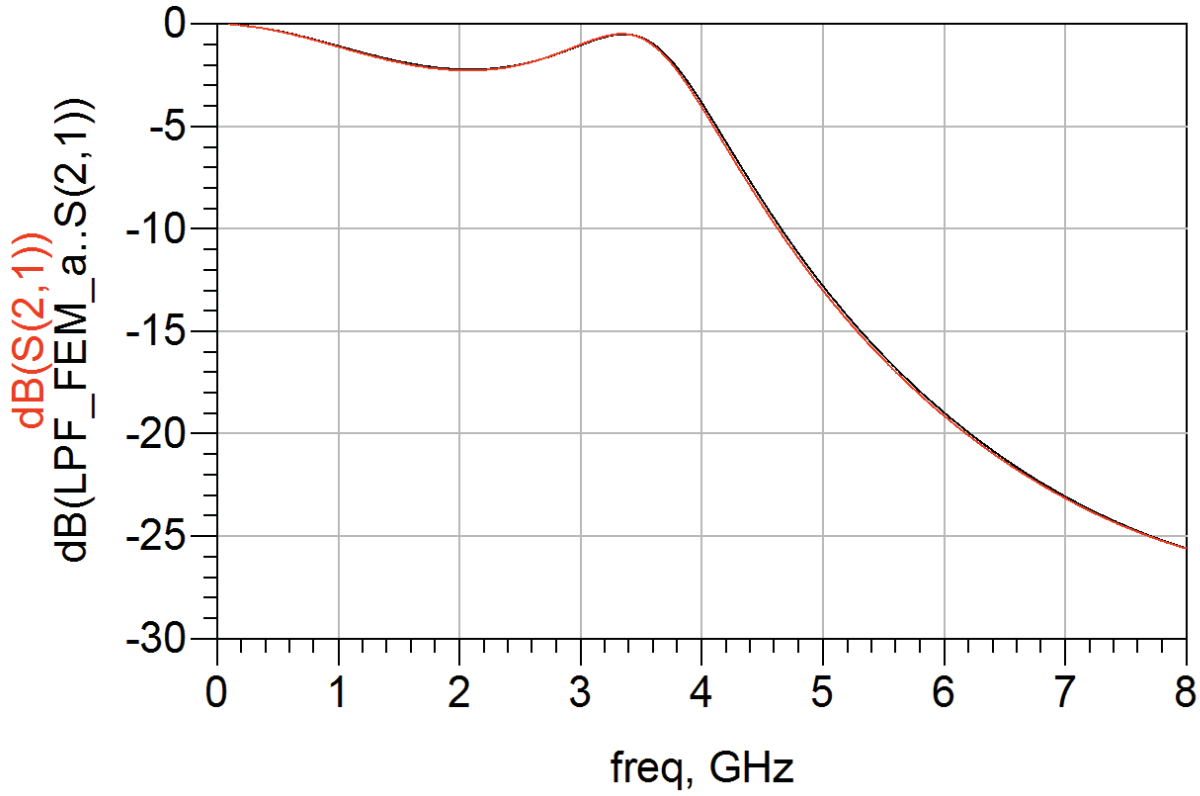
Notice the selection Cross-hair is now available with mouse cursor, click either on the Port 1 or Port2 to apply the symmetry plane, once finished it will appear as below



Note the dotted line which indicates symmetry plane condition.

Step 3: FEM Simulation

FEM simulation steps are exactly the same as described earlier. Follow the same steps and run FEM simulation



From above display it can be seen that results for full structure FEM simulation and Symmetry plane condition are identical.

Comparing simulation statistics of Full FEM and Symmetry Plane condition:

Full FEM Simulation	FEM simulation with Symmetry Plane
INITIAL MESH nbPoints: 188 nbTetrahedra: 618 @Delta Error < 0.01 nbTetrahedra: 4378	**INITIAL MESH** nbPoints: 144 nbTetrahedra: 419 @Delta Error < 0.01 nbTetrahedra: 2145
Solver Time: 2m39s	**Solver Time: 1m47s**

Please note:

1. In this case we do not see great improvement in terms of solver time because of simpler nature of the structure but with more complex problems this difference would be appreciable.
2. Simulations are run on 2GHz, Intel Dual core PC with 4GB RAM.

3. Statistics indicated here might change with software release because of the modification of the internal simulator and mesh algorithms etc.

More details on FEM simulator in ADS, kindly refer to the ADS documentation.

Chapter 6: RF System Design

ADS Licenses Used:

- **RF System Simulation**

Chapter 6: RF System Design

Agilent ADS provides all the necessary capabilities to perform RF system design and simulations. RF system design is an important and critical step to validate the system performance for first pass success. RF system architecture can be implemented using RF System models available in Analog/RF library as shown here.

Filters-Bandpass
Filters-Bandstop
Filters-Highpass
Filters-Lowpass
System-Mod/Demod
System-PLL components
System-Passive
System-Switch & Algorithmic
System-Amps & Mixers
System-Data Models

The library names are self-explanatory and designers can select the desired component from respective library for their system design. It is also recommended to read the documentation of system components for better understanding of the component's behavior, its limitations and recommend simulator which can be used for simulation.

Case Study 1: Receiver System Design

1. Create a new workspace Lab5_RF_System_Design_wrk and open a new schematic cell and name it as Lab5a_RFSystemDesign.
2. Place Amp and Mixer2 from the System-Amps & Mixers library and set their characteristics as shown below

Amplifier2
AMP1
S21=dbpolar(20,0)
S11=dbpolar(-15,0)
S22=dbpolar(-20,180)
S12=dbpolar(-35,0)
NF=1.1 dB
SOI=20
TOI=10

Mixer2
MIX1
SideBand=BOTH
OutputSidebandSuppression=-35 dB
InputImageRejection=-35 dB
ConvGain=dbpolar(-8,0)
SP21=dbpolar(-35,0)
SP31=dbpolar(-35,0)
SP32=dbpolar(-35,0)

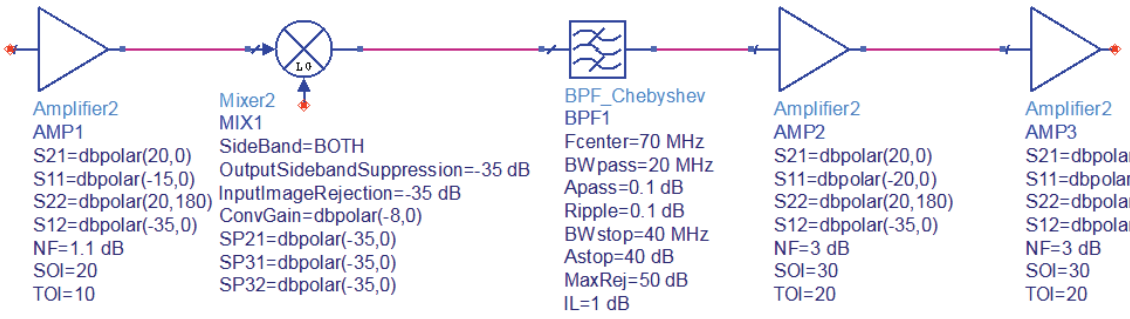
3. Place the **Chebyshev Bandpass filter** component at the Mixer output from **Filters-Bandpass library** and set its characteristics as shown here
4. Copy and paste Amplifier twice after BPF component and change following specifications (these will be used as 2-stage IF Amplifiers)
    a. TOI=20
    b. SOI=30
    c. NF=3 dB

BPF_Chebyshev
BPF1
Fcenter=70 MHz
BWpass=20 MHz
Apass=0.1 dB
Ripple=0.1 dB
BWstop=40 MHz
Astop=40 dB
MaxRej=50 dB
IL=1 dB

Amplifier2
AMP2
S21=dbpolar(20,0)
S11=dbpolar(-20,0)
S22=dbpolar(-20,180)
S12=dbpolar(-35,0)
NF=3 dB
SOI=30
TOI=20

Amplifier2
AMP3
S21=dbpolar(20,0)
S11=dbpolar(-20,0)
S22=dbpolar(-20,180)
S12=dbpolar(-35,0)
NF=3 dB
SOI=30
TOI=20

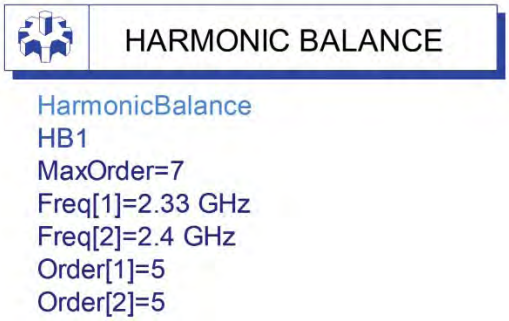
5. Once completed, the schematic will look similar to shown below



6. Now, our job remaining is to connect RF and LO source and setup the simulation to observe the system response. Place **P_1Tone** and Osc source from **Sources-Freq Domain** library and set their characteristics as shown below (***notice the PhaseNoise list in the Osc source..***)

Connect P_1Tone at the Receiver input and Osc at the LO terminal of Mixer component

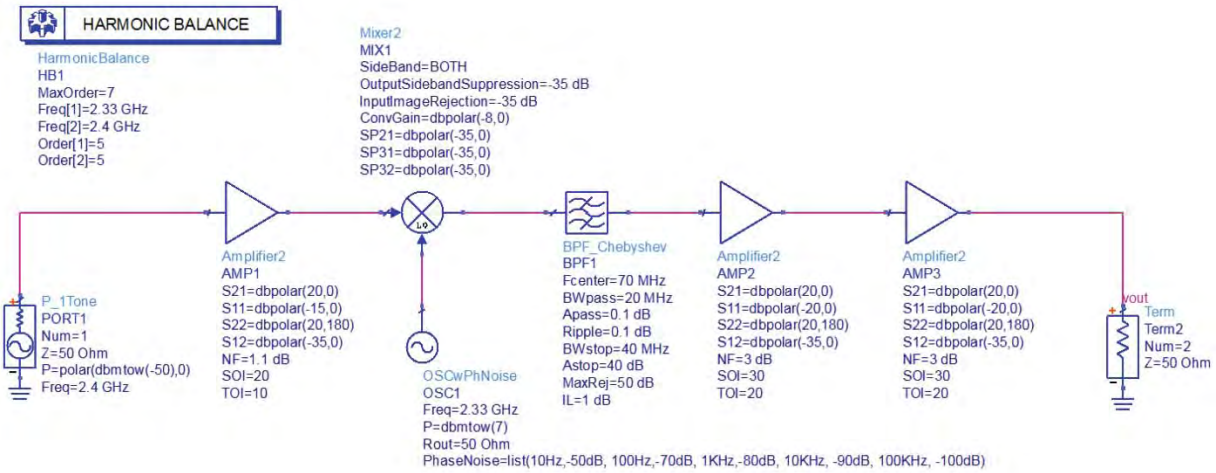
7. Place **HB simulation controller** from **Simulation-HB** library and set its characteristics as show below.
General convention to be followed for simulation involving more than 1 source (or tones) the frequency with more power should be defined first i.e. frequency components should appear in descending order on basis of power. If tones or sources have equal power then designers can decide which frequency to define first.



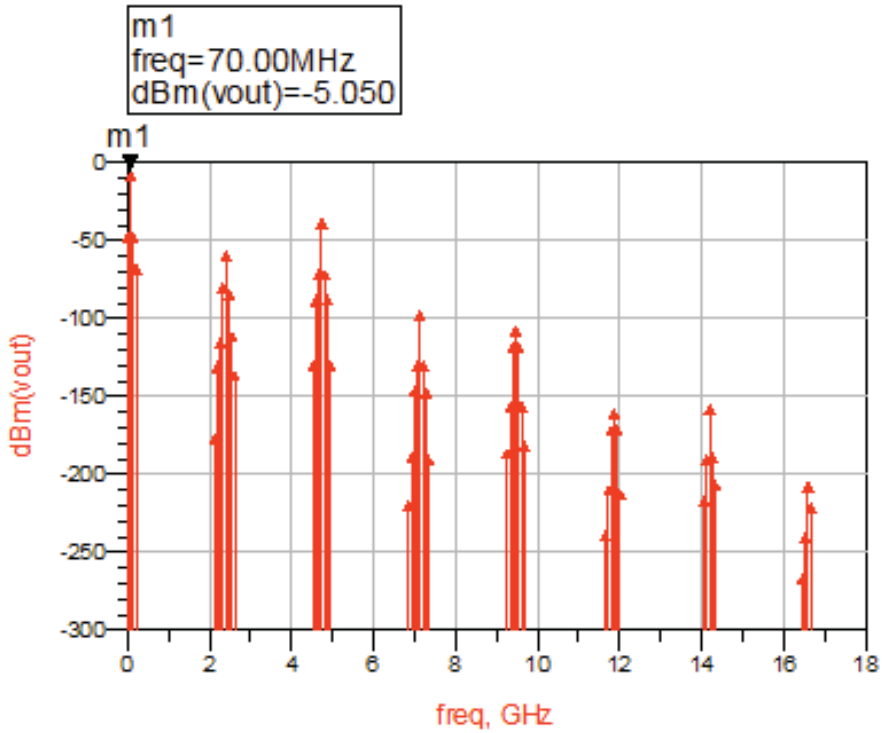
8. Place **Term** component at the output (after 2nd IF amplifier) and click on Wire Label 

and enter **vout** in the pop-up window and click on the "+" terminal of the Term component.

9. Once completed the receiver system diagram would look like as below.



10. Save the design and click on **Simulate** icon. Insert a rectangular graph in data display window & add **"vout"** from the measurement list and select **"Spectrum in dBm"** to observe the output spectrum.

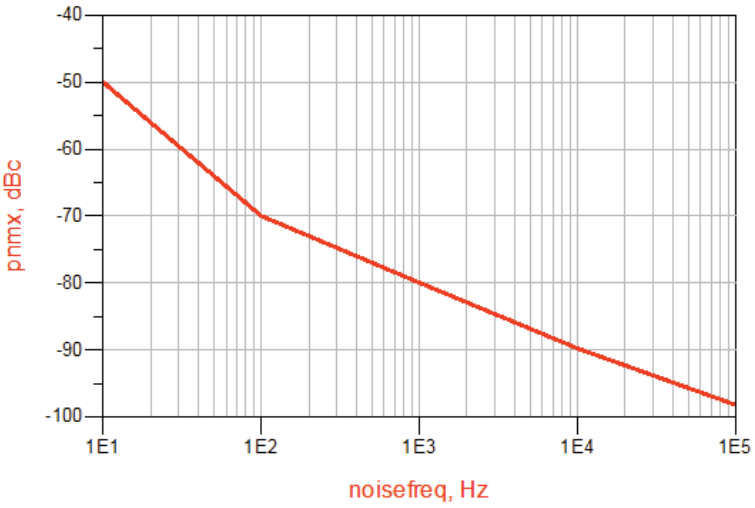


Additional Note: Try giving Wire Label at various points and observe the spectrum at those nodes

Case Study 2: Phase Noise Simulation

Phase noise is an important simulation for receiver systems and the example below shows how to perform Phase noise analysis using Harmonic Balance simulator in ADS.

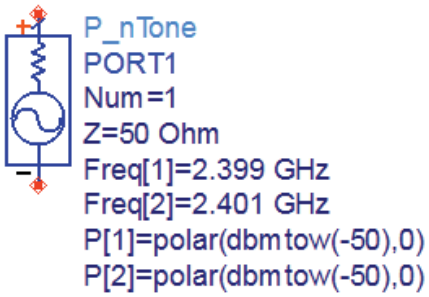
1. Right click on Lab5a_RFSystemDesign and click on Copy Cell
2. In the Pop up window, give new name as Lab5b_RFSystemDesign_PhaseNoise
3. Open the schematic design for this newly copied cell and from Simulation-HB library place NoiseCon (Noise Controller) block onto schematic.
4. Double click to open properties of NoiseCon and set following parameters:
    a. Freq tab:
        i. Sweep Type = Log
        ii. Start = 10 Hz, Stop = 100 KHz
        iii. Num. of pts. will automatically become 5 indicating 5 noise analysis frequencies i.e. 10 Hz, 100Hz, 1KHz, 10KHz and 100KHz which is the same as we are specifying in Oscillator used as LO source in the system
    b. Nodes tab:
        i. Select Pos Node = vout from the drop down box which is the output node where we provided label in earlier lab exercise.
        ii. Click on Add
    c. Phase Noise Tab:
        i. Phase Noise Type = Phase Noise Spectrum
        ii. Under Specify Phase Noise Carrier specify Frequency as 70 MHz, alternatively we can also specify Carrier mixing indices such as {-1,1} etc
5. Click OK and now our Noise Controller is setup nicely, we have one extra step in linking this Noise Controller to our HB simulation controller
6. Double click on HB controller, and go to Noise Tab
    a. Check Noise Cons option
    b. From Edit drop down box select NC1 (name of Noise controller)
    c. Click on Add
    d. Click OK and close the HB simulation controller properties box.
7. Run simulation and a new data display window will come up. Insert a new rectangular plot and select vout to be plotted in dBm to see the spectrum same as in earlier lab.
8. Insert a new rectangular plot, select pnmx (i.e. Phase Noise) to be plotted and from Plot Options change the X-axis as Log. Click OK to see the Phase Noise plot at various offsets.



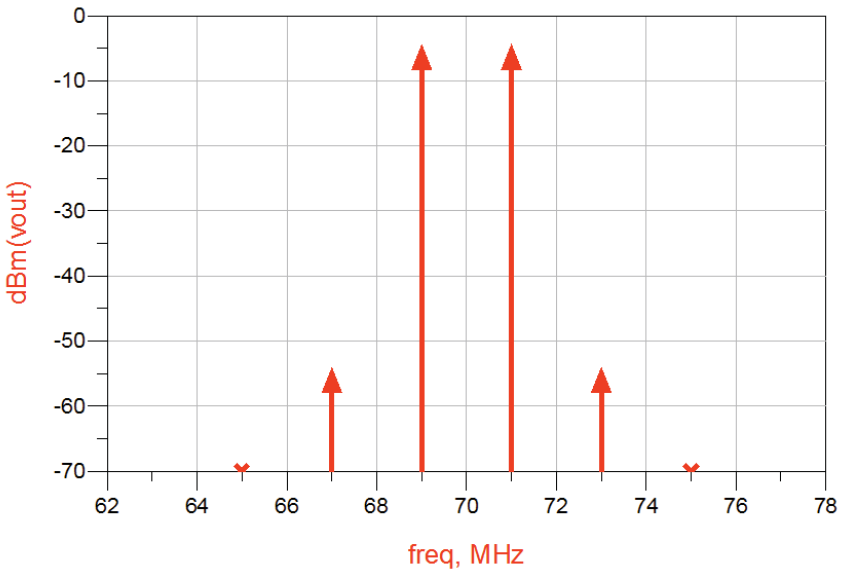
Case Study 3: 2-Tone Simulation of Receiver System

Performing 2-tone simulation is also of specific importance for system level analysis and example here shows how to perform 2-tone simulations on frequency converting based systems.

1. Right click on Lab5a_RFSystemDesign and click on Copy Cell
2. In the Pop up window, give new name as Lab5c_RFSystemDesign_2Tone and click OK
3. Open the schematic of newly copied cell. For 2-tone simulation we need to change the P_1Tone source which is currently used for the RF source. Delete the 1-tone source and from **Sources-Freq Domain** library place **P_nTone** source on schematic.
4. Double click on the P_nTone source and edit the properties as below:
    a. Click on Freq[1] and enter frequency as 2.399 GHz, click Apply
    b. Click on Add button to add 2nd tone frequency with the name Freq[2] and enter the frequency as 2.401 GHz, click Apply.
    c. Click on P[1] which is power in 1st tone, enter the power as polar(dbmtow(-50),0) and click on Apply
    d. Click on Add button to add power for 2nd tone and enter the same power as for 1st tone. Please note that for 2-tone test it is mandatory to have same power in both of the tones else the analysis will not be valid.



5. Now, as we have 3 source frequencies in the schematic, we need to modify the HB simulator to specify these 3 frequencies for proper mixing product calculations. Double click on HB controller and specify 3 frequencies in order as following
    a. Freq[1] = 2.33 GHz
    b. Freq[2] = 2.399 GHz
    c. Freq[3] = 2.401 GHz
6. Click on Simulate button to run simulation and then zoom using graph zoom icon on data display near 70MHz to see 2-tone simulation results as shown below.

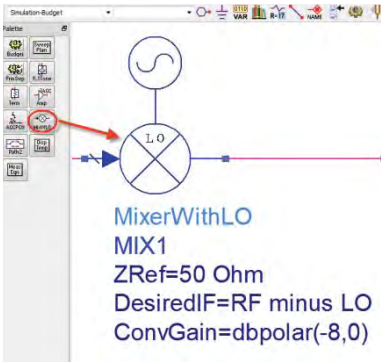


Case Study 4: RF System Budget Analysis

Performing RF System Budget is very useful to characterize the system behavior and analyze how system behaves as the signal transitions from each component. Easiest way to perform RF System Budget analysis is using Budget Controller which offers more than 40 built-in budget measurements offering great ease-of-use.

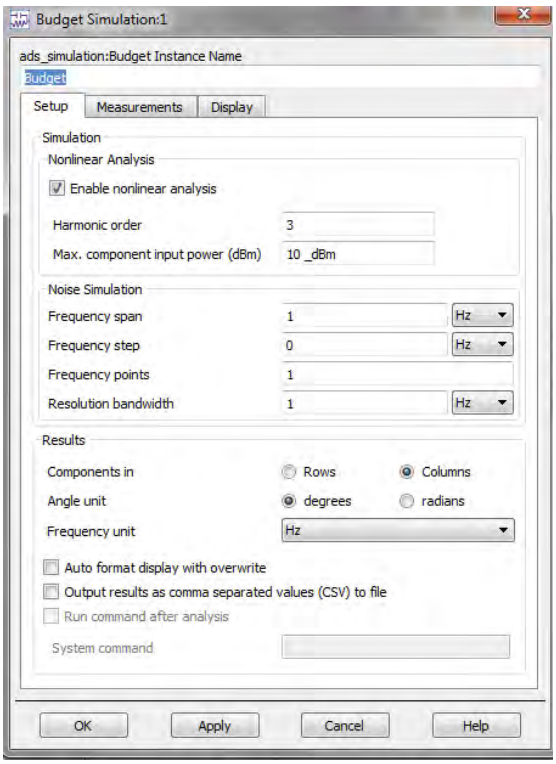
One of the fundamental rules to follow while using Budget Controller is that system should only have 2-port components with exception of S2P files, AGC Amplifier with Power Control. ADS Simulation-Budget library provides special Mixer with Internal LO so that super-heterodyne type of systems can be analyzed.

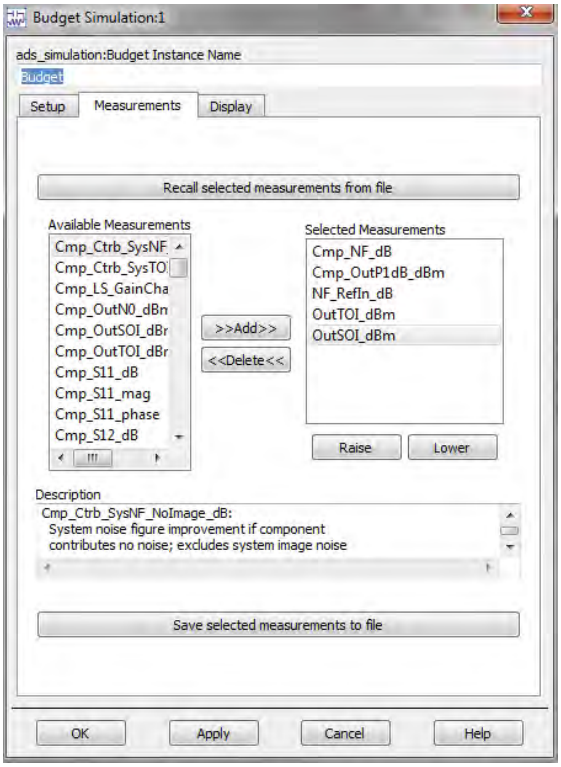
Step1: Modifying the RF system design



1. Copy **Lab5a_RFSystemDesign** cell by right clicking and selecting Copy Cell and provide the new name as **Lab5d_RFSystemDesign_Budget**
2. In order to perform budget analysis on our receiver system, we need to replace the Mixer and LO source component by Mixer with LO component from Simulation-Budget library as shown here.

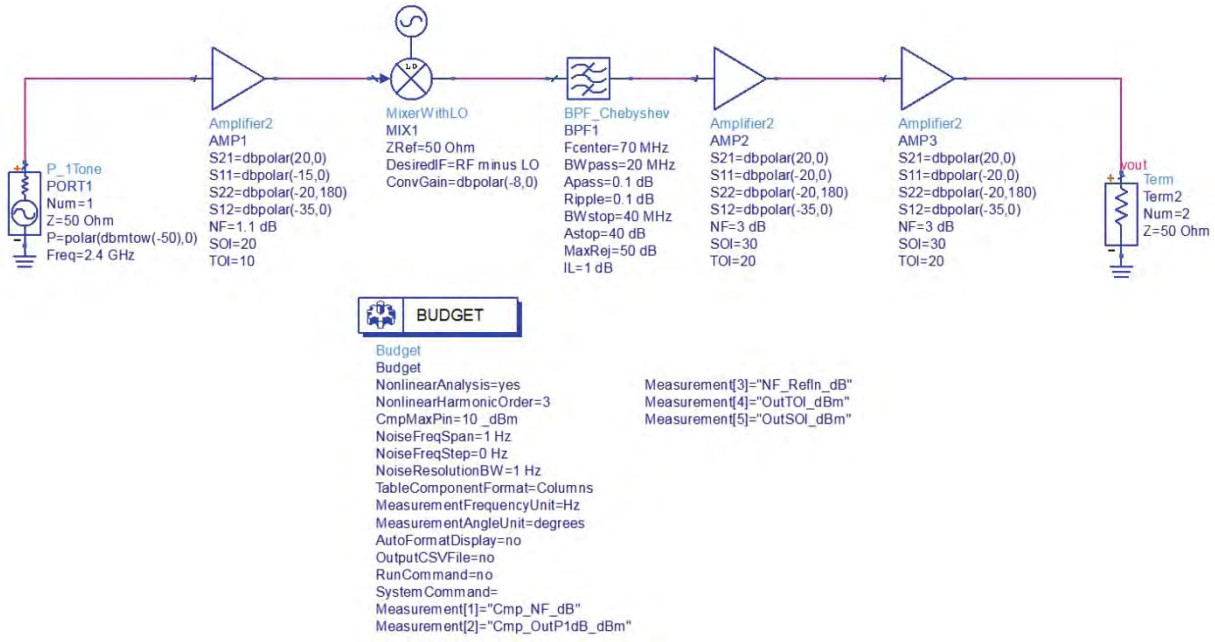
   Modify following parameters-
   ConvGain=dbpolar(-8,0)
   Desired IF = RF minus LO
3. Delete the HB controller and insert the Budget controller from Simulation-Budget library, double click on it and modify the parameters under Setup tab as shown below. From the measurements tab select measurements as shown below (namely: Cmp_NF_dB, Cmp_OutP1dB_dBm, NF_Refln_dB, OutTOI_dBm, OutSOI_dBm)



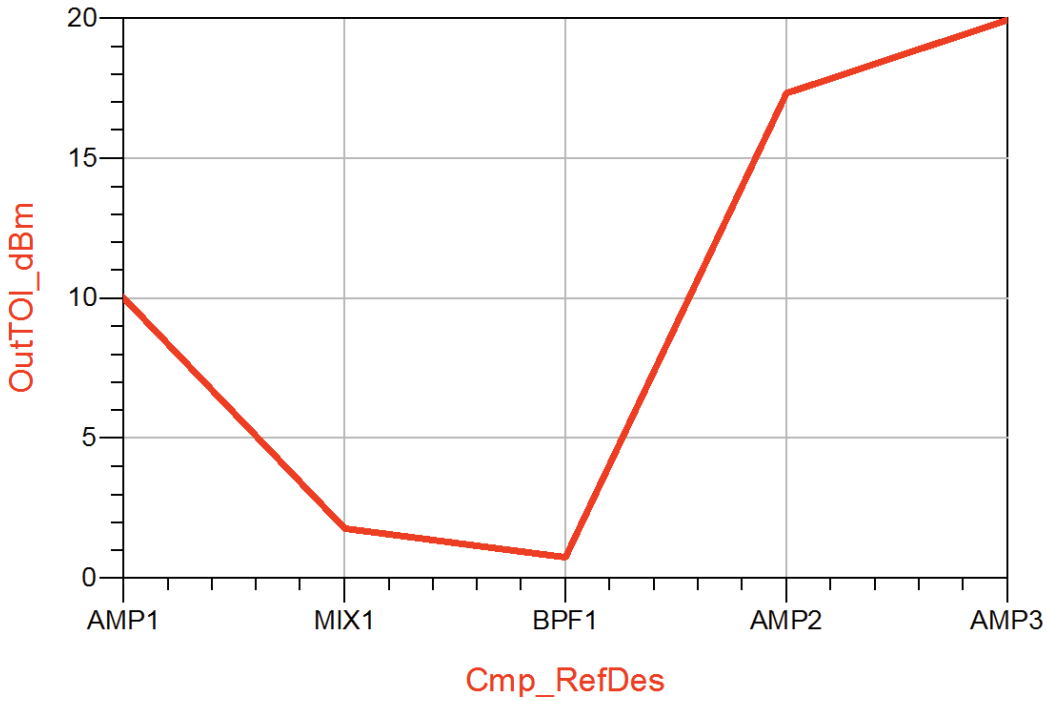


Step2: Perform Budget Analysis

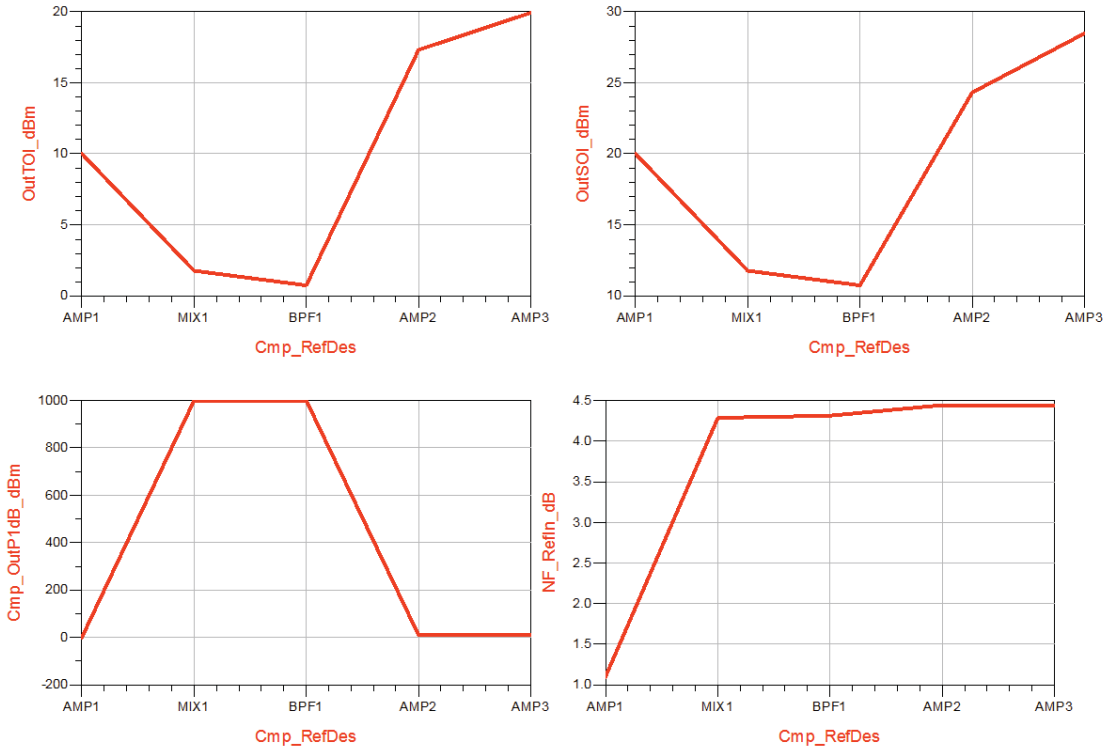
1. Overall schematic should look similar to the one shown below, click on Simulate button



2. Insert Rectangular graph in the data display page. Select **OutTOI_dBm** from the measurement list, click on **Add Vs>>** button and select **Cmp_RefDes** to plot budget measurement results vs. component names so that it is easier to see results vs. Component Names as used in RF System design schematic. ***(Notice the X-axis which should display the name of the system components)***



3. Similar add **OutSOI_dBm, Cmp_OutP1dB_dBm, NF_Refln_dB vs. Cmp_ResDes** to see different budget measurements as shown below.

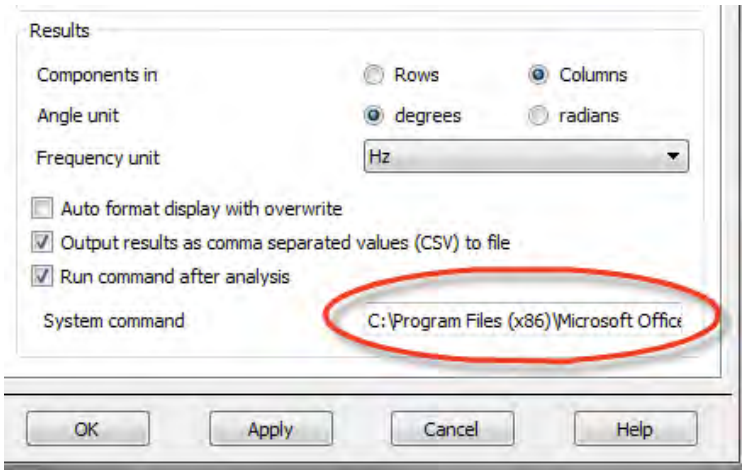


Question: Why Receiver's Noise Figure is @4.5dB? Is it too high or as expected? Try comparing it against theoretical calculations using Cascaded Noise Figure equation.

Case Study 5: Exporting RF Budget Analysis results to Excel

ADS budget controller allows exporting the budget simulation results to Microsoft Excel. In order to activate this feature double click on Budget Controller and select the options as shown below. Also we need to enter the path to Excel.exe as per our installation

e.g. in case below it is **C:\Program Files (x86)\Microsoft Office\Office12\Excel.exe**



Click on Simulate icon to see Excel open up with our budget simulation results. Scroll down on the excel sheet and notice budget simulation results as shown in snapshot below

42	Meas_Name	AMP1	MIX1	BPF1	AMP2	AMP3
43	Cmp_NF_dB	1.131617	8.036397	1.021553	3.021827	3.021827
44	Cmp_OutP1dB_dBm	-0.63804	1000	1000	9.366897	9.366965
45	NF_RefIn_dB	1.1	4.285689	4.312709	4.441894	4.443175
46	OutTOI_dBm	10	1.755889	0.729914	17.30733	19.91895
47	OutSOI_dBm	20	11.75589	10.72991	24.30329	28.46084
48						

Chapter 7: Microwave Discrete and Microstrip Filter Design

ADS Licenses Used:

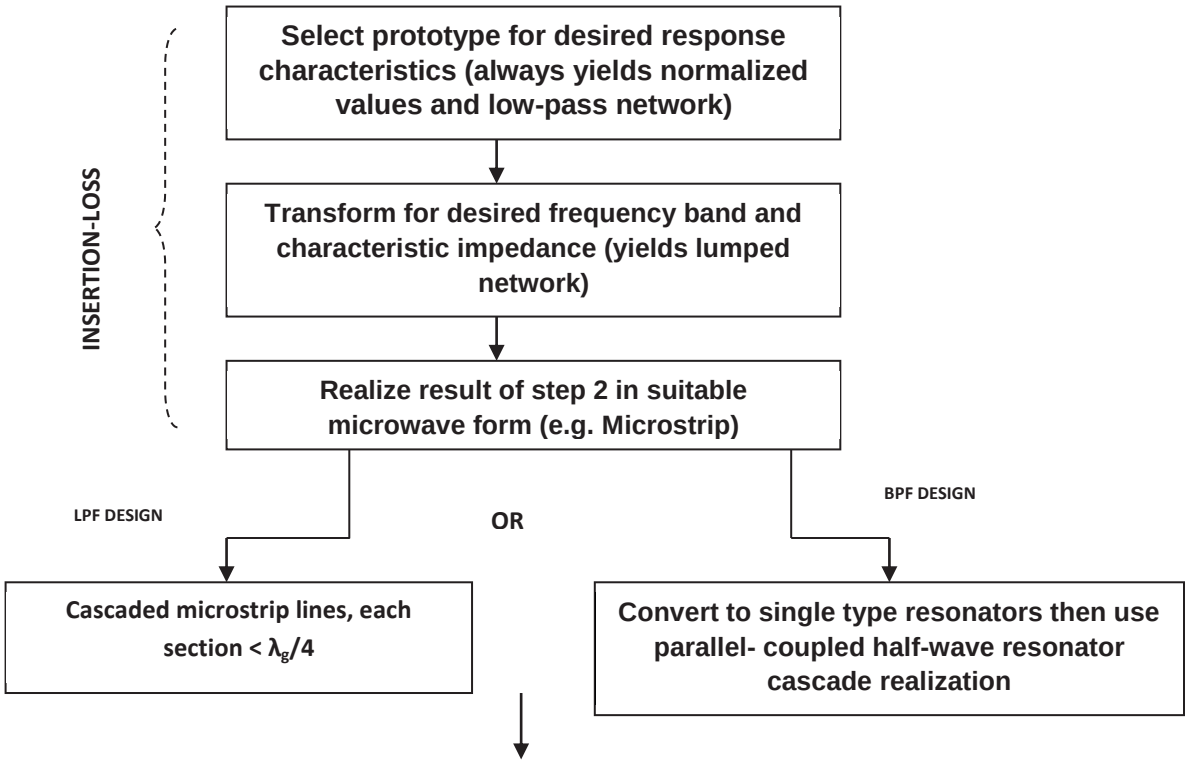
- **Linear Simulation**
- **Momentum Simulation**
- **Layout**

Chapter 7: Microwave Discrete and Microstrip Filter Design

Theory:

Microwave filters play an important role in any RF front ends for the suppression of out of band signals. They in the lumped and distributed form are extensively used for both commercial and military applications. A filter is reactive network that passes desired band of frequencies while almost stops all other band of frequencies. The frequency that separates the transmission band from the attenuation band is called the cut-off frequency and denoted as f_c. The attenuation of the filter is denoted in decibels or nepers. A filter in general can have any number of pass bands separated by stop bands. They are mainly classified in to four common types namely lowpass, highpass, bandpass and band stop filters.

An ideal filter should have zero insertion loss in the pass band, infinite attenuation in the stop band and a linear phase response in the pass band. Ideal filter cannot be realizable as the response of an ideal low pass or band pass filter is rectangular pulse in frequency domain. When converting this rectangular pulse into time domain results in **sinc** function which makes the filter system to be causal. Hence ideal filter is not realizable hence the art of filter design necessitates compromises with respect to cutoff and roll off. There are basically three methods for filter synthesis. They are Image parameter method, Insertion loss method and numerical synthesis. The image parameter method is an old and crude method whereas the numerical method of synthesis is novel but cumbersome. The insertion loss method of filter design on the other hand is the optimum and more popular method for higher frequency applications. The filter design flow for insertion loss method is shown in figure below.



Since characteristics of an ideal filter cannot be obtained, the goal of filter design is to approximate the ideal requirements within an acceptable tolerance. There are four types of approximations namely Butterworth or maximally flat, Chebyshev, Bessel and Elliptic approximations. For the proto type filters, maximally flat or Butterworth provides the flattest pass band response for a given filter order. In the Chebyshev method, sharper cutoff is achieved and the pass band response will have ripples of amplitude $1+k^2$. Bessel approximations are based on the Bessel function which provides sharper cutoff and Elliptic approximations results in pass band and stop band ripples. Depending on applications and the cost the approximations can be chosen. The optimum filter is Chebyshev filter with respect to response and the bill of materials. Filter can be designed both in the lumped and distributed form using the above approximations.

Design of Microwave Filters:

The first step in the design of Microwave filter is to select a suitable approximation of the prototype model based on the specifications.

Calculate the order of the filter from the necessary roll off as per the given specifications.

The order can be calculated as follows

Butterworth Approximation:

$L_A(\omega') = 10\log_{10}\{1+\varepsilon\,(\omega'/\omega_c)^{2N}\}$

Where $\varepsilon = \{\text{Antilog}_{10} L_A/10\} - 1$ and L_A = 3dB for Butterworth

Chebyshev Approximation:

$$L_A(\omega') = 10\log_{10}\left\{1+\varepsilon\cos^2\left[n\cos^{-1}\left(\frac{\omega'}{\omega_1'}\right)\right]\right\} \quad \text{when } \omega' \le \omega_1' \text{ and}$$

$$L_A(\omega') = 10\log_{10}\left\{1+\varepsilon\cosh^2\left[n\cosh^{-1}\left(\frac{\omega'}{\omega_1'}\right)\right]\right\} \quad \text{when } \omega' \ge \omega_1'$$

Where ω_c is the angular cutoff frequency

ω' is the angular attenuation frequency

$L_A(\omega')$ is the attenuation at ω'

N is the order of the filter

$\varepsilon = \{\text{Antilog}_{10} L_{Ar}/10\} - 1$ and L_{Ar} = Ripple in passband

The next step in the filter design is to calculate the prototype values of the filter depending on the type of approximation. The prototype values for the Chebyshev and Butterworth approximations can be calculated using the given equations

Butterworth Approximation

$g_0 = 1$,

$g_k = 2\sin\{(2k-1)\pi/2n\}$ where k = 1,2,.....n and

$g_{N+1} = 1$

Where n is the order of the filter

Chebyshev Approximation

The element values may be computed as follows

$\beta = \ln\left(\coth\frac{L_{Ar}}{17.37}\right)$ L_{Ar} is the ripple in the passband

$\gamma = \sinh\left(\frac{\beta}{2n}\right)$

$a_k = \sin\left[\frac{(2^k - 1)\pi}{2n}\right]$, k=1, 2, 3....n

$b_k = \gamma^2 + \sin^2\left(\frac{k\pi}{n}\right)$, k=1, 2, 3....n

$g_1 = \frac{2a_1}{\gamma}$

$g_k = \frac{4a_{k-1}a_k}{b_{k-1}g_{k-1}}$, k=2, 3.....n

g_{n+1} =1 for n odd

$= \coth^2\left(\frac{\beta}{4}\right)$ for n even.

After computing the prototype values the prototype filter has to be transformed with respect to frequency and impedance to meet the specifications. The transformations can be done using the following equations.

For Lowpass filter:

After Impedance and frequency scaling:

$C'_k = C_k / R_0 \omega_c$

$L'_k = R_0 L_k / \omega_c$ Where $R_0 = 50\Omega$

For distributed design the electrical length is given by

Length of capacitance section: $Z_l / R_0 C_k$,

Length of inductance section: $L_k R_0 / Z_h$

Where Z_l is the low impedance value and Z_h is the high impedance value

For bandpass filter:

Impedance and frequency scaling:

$L'_1 = L_1 Z_0 / \omega_0 \Delta$

$C'_1 = \Delta / L_1 Z_0 \omega_0$

$L'_2 = \Delta Z_0 / \omega_0 C_2$

$C'_2 = C_2 / Z_0 \Delta \omega_0$

$L'_3 = L_3 Z_0 / \omega_0 \Delta$

$C'_3 = \Delta / L_3 Z_0 \omega_0$

Where Δ is the fractional bandwidth $\Delta = (\omega_2 - \omega_1) / \omega_0$

Simulation of a Lumped and Distributed Lowpass filter using ADS:

Typical Design:

Cutoff Frequency (f_c) : 2 GHz

Attenuation at (f = 4 GHz) : 30dB (LA(ω))

Type of Approximation : Butterworth

Order of the filter:

$$LA(\omega) = 10\log_{10}\{1+\varepsilon(\omega/\omega_c)^{2N}$$

Where

$$\varepsilon = \{\text{Antilog}_{10} LA/10\} - 1$$

Substituting the values of LA (ω), ω and ω_c, the value of N is calculated to be 4.

Prototype Values of the lowpass Filter:

The prototype values of the filter is calculated using the formula given by

$g_0 = 1$,

$g_k = 2\sin\{(2k-1)\pi/2N\}$ where k = 1,2,.....N

and $g_{N+1} = 1$

The prototype values for the given specifications of filter are

g1 = 0.7654 = C_1, g2 = 1.8478 = L_2, g3 = 1.8478 = C_3 & g4 = 0.7654 = L_4

Lumped Model of the Filter

The Lumped values of the Lowpass filter after frequency and impedance scaling are given by

$C_k' = C_k / R_0\omega_c$

$L_k' = R_0 L_k/\omega_c$ where R_0 is 50Ω

The resulting lumped values are given by C_1' = 1.218 pF, L_2' = 7.35 nH, C_3' = 2.94 pF and L_4' = 3.046 nH

Distributed Model of the Filter

For distributed design the electrical length is given by

Length of capacitance section (βLc) : $C_k Z_l/R_0$,

Length of inductance section (βLi) : $L_k R_0/Z_h$

Where Z_l is the low impedance value,

Z_h is the high impedance value,

R_0 is the Source and load impedance,

ω_c is the desired cutoff frequency

If we consider $Z_l = 10\Omega$ and $Z_h = 100\Omega$ then $\beta Lc_1 = 0.153$, $\beta Li_2 = 0.9239$,

$\beta Lc_3 = 0.3695$ and $\beta Li_4 = 0.3827$

Since $\beta = 2\pi/\lambda$, the physical lengths are given by

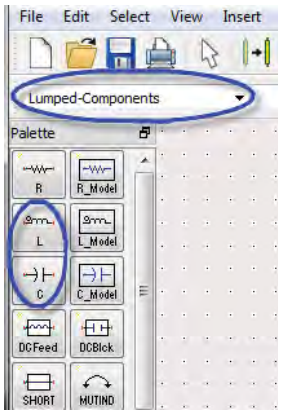
$Lc_1 = 1.68$ mm,

$Li_2 = 10.145$ mm,

$Lc_3 = 4.057$ mm and

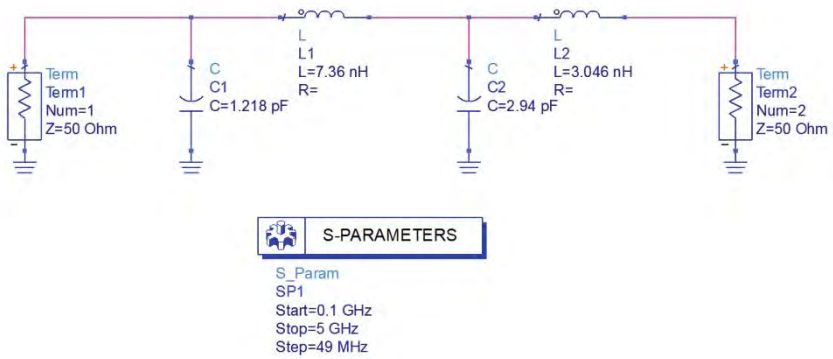
$Li_4 = 4.202$ mm.

Schematic Simulation steps for Lumped Low Pass Filter:

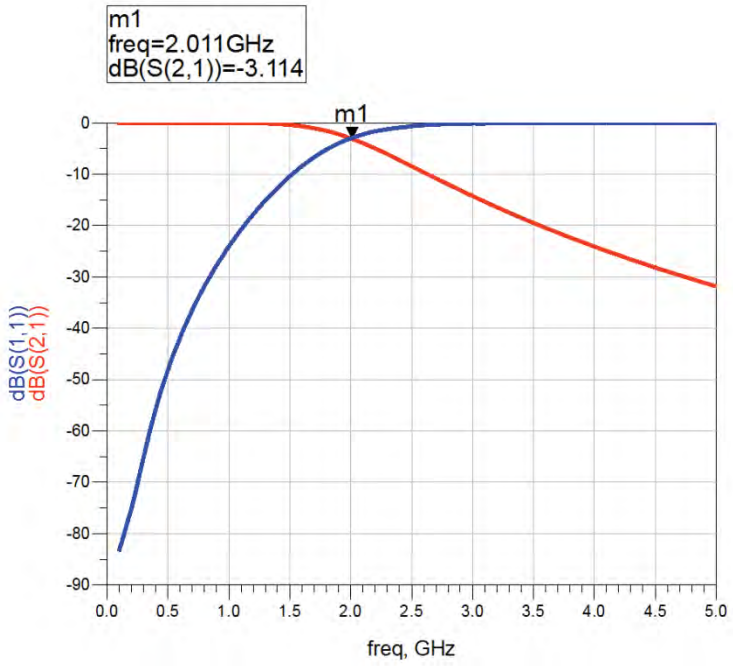


1. Open the Schematic window of ADS
2. From the Lumped Components library select the appropriate components necessary for the lumped filer circuit. Click on the necessary components and place them on the schematic window of ADS as shown in figure 2.
3. Create the lumped model of the lowpass filter on the schematic window with appropriate lumped components and connect the circuit elements with wire. Enter the component values as calculated earlier.
4. Terminate both the ports of the lowpass filter using terminations selected from the Simulation-S_Param library.
5. Place the S-Parameter simulation controller from Simulation-S_Param library and set its parameters as:
   Start = 0.1 GHz
   Stop = 5 GHz
   Number of Points=101 (or enter Step Size = 49 MHz)

This completes the lumped model design of the filter as shown in figure below.



6. Simulate the circuit by clicking F7 or simulation gear icon.
7. After the simulation is complete the ADS automatically open the Data Display window displaying the results. If the Data Display window does not open click Window>>New Data Display. In the data display window select a rectangular plot and this automatically opens the place attributes dialog box. Select the traces to be plotted (in our case S(1,1) & S(2,1) are plotted in dB) and click on Add>>.
8. Click OK and insert a marker on S(2,1) trace around 2GHz to see the data display graph as shown below.



Results and Discussions:

It is observed from the schematic simulation that the lumped model of the lowpass filter has a cutoff of 2 GHz and a roll off as per the specifications.

Layout Simulation steps for Distributed Low Pass Filter:

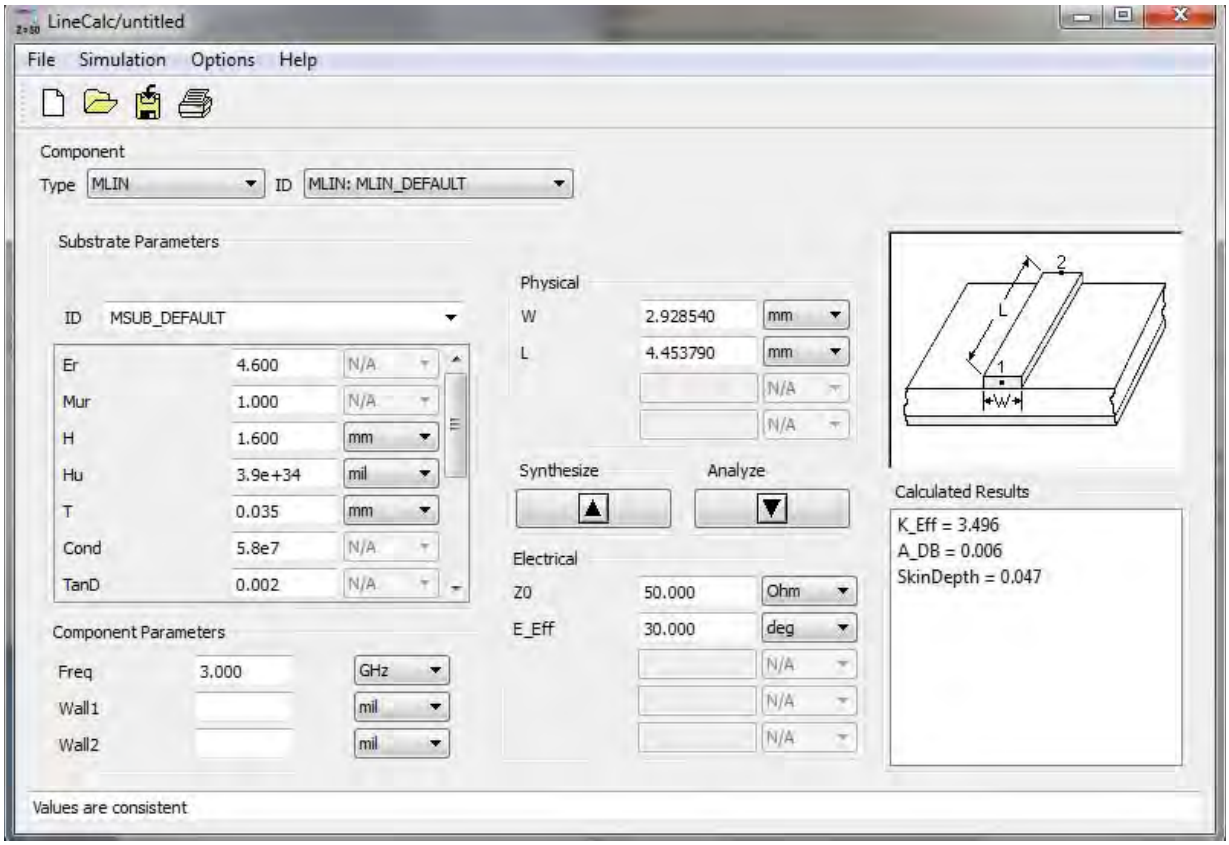
Calculate the physical parameters of the distributed lowpass filter using the design procedure given above. Calculate the width of the Z_l and Z_h transmission lines for the design of the stepped impedance lowpass filter. In this case Z_l = 10Ω and Z_h = 100Ω and the corresponding line widths are 24.7 mm and 0.66mm respectively for a dielectric constant of 4.6 and a thickness of 1.6 mm.

Calculate the length and width of the 50 Ω line using the line calc (Tools->Line Calc->Start Line Calc) window of ADS as shown in figure below.

50 Ω Line input & output connecting line:

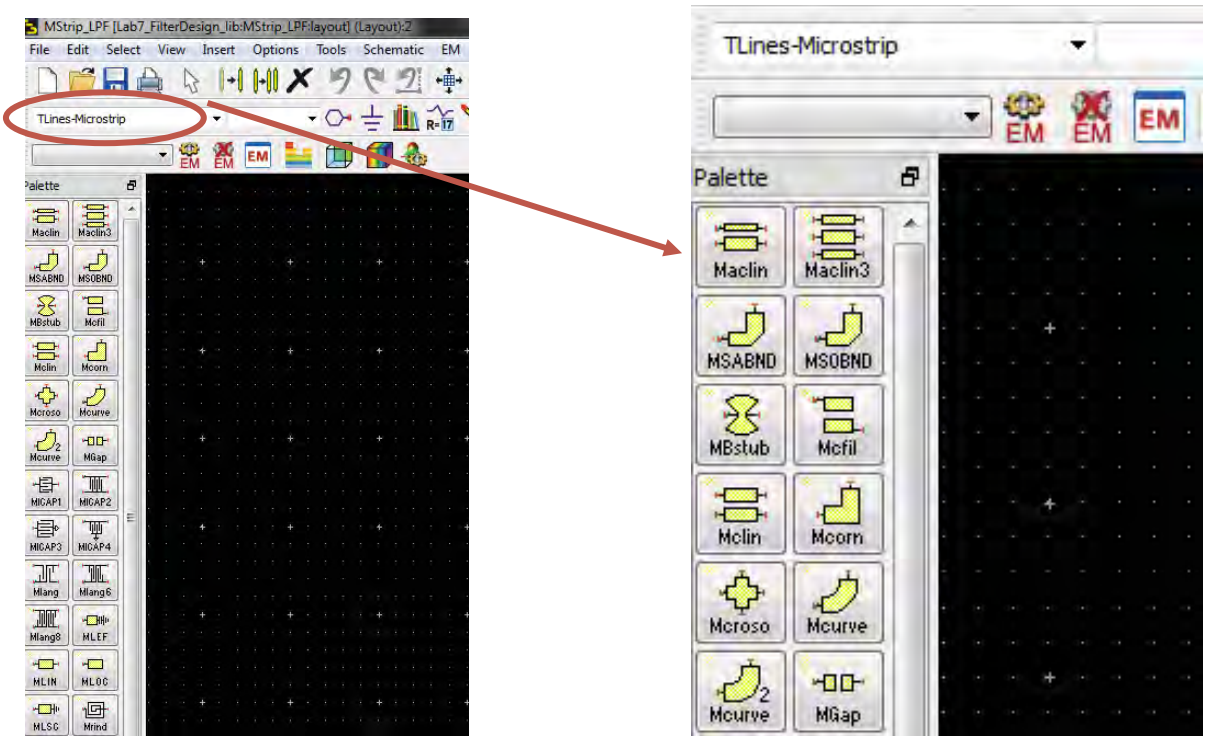
Width: 2.9 mm

Length: 4.5 mm

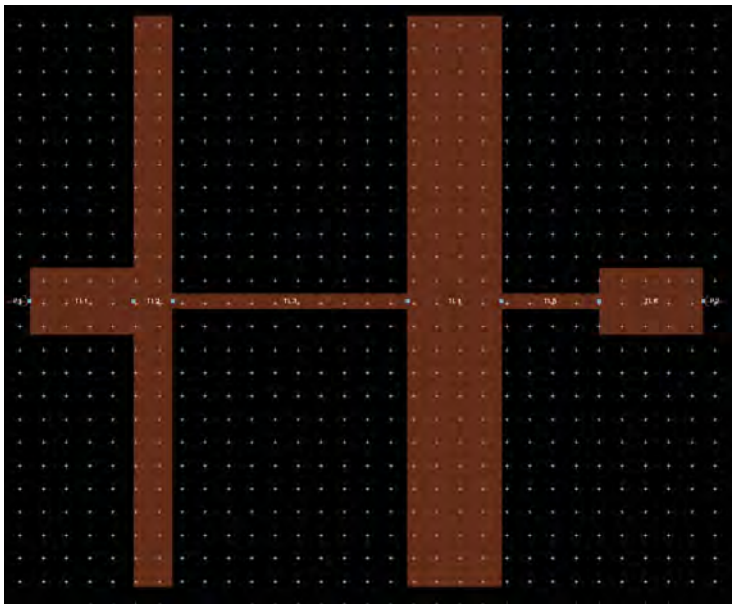


Create a model of the lowpass filter in the layout window of ADS. The Model can be created by using the available library components **or** by drawing rectangles.

To create the model using library components select the **TLines–Microstrip** library. Select the appropriate Microstrip line from the library and place it on the layout window as shown.



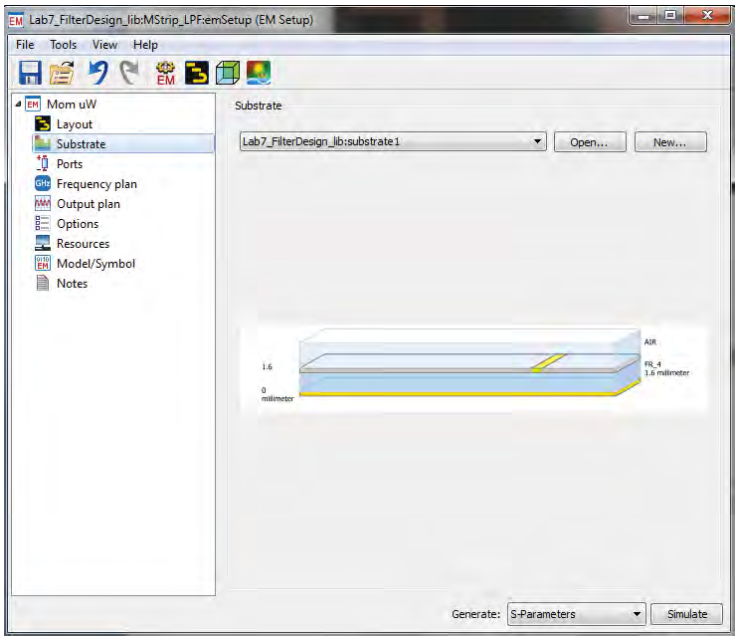
Complete the model by connecting the transmission lines to form the stepped impedance lowpass filter as shown in figure below based on the width & length calculations done earlier.



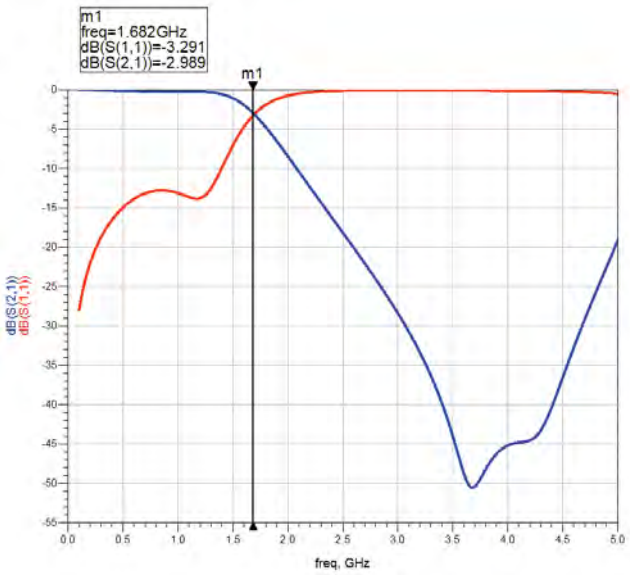
Connect Pins at input & output and define the substrate stackup and setup EM simulation as described in EM simulation chapter earlier. We shall use following properties for stackup:

Er=4.6
Height = 4.6 mm
Loss Tangent = 0.0023
Metal Thickness = 0.035 mm
Metal Conductivity = Cu (5.8E7 S/m)

In the EM setup window, go to Options->Mesh and switch on the Edge Mesh



Click on Simulate button and observe the S11 and S21 response

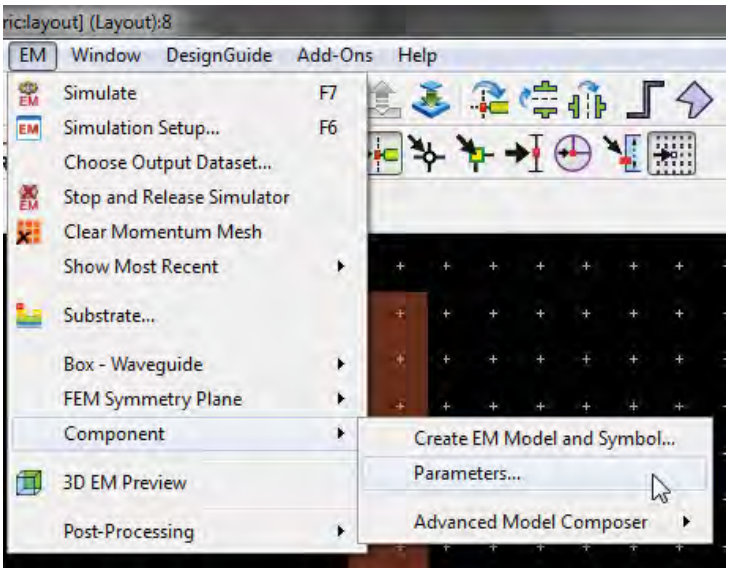


It can be noted that 3dB cut-off has shifted to 1.68GHz instead of 2 GHz as our theoretical calculations doesn't allow accurate analysis of open end effect and sudden impedance change of the transmission lines hence the lengths of the lines needs to optimized little bit to recover the desired 2GHz cutoff frequency specifications.

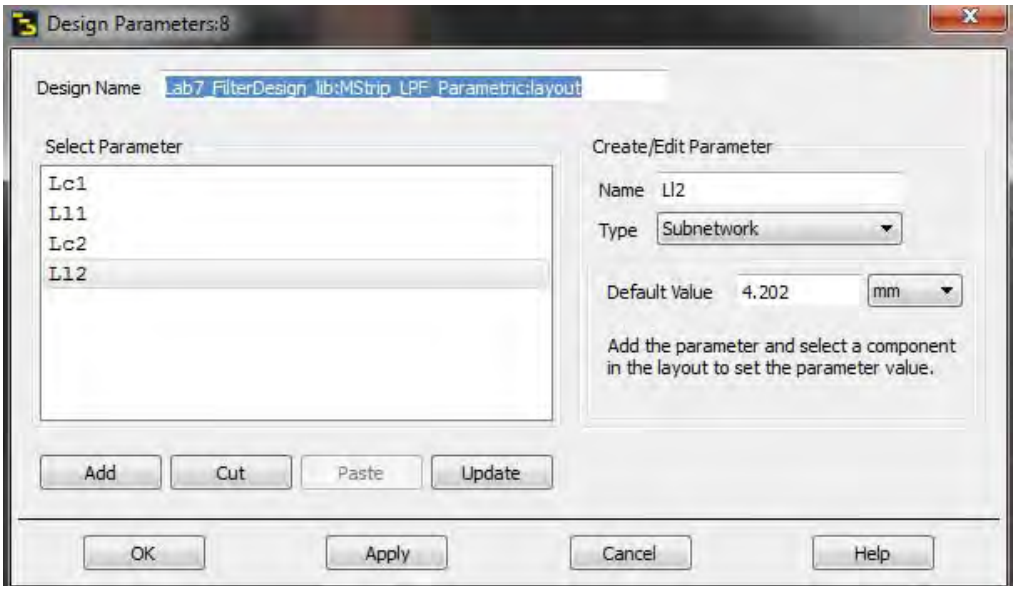
This optimization can be carried out using Momentum simulator in ADS or by performing parametric sweep on the lengths of Capacitive and Inductive lines.

Parametric EM simulations in ADS2011:

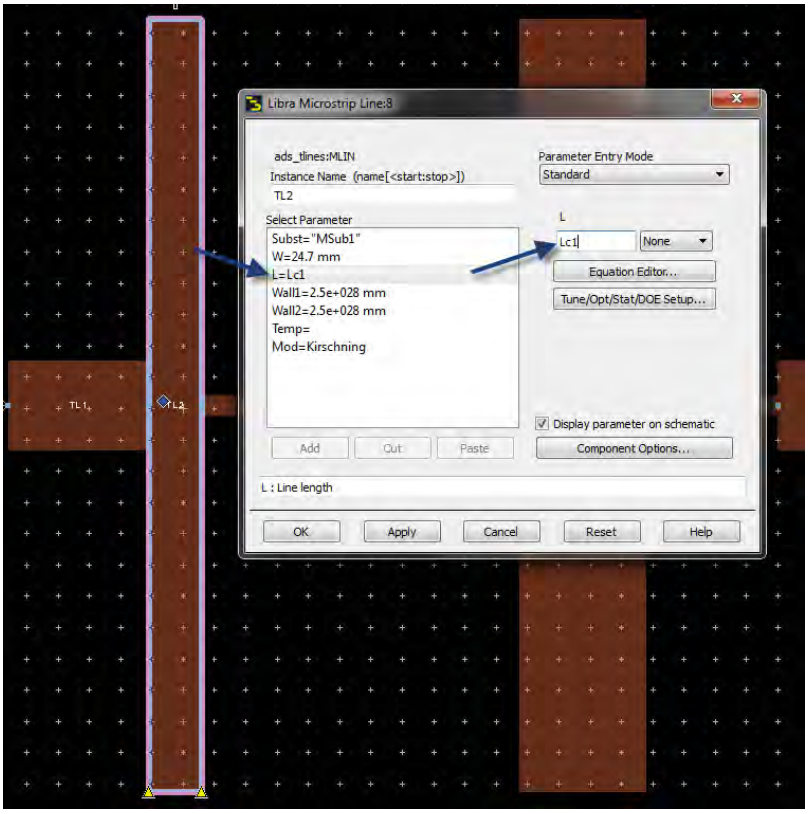
To begin parametric simulation on the layout, we need to define the variable parameters which shall be associated with the layout components. Click on EM->Component->Parameters as shown below



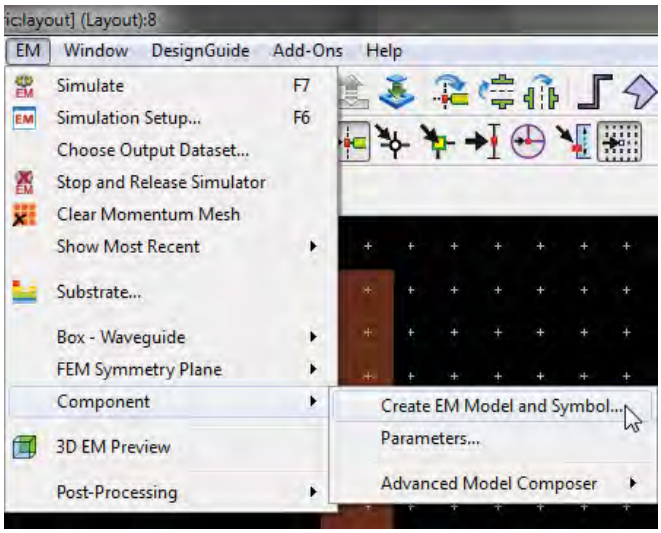
In the parameter pop-up window, define 4 variables for capacitive and inductive lines and enter their nominal values alongwith the corresponding units and choose **Type = Subnetwork** as these parameters will be associated with Microstrip library components which has parameterized artwork. If we are trying to parameterize the polygon/rectangle based components then we can select Nominal/Perturbed method which requires additional attention to the way component gets parameterized.



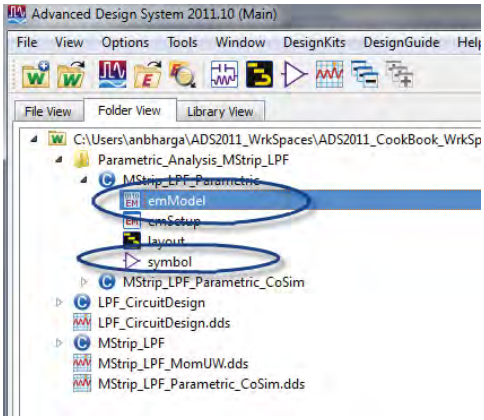
Once the parameters have been added in the list, double click on the respective components and insert the corresponding variable names, pls note that no units needs to be defined here as we have already defined units in the variable parameter list. Example of one component has been shown below:



After defining all the parameter values in the desired layout components we can create a EM model and symbol which shall then be used for parametric EM cosimulation in schematic. To create a parametric model and symbol for the layout, click on EM->Component->Create EM Model and Symbol.

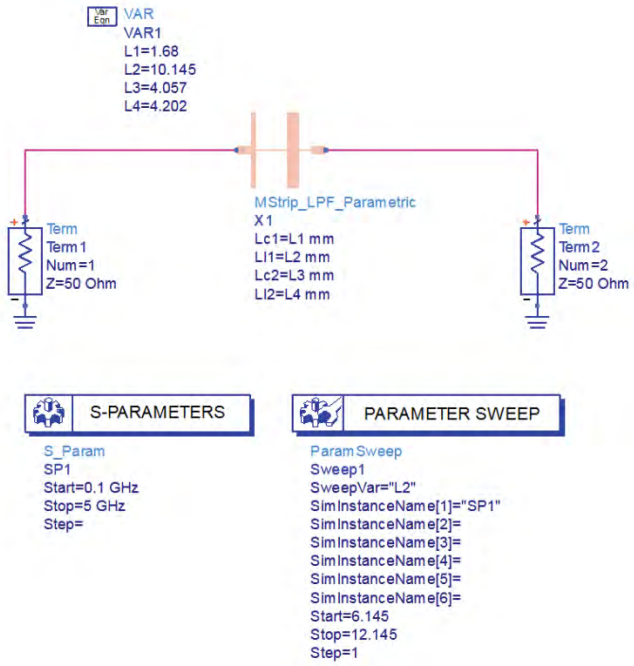


Once done, observe the main ADS window where it would display the name of the emmodel and symbol below the layout cell name as shown below:

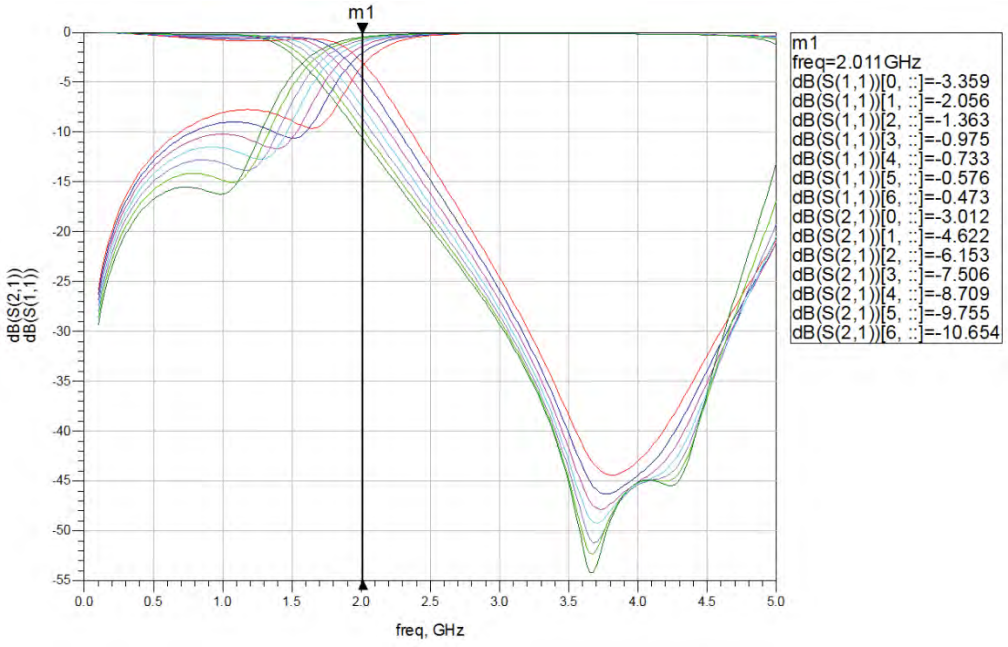


Open a new schematic cell and drag and drop the emModel component to place it as subcircuit. You will notice the defined parameters being added to the emModel component which can then be swept using regular Parameter Sweep component in ADS schematic as shown below. In this case, we have defined variables L1-L4 and assigned it to the emModel component. To start with, we sweep length of L2 (1st inductive line) from 6.145 to 12.145 in steps of 1.

At this stage we can decided to setup optimization and then optimize the layout component variables like any other circuit optimization but please note that EM optimization will have longer time as compared to circuit based optimization but produces more accurate response as EM simulation will be performed for every combination.

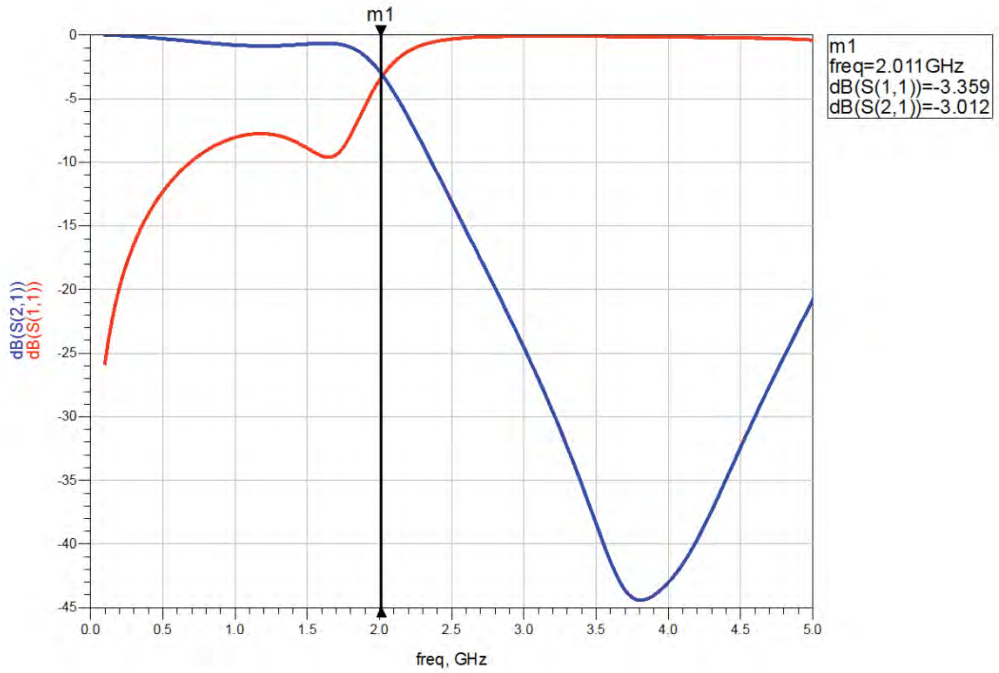


Click on Simulate icon and plot the graph in data display window to see how filter response changes with length of 1st inductive line



From the data display, we can see that 1st sweep value of L2 is providing 3dB cutoff at 2 GHz i.e. L2=6.145 mm seems to be the correct value.

Disable the parameter sweep and change the value of L2 = 6.145 mm and perform the simulation again to see the filter response. Circuit can be EM optimized if better return loss is expected from the circuit.



Results and Discussions:

It is observed from the layout simulation that the Lowpass filter has a 3 dB cutoff frequency of 2 GHz after parametric EM analysis.

Simulation of a Lumped and Distributed Bandpass filter using ADS

ypical Design:

Upper Cutoff Frequency (f_{c1})	: 1.9 GHz
Lower Cutoff Frequency (f_{c2})	: 2.1 GHz
Ripple in passband	: 0.5 dB
Order of the filter	: 3
Type of Approximation	: Chebyshev

Prototype Values of the Filter:

The prototype values of the filter for Chebyshev approximation is calculated using the formulae given above in previous text.

The prototype values for the given specifications of filter are

g1 = 1.5963, g2 = 1.0967 & g3 = 1.5963

Lumped Model of the Filter:

The Lumped values of the Bandpass filter after frequency and impedance scaling are given by:

$L'_1 = L_1 Z_0 / \omega_0 \Delta$

$C'_1 = \Delta / L_1 Z_0 \omega_0$

$L'_2 = \Delta Z_0 / \omega_0 C_2$

$C'_2 = C_2 / Z_0 \Delta \omega_0$

$L'_3 = L_3 Z_0 / \omega_0 \Delta$

$C'_3 = \Delta / L_3 Z_0 \omega_0$ where Z_0 is 50Ω

$\Delta = (\omega_2 - \omega_1) / \omega_0$

The resulting lumped values are given by

L'_1 = 63 nH

C'_1 = 0.1004 pF

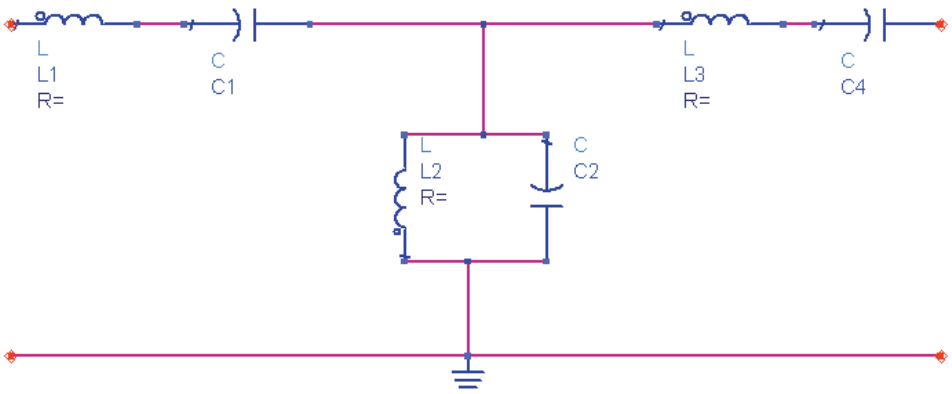
L'_2 = 0.365 nH

C'_2 = 17.34 pF

L'_3 = 63 nH

C'_3 = 0.1004 pF

The Geometry of the lumped element bandpass filter is shown in next figure.



Distributed Model of the Filter:

Calculate the value of j from the prototype values as follows

$$\left[z_0 j_1 = \sqrt{\frac{\pi\Delta}{2g_1}} \right]$$

$$z_0 j_n = \frac{\pi\Delta}{2\sqrt{g_n - 1 g_n}} \qquad \text{For n =2, 3....N,}$$

$$z_0 j_{N+1} = \sqrt{\frac{\pi\Delta}{2g_N g_{N+1}}}$$

Where $\Delta = (\omega_2 - \omega_1) / \omega_0$

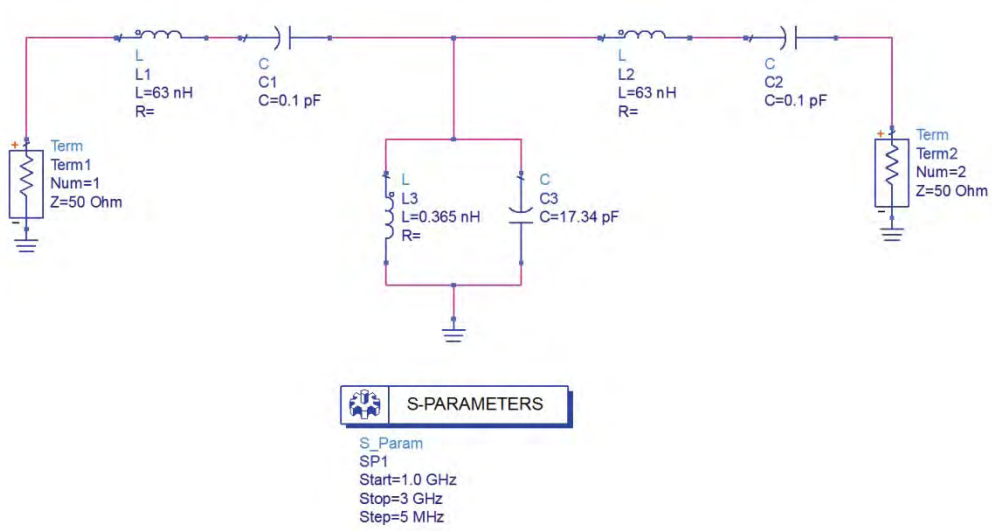
Z_0 = Characteristic Impedance = 50Ω

The values of odd and even mode impedances can be calculated as follows

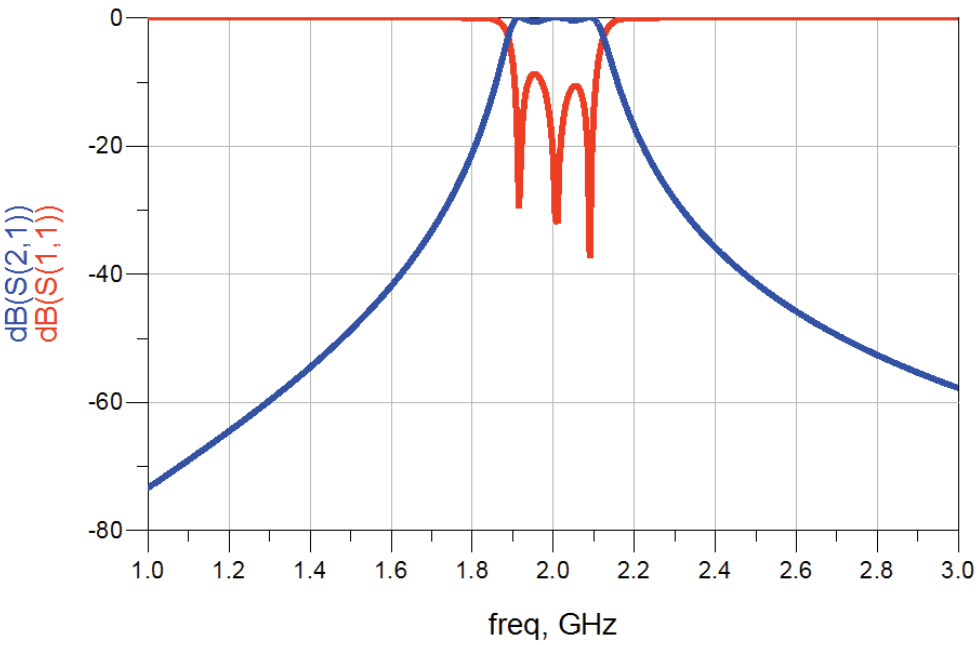
$$z_{0e} = z_0[1 + jz_0 + (jz_0)^2]$$
$$z_{0o} = z_0[1 - jz_0 + (jz_0)^2]$$

Schematic Simulation steps for Lumped Bandpass Filter:

Open the Schematic window of ADS and construct the lumped bandpass filter as shown below. Setup the S-Parameter simulation from 1 GHz to 3 GHz with steps of 5 MHz (401 points).



Click on Simulate icon to observe the graph as shown below:



Results and Discussions:

It is observed from the schematic simulation that the lumped model of the bandpass filter has an upper cutoff at 1.9 GHz, lower cutoff at 2.1 GHz and a roll off as per the specifications.

Layout Simulation steps for Distributed Bandpass Filter

Calculate the odd mode and even mode impedance values (Zoo & Zoe) of the bandpass filter using the design procedure given above. Synthesize the physical parameters (length & width) for the coupled lines for a substrate thickness of 1.6 mm and dielectric constant of 4.6.

The physical parameters of the coupled lines for the given values of Zoo and Zoe are given as follows

Substrate Thickness : 1.6 mm

Dielectric Constant : 4.6

Frequency : 2 GHz

Electrical Length : 90 degrees

Section 1: Zoo = 36.23, Zoe = 66.65

Width = 2.545

Length = 20.52

Spacing = 0.409

Section 2: Zoo = 56.68, Zoe = 44.73

Width = 2.853

Length = 20.197

Spacing = 1.730

Section 3: Zoo = 56.68, Zoe = 44.73

Width = 2.853

Length = 20.197

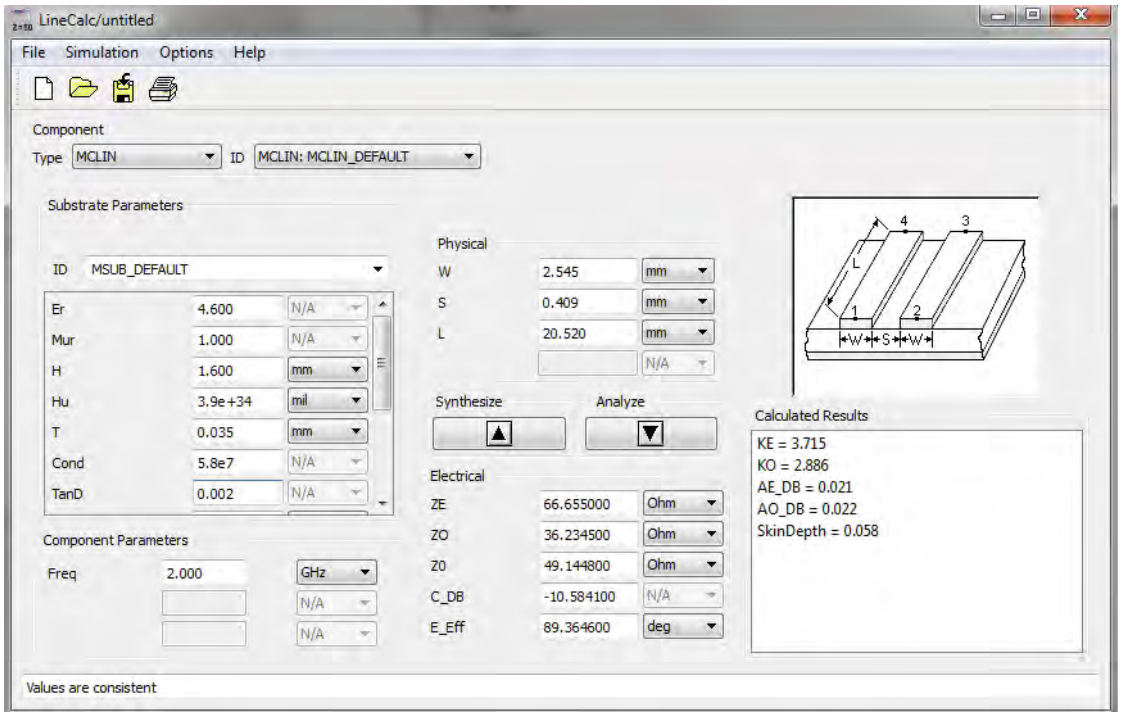
Spacing = 1.730

Section 4: Zoo = 36.23, Zoe = 66.65

Width = 2.545

Length = 20.52

Spacing = 0.409



Calculate the length and width of the 50 Ω line using the line calc window of ADS as done earlier.

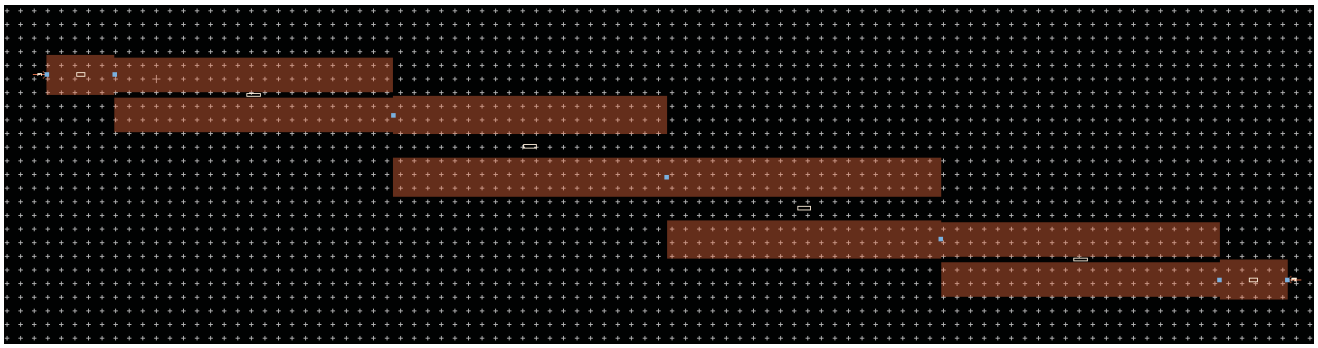
50 Ω Line:

Width: 2.9 mm

Length: 5 mm

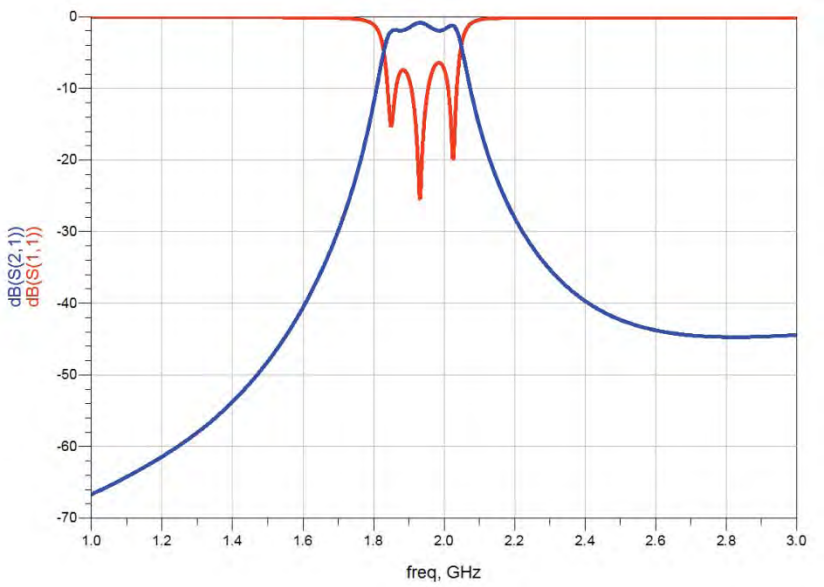
Create a model of the bandpass filter in the layout window of ADS. The Model can be created by using the available library components or by drawing rectangles.

To create the model using library components select the MCFIL from TLines–Microstrip library. Select the appropriate kind of Microstrip line from the library and place it on the layout window as shown in figure below:



Setup EM simulation using the procedure defined earlier for 1.6mm FR4 dielectric and perform Momentum simulation from 1 GHz to 3 GHz and don't forget to switch on the Edge Mesh from Options->Mesh tab of the EM setup window.

Once simulation finishes, plot S11 and S21 response of the BPF as shown below:



Results and Discussions:

While the results are good in lumped element filters but the circuit needs to simulated and probably needs to be re-optimized with the Vendor components libraries and we need to perform Yield analysis simulation to take note of the performance variation which may be caused due to tolerances of the lumped components.

For distributed filter design we can further optimize the design using circuit simulator or Momentum EM simulator to obtain better bandpass filter characteristics if desired as EM simulation is showing little degraded performance for BPF in EM simulation.

Chapter 8: Discrete and Microstrip Coupler Design

ADS Licenses Used:

- **Linear Simulation**
- **Momentum Simulation**
- **Layout**

Chapter 8: Discrete and Microstrip Coupler Design

Theory:

A coupler is basically a device that couples the power from the input port to two or more output ports equally with less loss and with or without the phase difference. The branch line coupler is a 3 dB coupler with 90^0-phase difference between the two output ports. An ideal branch line coupler as shown in figure 1 is a four-port network and is perfectly matched at all the four ports.

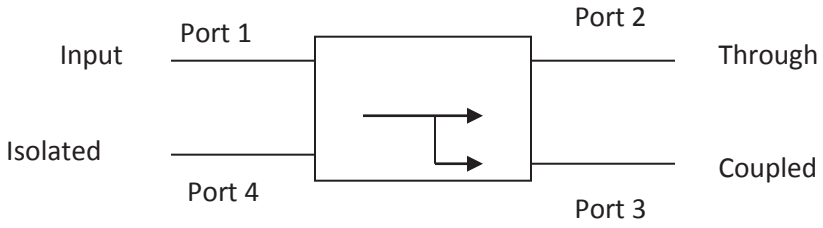


Fig. 1 Block diagram of a four port coupler

The power entering in port 1 is evenly divided between ports 2 and 3, with a phase shift of 90 degree between the ports. The 4^{th} port is the isolated port and no power flows through it. The branch line coupler has a high degree of symmetry and allows any of the four ports to be used as the input port. The output ports are in the opposite sides of the input port and the isolated port is in the same side of the input port. This symmetry is reflected in the S matrix as each row can be the transposition of the first row. The [S] matrix of the ideal branch line coupler is given as follows

$$[S]=\frac{-1}{\sqrt{2}}\begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix}$$

The major advantage of this coupler is easier realization and disadvantages are lesser bandwidth due to the use of quarter wave length transmission line for realization and discontinuities occurring at the junction. To circumvent the above disadvantages multi sections of branch line coupler in cascade can increase the bandwidth by a decade and 10^o – 20^o increase in length of the shunt arm can compensate the power loss due to discontinuity effects.

Objective:

Design a lumped element and distributed branch line coupler at 2 GHz and simulate the performance using ADS.

Design of Lumped Element Branch Line Coupler

Calculate the values of the capacitances (C_0 & C_1) and inductances (L) required for the Lumped model of the coupler shown in Fig.2 using the given formulae.

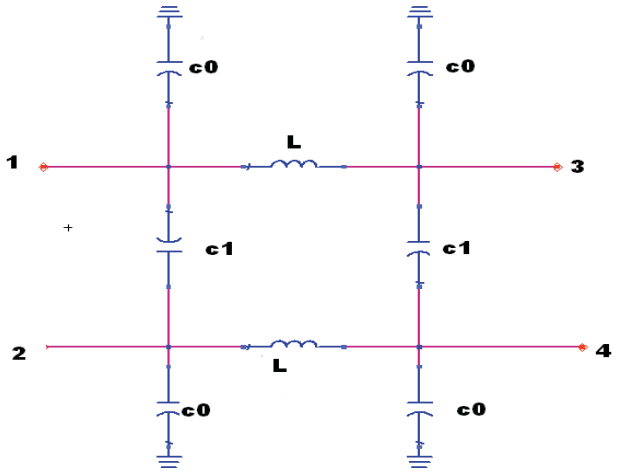


Fig. 2 Lumped Model of the Directional Coupler

$$\omega = 2\pi f_c$$

$$C_1 = \frac{1}{\omega Z_0 \sqrt{K}}$$ Where K = 1 for the 3dB coupler

$$C_0 = \frac{1}{(\omega^2 L)} - C_1$$

$$L = \frac{Z_0}{\omega\sqrt{1 + Zo\omega C_1}}$$

Where f_c is the design frequency of the coupler

Z_0 is the characteristic impedance of the transmission line

Typical Design Specs:

Design Frequency f_c = 2 GHz

Angular Frequency ω in radians = $2\pi f_c$ = 1.25×10^{10}

Characteristic Impedance Z_0 = 50 Ω

Substituting the values in the above design equation the values for the lumped model are obtained as follows

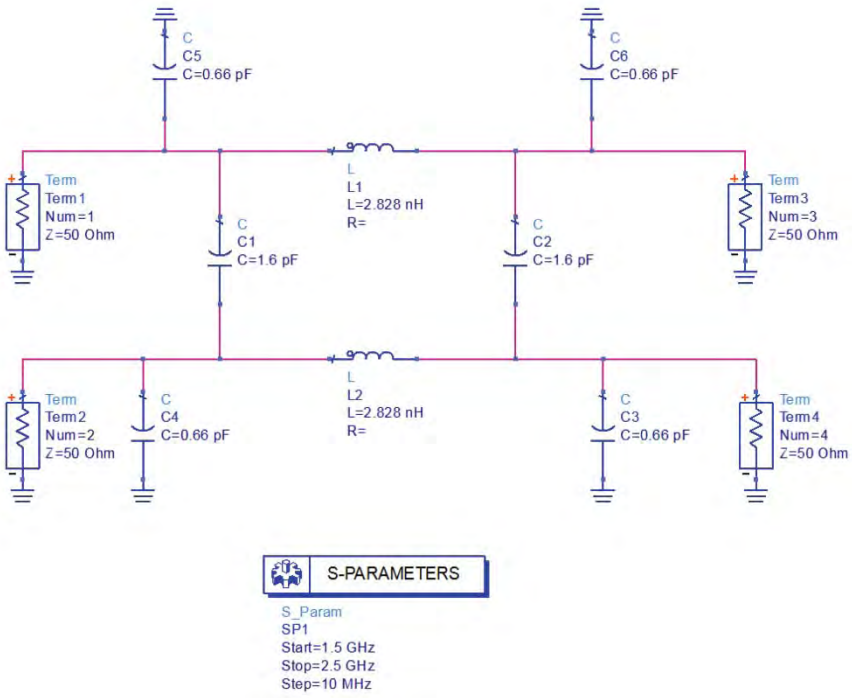
C_1 = 1.6 pF

L = 2.8 nH

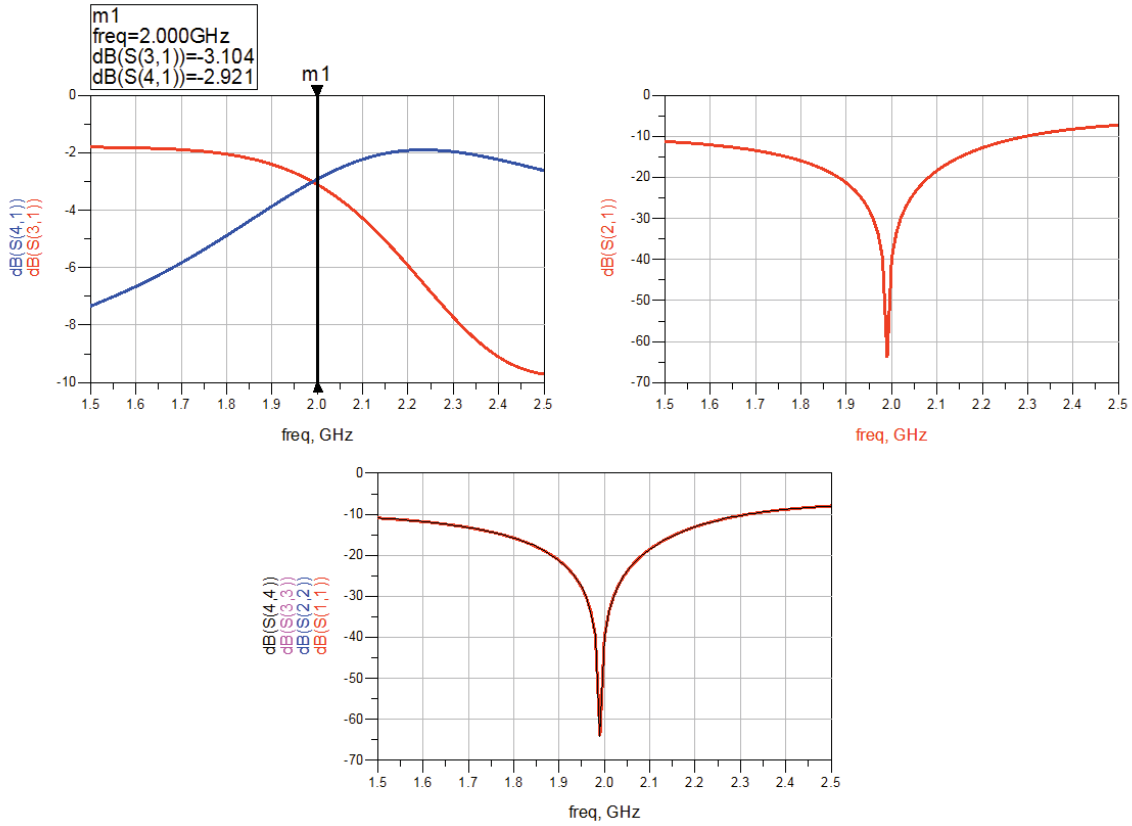
C_0 = 0.66 pF

Schematic Simulation Steps

1. Open the Schematic window of ADS
2. From the lumped components library select the appropriate components necessary for the lumped model. Click on the necessary components and place them on the schematic window of ADS as shown in next figure.
3. Setup a S-Parameter simulation for 1.5 GHz to 2.5 GHz with 101 points and run simulation.



4. Once the simulation is finished plot the required graphs to observe the Coupler response as shown in figure below



Design of Distributed Branch Line Coupler:

1. Select an appropriate substrate of thickness (h) and dielectric constant (ε_r) for the design of the coupler. For present example, we will select following dielectric parameters:
    a. Er = 4.6
    b. Height = 1.6 mm
    c. Loss Tangent = 0.0023
    d. Metal Thickness = 0.035 mm
    e. Metal Conductivity = 5.8E7 S/m
2. Calculate the wavelength λ_g from the given frequency specifications as follows

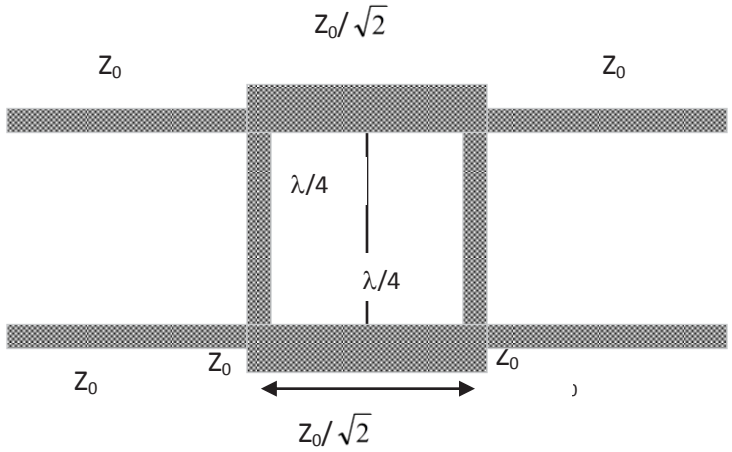
$$\lambda_g = \frac{c}{\sqrt{\varepsilon_r}\, f}$$

Where, c is the velocity of light in air

f is the frequency of operation of the coupler

ε_r is the dielectric constant of the substrate.

3. Synthesize the physical parameters (length & width) for the λ/4 lines with impedances of Z_0 and $Z_0/\sqrt{2}$ (Z_0 is the characteristic impedance of microstrip line is which taken as 50Ω). The geometry of the Branch line coupler is shown in figure below.



Layout Simulation using ADS

1. Calculate the physical parameters of the branch line coupler from the electrical parameters like Z_0 and electrical length using the above given design procedure. The physical parameters can be synthesized using Linecalc of the ADS as described in earlier labs. The physical parameters of the microstrip line for the 50Ω (Z_0) and 35Ω ($Z0/\sqrt{2}$) are as follows

   50Ω Line:

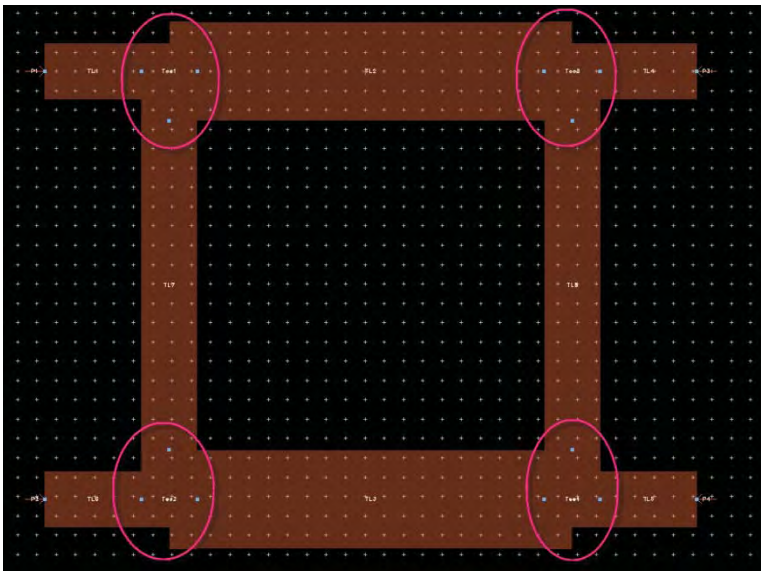
   i. Width - 2.9 mm
   ii. Length – 20 mm

35Ω Line:

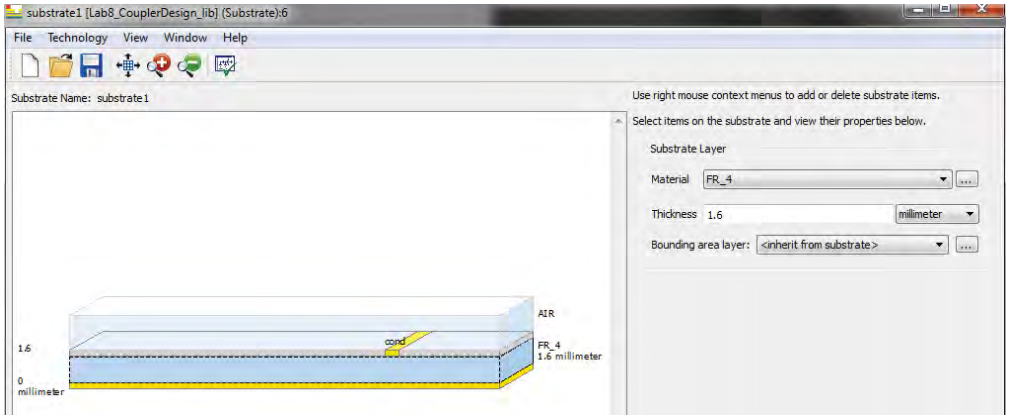
   iii. Width - 5.14 mm
   iv. Length – 19.5 mm

2. Create a model of the branch line coupler in the layout window of ADS. The Model can be created by using the available Microstrip library components or by drawing rectangles.

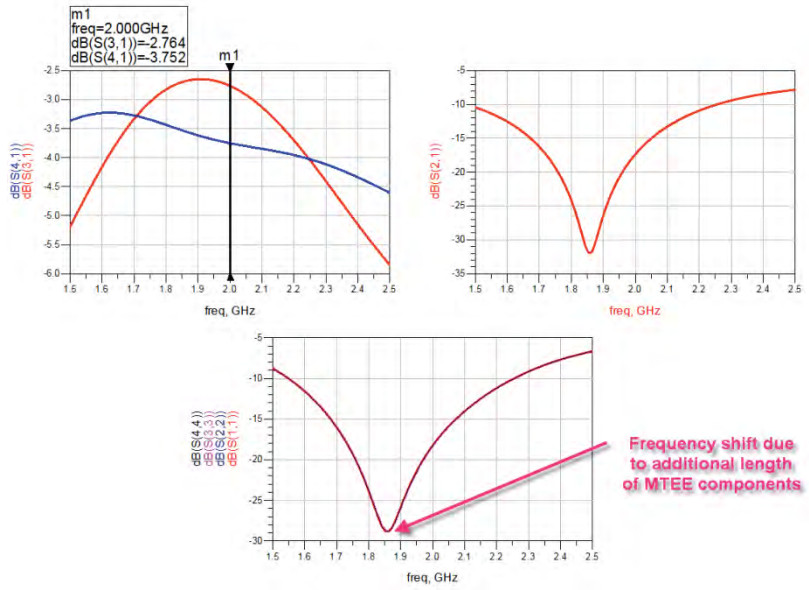
3. To create the model using library components select the TLines – Microstrip library. Select the appropriate kind of Microstrip line from the library and place it on the layout window as shown in figure below. We need to add Microstrip TEE at the 4 junctions for proper connections of the lines as highlighted in the figure below.



4. Using the EM setup window, define the dielectric and conductor properties using the procedure described in Momentum simulation lab. Once defined properly, it should look as shown below

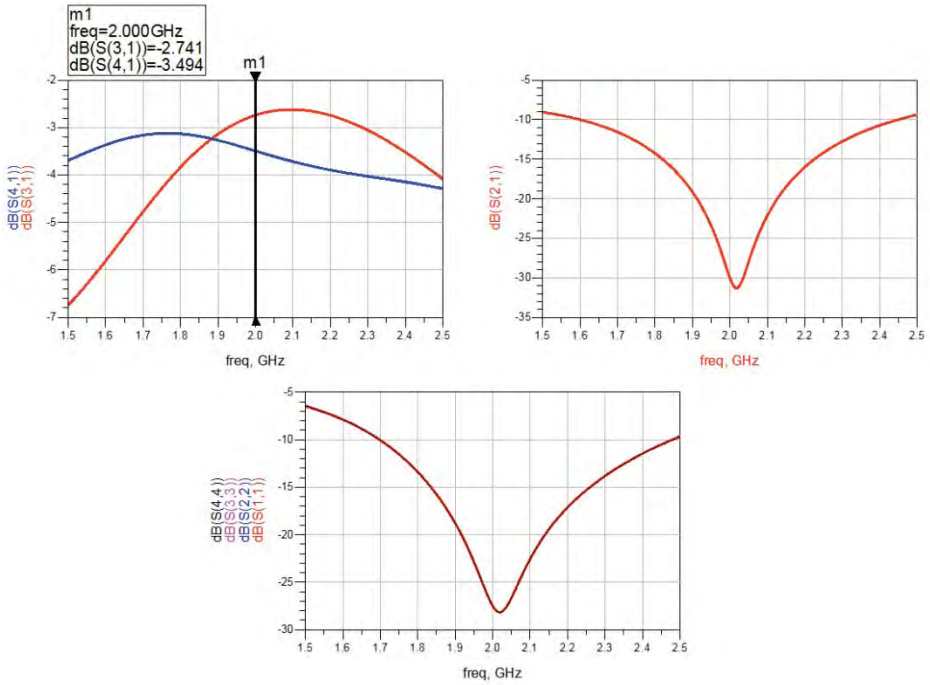


5. Setup the simulation frequency from 1.5GHz – 2.5 GHz, switch on the Edge Mesh from Options->Mesh tab of the EM setup window and click on Simulate button.
6. Once simulation is finished, plot and observe the required response and note that frequency is little shifted to the lower side as shown below



7. In order to compensate for TEE effect, we need to reduce the calculated lengths of coupler lines by ~ w/2 of the intersecting line, e.g. 19.5 mm 35Ohm line should have approx length of 18.2 mm and 19.5 mm, 50Ohm vertical line should have length of 17.1 mm

8. Modify the length of lines and reconnect the lines as shown below and simulate the layout again with the same simulation setting to observe the response coming close to desired 2 GHz frequency.



Conclusion

While the results are good in lumped element coupler but the circuit needs to simulated and probably needs to be re-optimized with the Vendor components libraries and we need to perform Yield analysis simulation to take note of the performance variation which may be caused due to tolerances of the lumped components.

For distributed coupler design we can optimize the design using circuit simulator or Momentum EM simulator to obtain better coupling if desired as circuit is showing over-coupling in one of the branches.

Chapter 9: Microstrip and CPW Power Divider Design

ADS Licenses Used:

- **Linear Simulation**
- **Momentum (EM) Simulation**
- **Layout**

Chapter 9: Microstrip and CPW Power Divider Design

Theory:

A power divider is a three-port microwave device that is used for power division or power combining. In an ideal power divider the power given in port 1 is equally split between the two output ports for power division and vice versa for power combining as shown in figure 1. Power divider finds applications in coherent power splitting of local oscillator power, antenna feedback network of phased array radars, external leveling and radio measurements, power combining of multiple input signals and power combining of high power amplifiers**.**

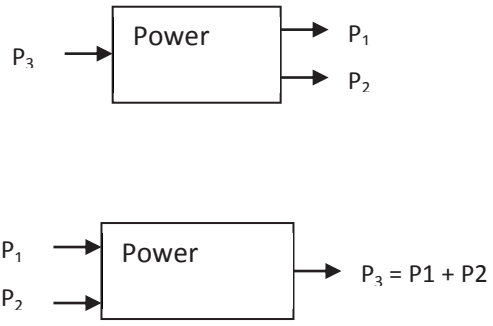


Fig1. Model of an Ideal power divider and power combiner

T –Junction Power Divider:

The different types of power divider are T junction power divider, Resistive divider and Wilkinson power and hybrid couplers. The T –junction power divider is a simple 3-port network and can be implemented in any kind of transmission medium like microstrip, stripline, coplanar wave guide etc. Since any 3-port network cannot be lossless, reciprocal and matched at all the ports, the T junction power divider being lossless and reciprocal and cannot be perfectly matched at all the ports. The T junction power divider can be modeled as a junction of three transmission lines as shown in figure below.

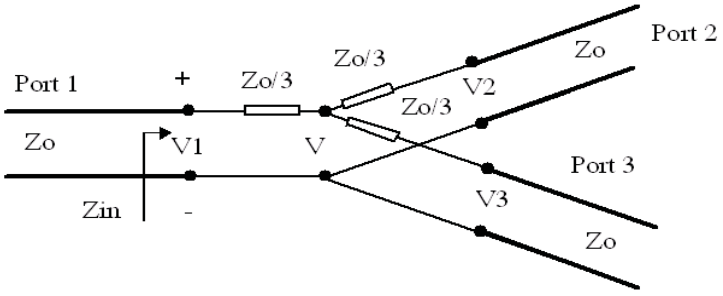


Fig2. Model of the T- junction power divider

Objective:

To design various types of Power Divider at 3 GHz and simulate the performance using ADS.

Design of Distributed T junction Power Divider:

1. Select an appropriate substrate of thickness (h) and dielectric constant (ε_r) for the design of the power divider.
2. Calculate the wavelength λ_g from the given frequency specifications as follows

$$\lambda_g = \frac{c}{\sqrt{\varepsilon_r}\ f}$$

where c is the velocity of light in air

f is the frequency of operation of the coupler

ε_r is the dielectric constant of the substrate

3. Synthesize the physical parameters (length & width) for the $\lambda/4$ lines with impedances of Z_0 and $\sqrt{2}\ Z_0$ (Z_0 is the characteristic impedance of microstrip line which is = 50Ω)

Layout Simulation using ADS:

1. Calculate the physical parameters of the T junction power divider from the electrical parameters like Z_0 and electrical length using the above given design procedure. The physical parameters can be synthesized using Linecalc of the ADS as shown in earlier chapters. The Physical parameters of the microstrip line for the 50Ω (Z_0) and 70.7Ω ($\sqrt{2}\ Z_0$) are as follows

2. Dielectric properties: Er = 4.6, Height = 1.6 mm, Loss Tangent = 0.0023, Metal Height = 0.035 mm, Metal Conductivity = 5.8E7

   50Ω Line:

   Width – 2.9 mm

   Length – 13.3 mm

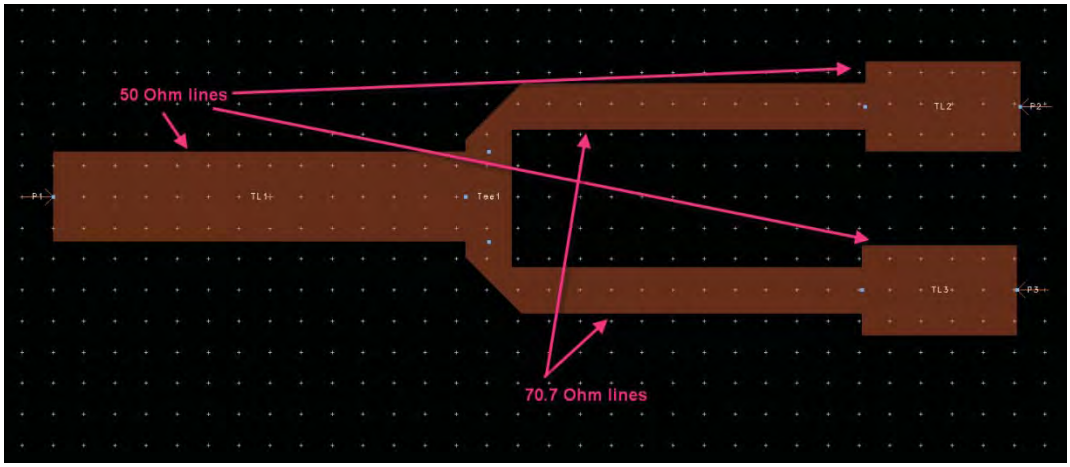
   70.7Ω Line:

   Width – 1.5 mm

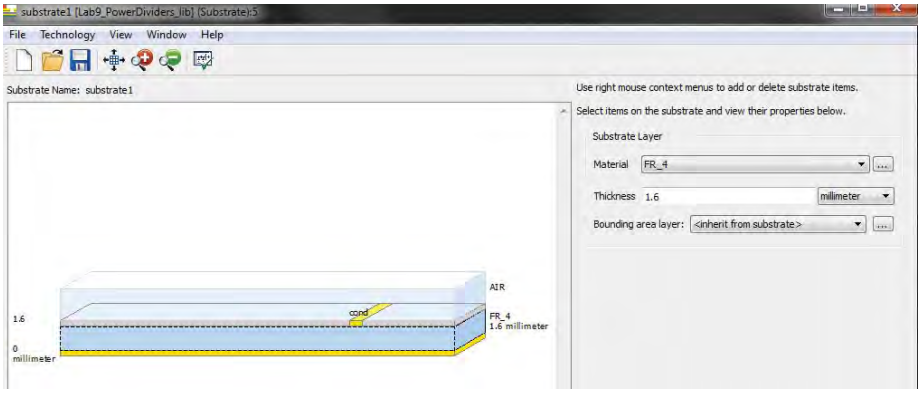
   Length – 13.6 mm

3. Create a model of the T-junction power divider in the layout window of ADS. The Model can be created by using the available Microstrip library components or by drawing rectangles.

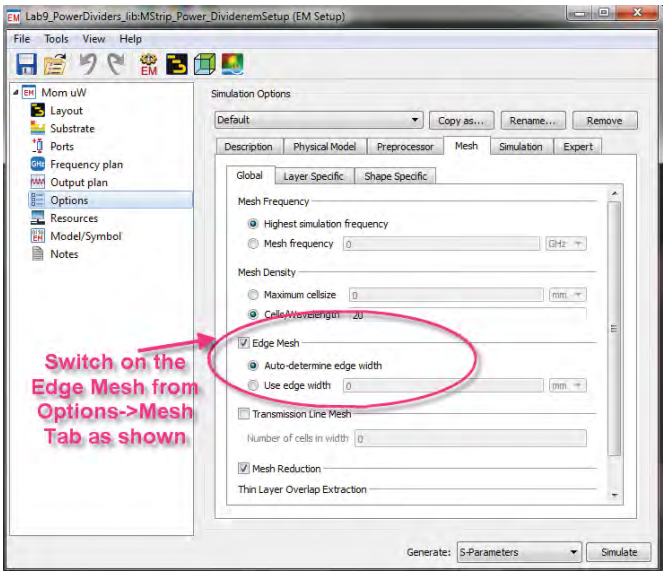
4. To create the model using library components select the TLines – Microstrip library. Select the appropriate Microstrip line from the library and place it on the layout window as shown in next figure.



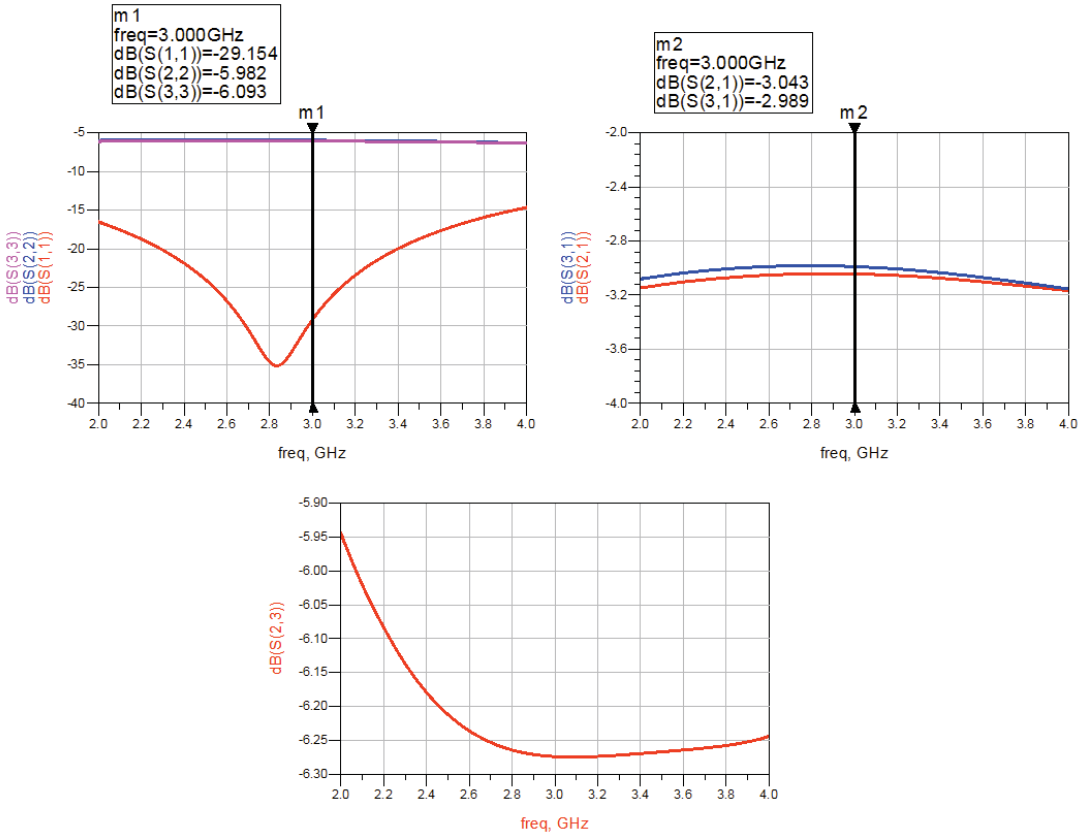
- Connect the Pins and input and output terminals and set the EM simulation as described in EM simulation chapter earlier. Once done it should be as figure below



- Define the simulation frequency from 2 GHz – 3 GHz and switch on the Edge Mesh from Options->Mesh tab in the EM set up window.



- Click on Simulate icon and plot the required to observe the T-junction power divider response as shown below



Results and Discussions:

It is observed from the layout simulation that the T junction power divider has an insertion loss (S_{12} and S_{13}) of 3.0dB and return loss (S_{11}) of about 29 dB but as expected isolation between 2 output branches is only 6 dB representing real characteristics of T-junction power divider.

Wilkinson Power Divider:

Theory:

The Wilkinson power divider is robust power divider with all the output ports matched and only the reflected power is dissipated. The Wilkinson power divider provides better isolation between the output ports when compared to the T junction power divider The Wilkinson power divider can also be used to provide arbitrary power division. The geometry of Wilkinson power divider and its transmission line equivalent is shown in figure 3 below.

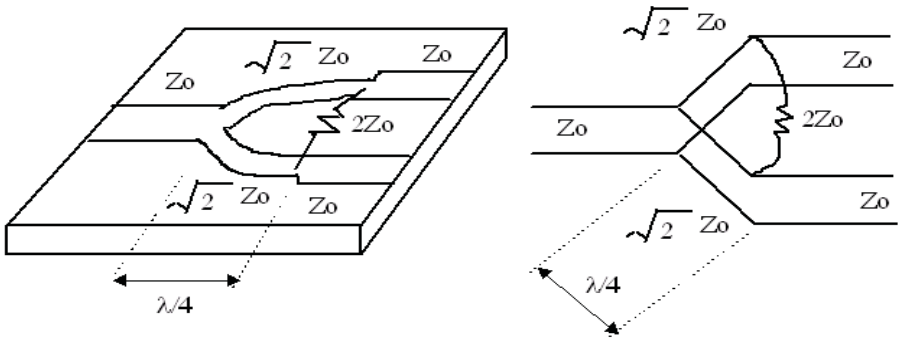


Fig3. Geometry and Transmission line equivalent of Wilkinson power divider

Design of Lumped model Wilkinson Power divider

Calculate the values of the capacitances (C_1 & C_2), inductances (L_1, L_2 & L_3) and resistance (R1) required for the Lumped model of the coupler shown in figure 4 using the given formulae.

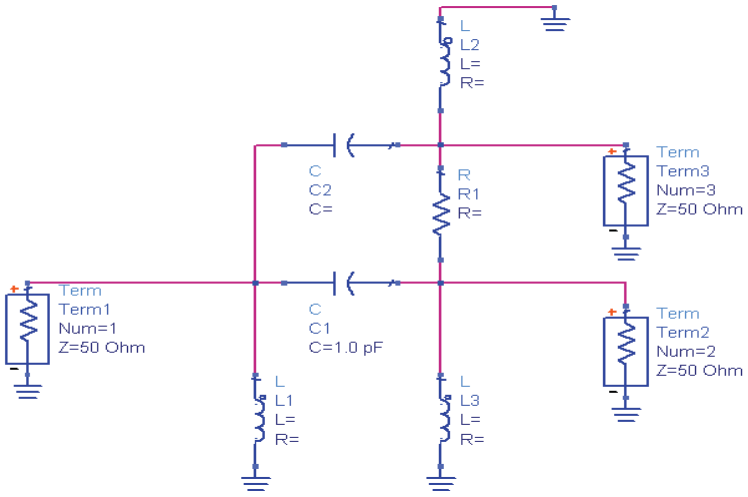


Fig4. Lumped Model of the Wilkinson power divider

$$C_1 = C_2 = \frac{1}{\sqrt{\left(2R_a \cdot \sqrt{R_b R_c} \cdot \omega^2\right)}}$$

$$L_3 = L_2 = \sqrt{\frac{2R_a\sqrt{R_b R_c}}{\omega^2}}$$

$$L_1 = \sqrt{\frac{R_a\sqrt{R_b R_c}}{2\omega^2}}$$

$$R = 2\sqrt{R_a R_b}$$

Where for any arbitrary impedance $Z_0 = R_a = R_b = R_c = 50$ohms

ω is the angular frequency

Typical Design

Design frequency = 3 GHz

Angular frequency in radians = 1.88×10^{10}

$C_1 = C_2 = 0.75$ pF,

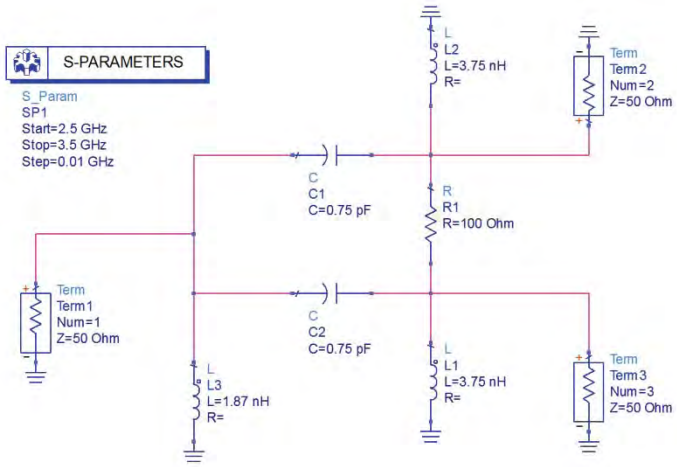
$L_2 = L_3 = 3.75$ nH

$L_1 = 1.87$ nH

$R = 100\ \Omega$

Schematic Simulation Steps

1. Open the Schematic window of ADS
2. From the lumped components library select the appropriate components necessary for the lumped model. Click on the necessary components and place them on the schematic window of ADS as shown in figure below



3. Setup the S-Parameter simulation from 2.5 GHz – 3.5 GHz with step size of 0.01 GHz. Perform simulation and observe required parameter response as shown below

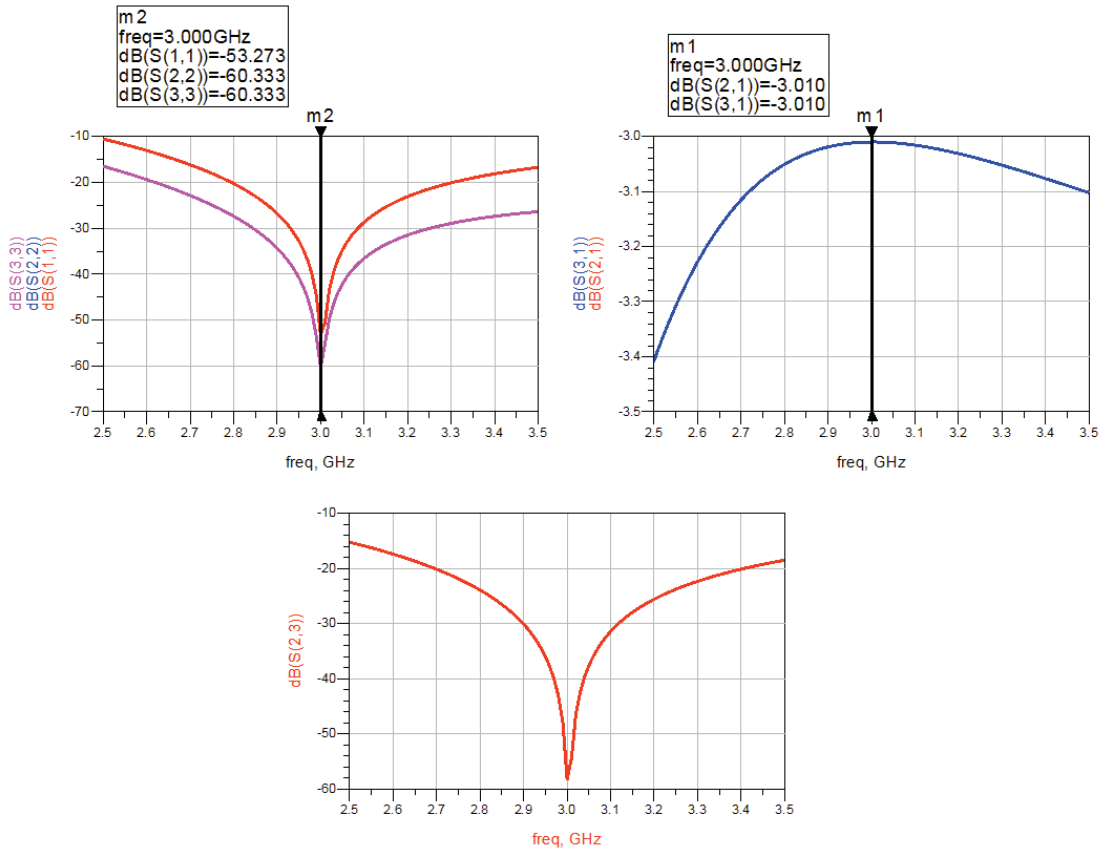


Fig5. Scattering Parameters of the Lumped model Wilkinson Power Divider

Results and Discussions:

It is observed from the schematic simulation that the lumped model of the Wilkinson power divider has an insertion loss (S_{12} and S_{13}) of 3 dB and return loss (S_{11}) of <30 dB.

Design of Distributed Wilkinson power divider:

Layout Simulation using ADS:

1. Calculate the physical parameters of the Wilkinson power divider from the electrical parameters like Z_0 and electrical length similar to T-junction power divider. The physical parameters can be synthesized using Linecalc of the ADS as shown in earlier chapters. The physical parameters of the microstrip line for the 50Ω (Z_0) and 70.7Ω ($\sqrt{2}\ Z_0$) are as follows on dielectric as selected in T-junction power divider design

   50Ω Line:

   Width – 2.9 mm

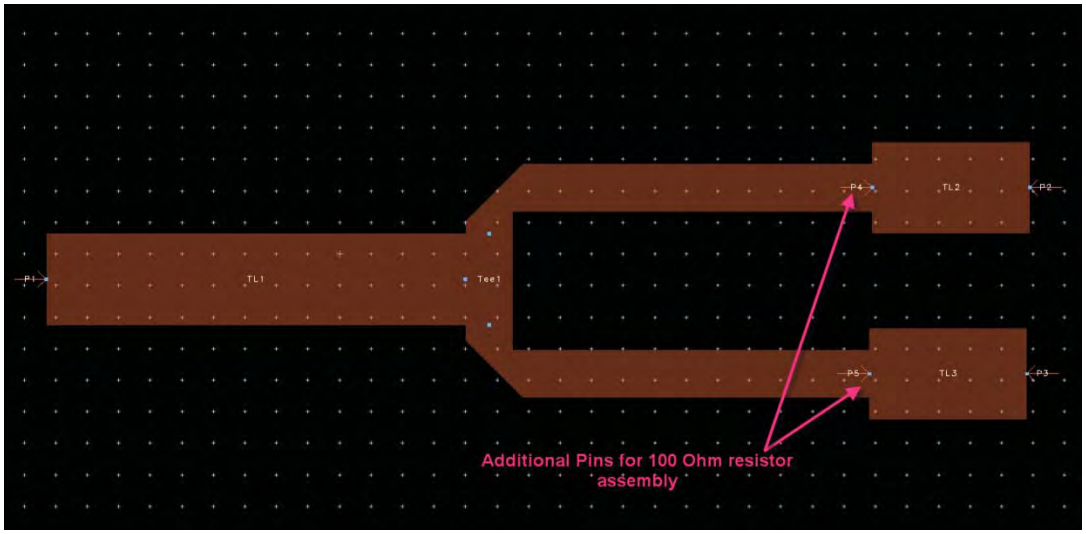
   Length – 13.3 mm

   70.7Ω Line:

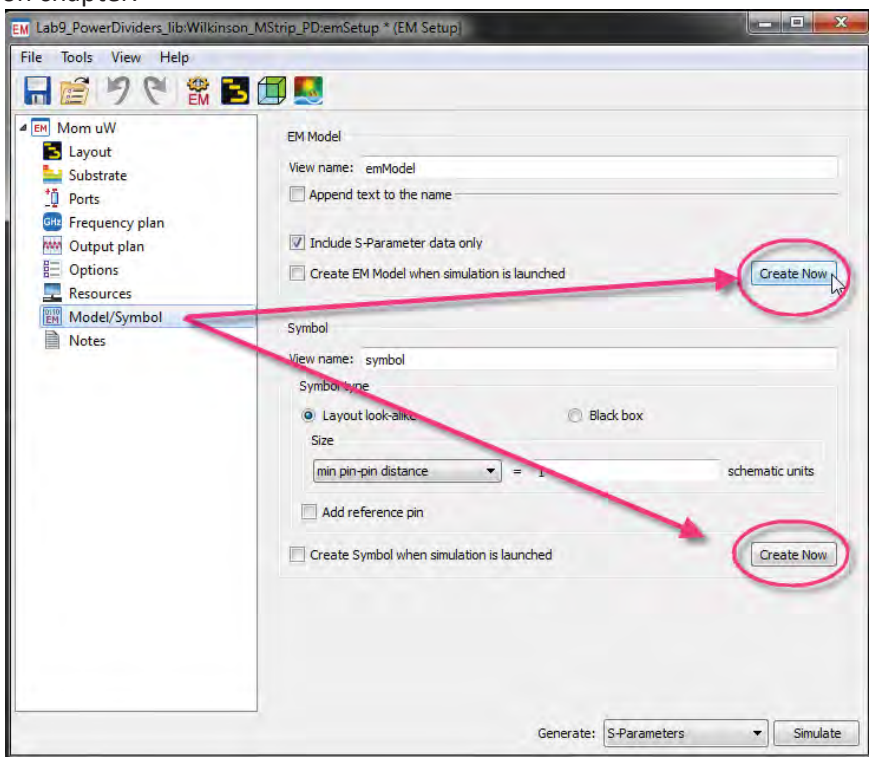
   Width – 1.5 mm

   Length – 13.6 mm

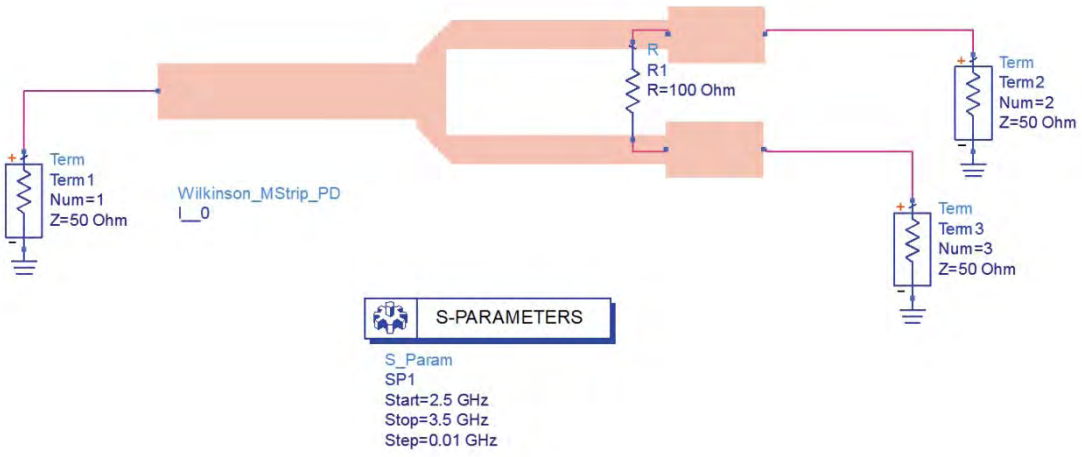
2. Layout of the Wilkinson power divider will be same done earlier except for the fact that we shall isolation resistor of 2*Z0 which in our case will be 100Ohm as characteristics impedance is 50 Ohm.
3. Use TLines-Microstrip components or rectangle/polygon icon to create power divider structure. Please note that in Wilkinson power divider we shall 2 extra Pins at the place where we shall later connect 100 Ohm resistor.



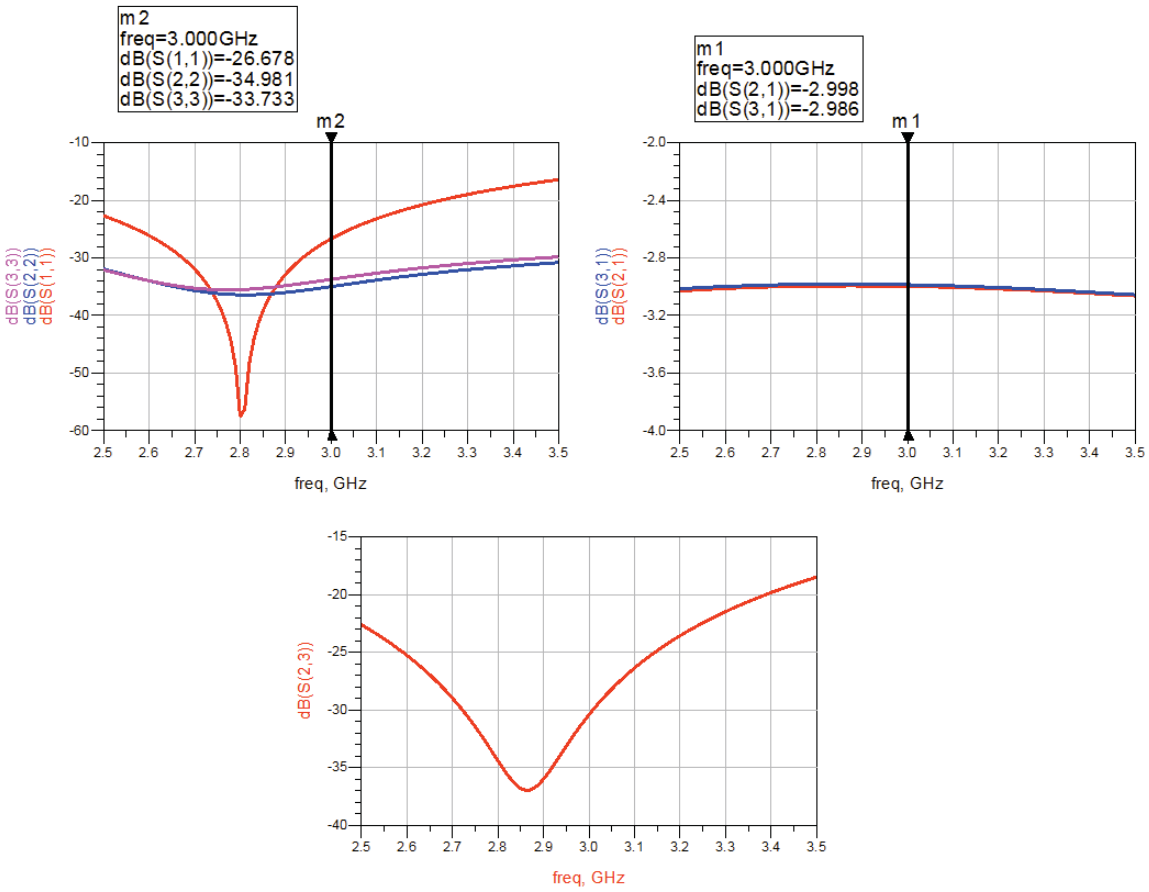
4. Define new or reuse the substrate defined earlier for T-junction power divider exercise. Define the frequency sweep from 2.5 GHz – 3.5 GHz and from Model/Symbol option in EM setup window click on Create Now button under EM Model and Symbol fields to generate EM Model data container and layout look alike symbol so that we can use this layout component to perform resistor assembly and EM cosimulation. Detailed steps for the same are provided in EM simulation chapter.



5. Open a new schematic cell, drag & drop this layout on the same and connect Terminations and Resistor at required place as shown below. Set up a S-Parameter simulation from 2.5 GHz – 3.5 GHz with Step=0.01 GHz



6. Click on Simulate icon to wait for EM simulation and Schematic simulation to get completed and plot the required graphs in data display as shown below



Results and Discussions:

It is observed from the layout simulation that the Wilkinson power divider has an insertion loss (S_{12} and S_{13}) of 3.0dB and return losses ($S_{11,}$ $S_{22,}$ S_{33}) < -25 dB.

Design of CPW T junction power divider

Objective:

To design a CPW T junction power divider at 2.4 GHz and simulate the performance using ADS.

Design Procedure

1. Select an appropriate substrate of thickness (h) and dielectric constant (ε_r) for the design of the power divider.
2. Calculate the wavelength λ_g from the given frequency specifications as follows

$$\lambda_g = \frac{c}{\sqrt{\varepsilon_r}\, f}$$

where c is the velocity of light in air

f is the frequency of operation of the coupler

ε_r is the dielectric constant of the substrate

3. Synthesize the physical parameters (length & width) for the $\lambda/4$ CPW line with impedances of Z_0 and $\sqrt{2}\ Z_0$ (Z_0 is the characteristic impedance of CPW line = 50Ω)

Layout Simulation using ADS:

1. Calculate the physical parameters of the T-junction power divider from the electrical parameters like Z_0 and electrical length using the above given design procedure. The physical parameters can be synthesized using Linecalc of the ADS as shown in figure 38. The Physical parameters of the CPW line for 50Ω (Z_0) and 70.7Ω ($\sqrt{2}\ Z_0$) are as follows

50Ω Line:
- Width: 3 mm
- Length: 20 mm
- Gap: 0.37mm

70.7Ω Line:
- Width: 1.5 mm
- Length: 19.6 mm
- Gap: 0.69 mm

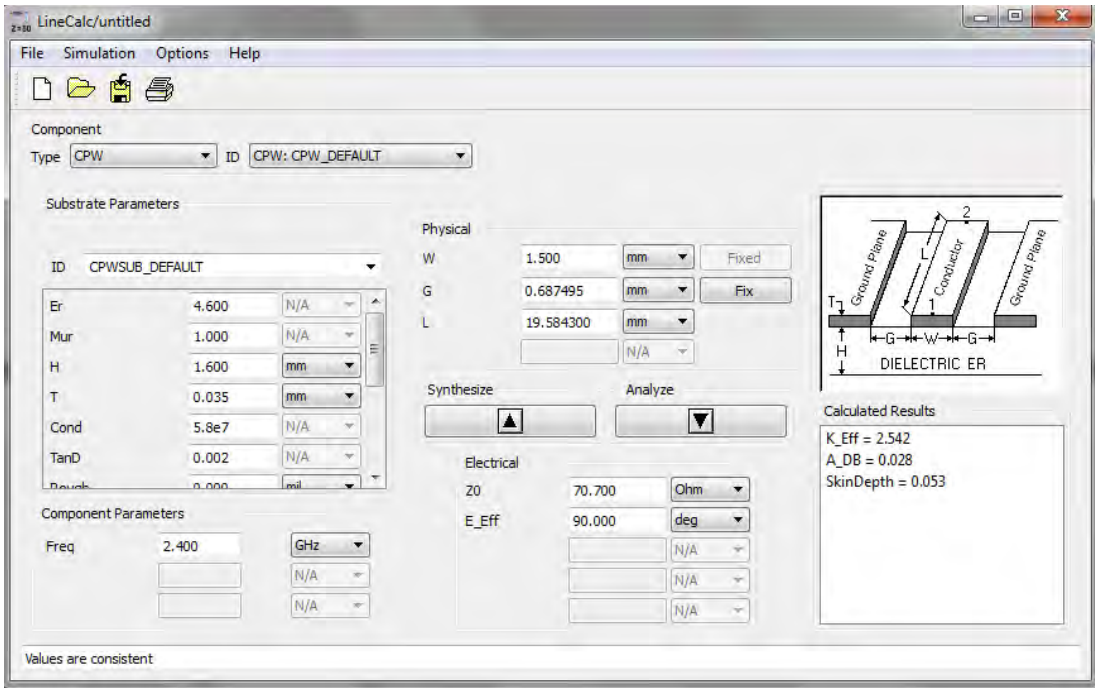


Fig6. Linecalc window of ADS showing the synthesis of physical parameters of power divider

2. Create a model of the T-junction power divider in the layout window of ADS. The Model can be created by using the available TLines-Waveguide library components or by drawing rectangles.

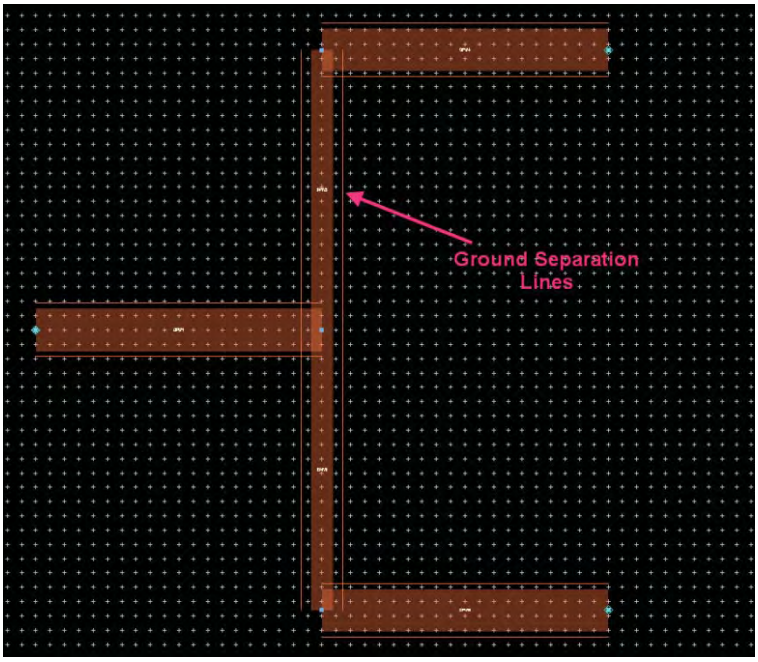
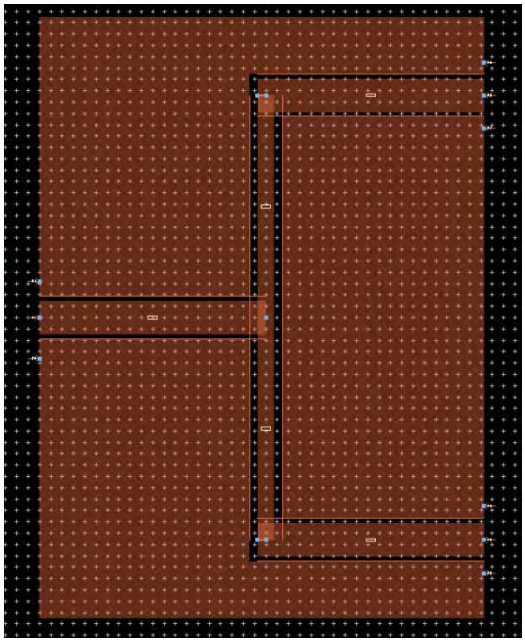


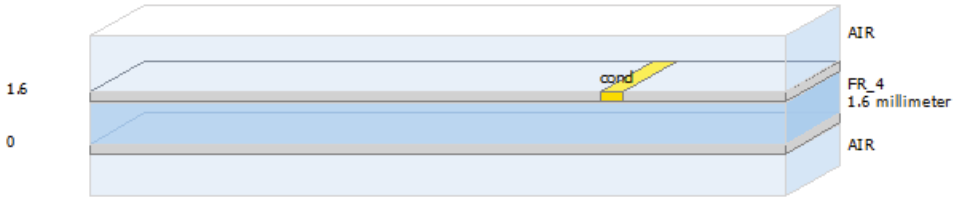
Fig7. Layout window of ADS showing the distributed model of CPW T junction power divider

The ground separation lines will help us as a guiding lines for ground creation and we can simply use the rectangle icon to create ground for these CPW lines as shown below

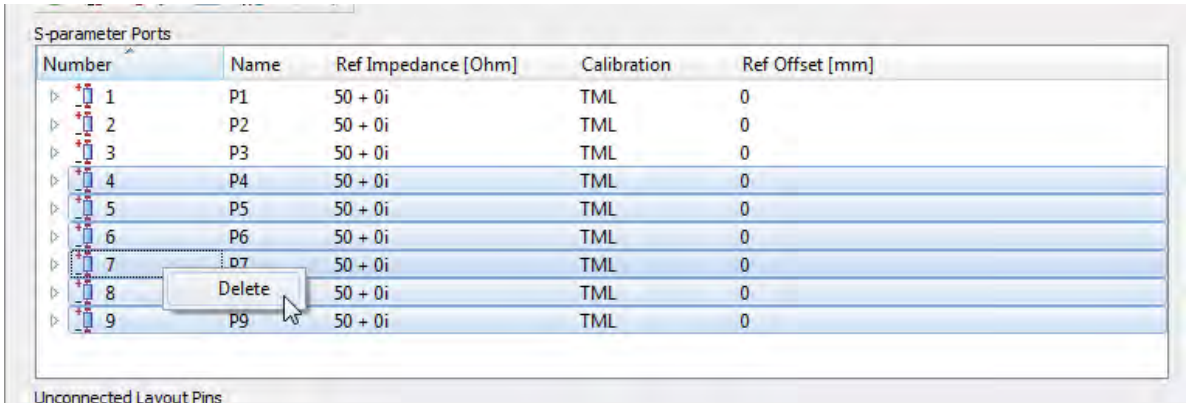


3. Assign Pins in layout for the CPW transmission line by clicking the Pin icon and placing them in the circuit i.e 1 Port on the main line and placing 2 port attached to the ground fill on either side of the main signal pin. For present case we shall have total of 9 Pins i.e. 3 Signal Pins and 6 ground pins. For easy remembrance, place 3 signal pins so that they are named as P1, P2 & P3 and then start placing P4 & P5 around P1, P6 & P7 around P2 and P8 & P9 around P3. **It is strongly advised to place ground port slightly inside the ground pattern.**

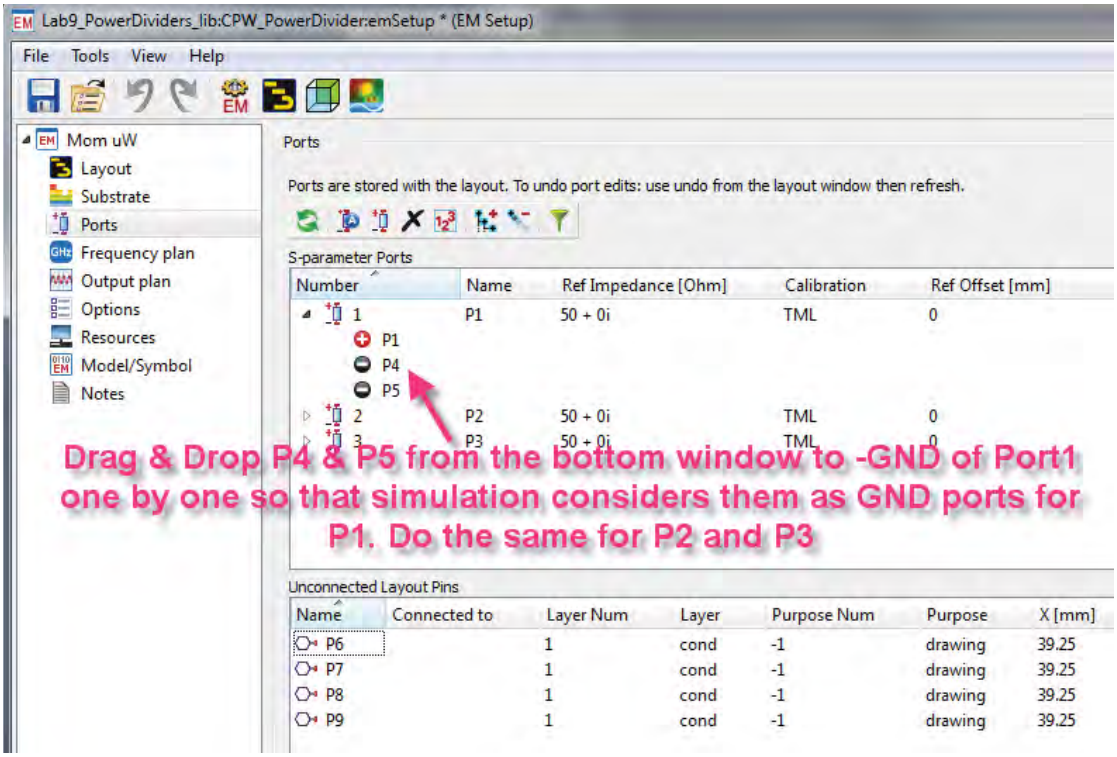
4. Defining CPW substrate without ground at the bottom will require substrate to be defined little differently than what we have done till now. Open the EM setup window, define the required dielectric as described in earlier labs and do following additional actions:
    a. Right click on the FR4 and select Insert Substrate Layer Below. Right click on the Cover and select Delete Cover.
    b. Change the bottom side dielectric as AIR (which is by default provided in substrate definition window). Once done it should look as shown below



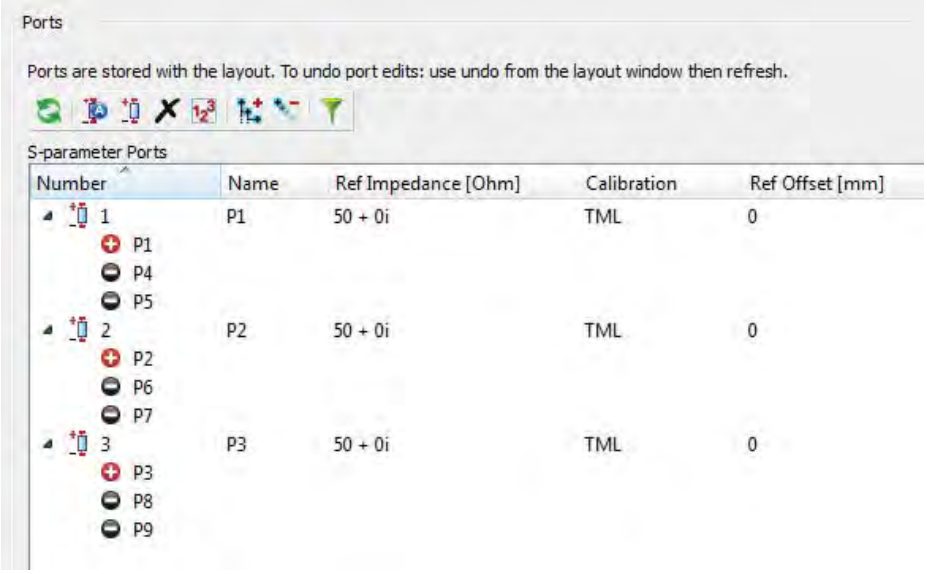
5. Go to Ports option in the EM setup windpw and select Ports 4 – 9, right click and delete so that they are removed from the list and appear at the bottom side.



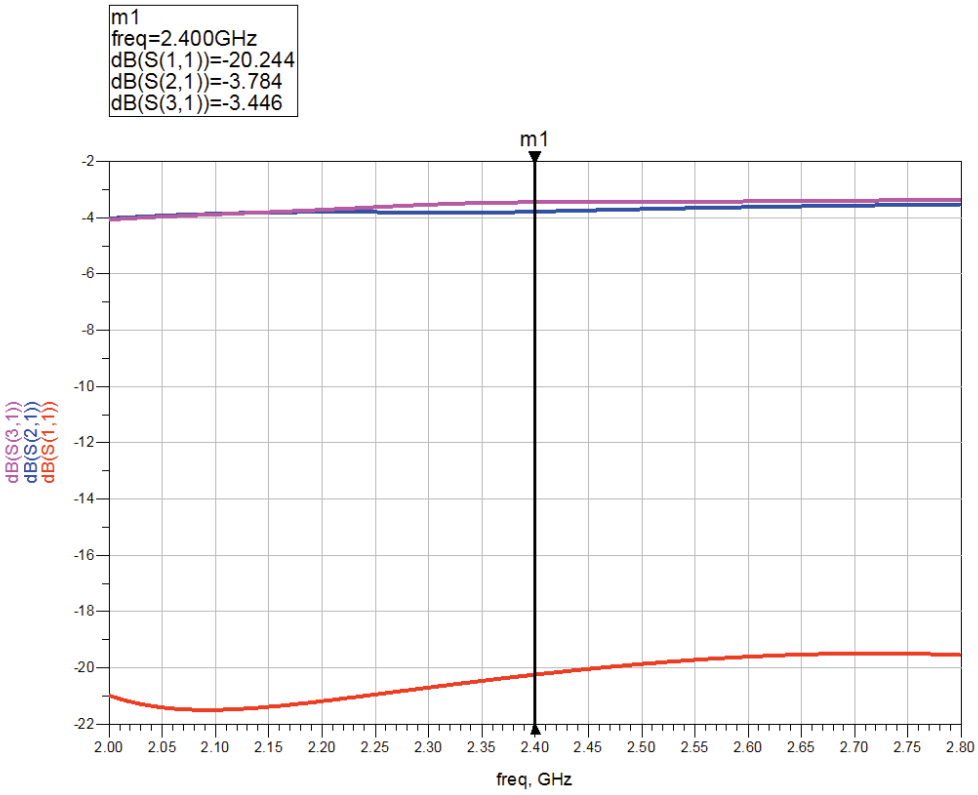
6. From the Unconnected Layout Pins, drag and drop P4 and P5 which placed on either side of P1 in layout on –GND so that it looks as below. Do the similar things for P2 and P3 using the respective unconnected Layout Pins.



7. Once done, it Port assignment will be as shown below



8. Setup simulation frequency as 2 GHz – 2.8 GHz and switch on Edge Mesh from Options->Mesh option of EM setup window. Perform simulation and plot desired response to observe Simulation Results as shown below



Chapter 10: Microwave Amplifier Design

Article originally published in Microwave Product Digest, January 2006 issue with title Amplifier Design Made Easy. Reproduced with permission

ADS Licenses Used:

- **Linear Simulation**

Chapter 10: Microwave Amplifier Design

Abstract

The purpose of this paper is to help designers understand a simple procedure to design and develop Amplifiers. There are many text books available on the Amplifier theory and design but they always leave a gap between theory and practical considerations that should be understood by a designer to produce a good amplifier circuit that compares well with the simulated data so that minimal or almost no post production tuning is required for the Amplifier. This paper tries to collect basic theory of Amplifier design as well as the practical procedure that needs to be adopted for making design first time success so that designers could save their time and efforts. This paper focuses more on CAD aided design procedure to design amplifiers because CAD software has become a necessity for a design house to design accurately and shorten time to market. The design process utilized in this paper makes use of Agilent Advanced Design System (ADS) software.

1. Introduction:

Amplifier is integral part of any communication system. The purpose of having an amplifier in a system is to boost the signal to the desired level. It also helps in keeping the signal well above noise so that it could be analyzed easily and accurately. Choice of amplifier topology is dependent on the individual system requirements and they could be designed for Low Frequency applications, medium to high frequency applications, mm-wave applications etc. and depending upon the system in which they are used, amplifiers can adopt many design topologies and could be used at different stages of system and accordingly they are classified as Low Noise Amplifiers, Medium Power Amplifiers, and Power Amplifiers etc. The most common structure that still finds application in many systems tends to be a Hybrid MIC amplifier. The main design concepts for amplifiers regardless of frequency and system remain the same and they need to be understood very clearly by a designer. Specific frequency ranges pose their own unique design challenges and needed to taken care by designers appropriately. This paper focuses on design of a small signal C-band Hybrid MIC amplifier. This procedure is equally valid for other amplifiers operating in other frequency ranges with minor changes in the design procedure.

2. Amplifier Theory:

There are few things that need to be understood by designer before he can start designing amplifiers like stability and matching conditions. These are discussed in the section below, there are many references available on amplifier basic concept and design procedure, the formula presented in this paper are taken from one of them [1]:

2.1 Stability Condition:

Stability analysis is the first step in any amplifier design. The stability of an amplifier or its resistance to oscillate is an important consideration in a design and can be determined from S-parameters, the matching networks, and the terminations. In a two-port network, oscillations are possible when either the input or output port presents a negative resistance [1]. This occurs when $\left|\Gamma_{IN}\right|>1$ or $\left|\Gamma_{OUT}\right|>1$, which for a unilateral device occurs when $\left|S_{11}\right|>1$ or $\left|S_{22}\right|>1$.

Unconditional stability of the circuit is the goal of the amplifier designer. Unconditional stability means that with any passive load presented the input or output of the device, the circuit should not become unstable i.e. it will not oscillate. In general, for a linear 2-port device characterized by S-parameters, the two necessary and sufficient conditions to guarantee unconditional stability are a) K >1 and b) $|\Delta|<1$, where

$$\Delta = S_{11}S_{22} - S_{21}S_{12}$$

$$K = (1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2) / (2\,|S_{21}\,S_{12}|)$$

2.2 Matching Conditions:

Amplifier could be matched for variety of conditions like Low Noise applications, unilateral case and bilateral case. The formulae for each condition are given below for designer's knowledge [1].

Optimum Noise Match:

The matching for lowest possible noise figure over a band of frequencies require that particular source impedance be presented to the input of the transistor. The noise optimizing source impedance is called as $\Gamma_{opt,}$ and is obtained from the manufacturers data sheet. The corresponding load impedance is obtained from the cascade load impedance formula.

$$\Gamma_L = \left(\frac{S_{22}-\Gamma_{opt}\Delta}{1-\Gamma_{opt}S_{11}}\right)^*$$

Unilateral Case:

$$\Gamma_{IN} = S_{11} + \left(\frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L}\right)$$

$$\Gamma_{OUT} = S_{22} + \left(\frac{S_{12} S_{21} \Gamma_S}{1 - S_{11} \Gamma_s} \right)$$

Bilateral Case (when $S_{12} \neq 0$):

$$\Gamma_{Ms} = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1}$$

$$\Gamma_{ML} = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2}$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2$$

$$C_1 = S_{11} - \Delta S_{22}^*$$

$$C_2 = S_{22} - \Delta S_{11}^*$$

The common source configuration is normally chosen for the highest gain per stage. If the stability factor K>1, the network gives MAG. If K<1, the network could cause oscillations i.e. Gmax is infinite and given as

$$G_{max} = \frac{S_{21}}{S_{12}} \left(k - \sqrt{(k^2 - 1)} \right)$$

This should be avoided by locating the region of instability in Γ_S and Γ_L planes.

3. CAD oriented design procedure:

The CAD oriented design procedure consists of following steps, which will be described one by one for reference and understanding of the designers.

3a). DC Analysis

3b). Bias circuit design

3c). Stability analysis

3d). Input and Output matching network design

3e). Overall Amplifier performance optimization

Amplifier Specifications:

Frequency Band: 5.3 GHz – 5.5 GHz

Gain: 12 dB or more

Gain Flatness: +/- 0.25 dB (max.)

Input/Output Return Loss: < -15 dB

DC Power Consumption: 50 mW (max.)

3a). DC Analysis:

Based on the frequency range and the gain requirement CFY67-08 HEMT device was selected for the present amplifier design. The first analysis that needs to be performed is the DC analysis to find out the right bias points for the amplifier. Fig. 5.1 shows the DC analysis setup and Fig. 5.2 shows the DC analysis results for the same. Based on the DC Power consumption and Gm requirement, bias points are selected as Vgs=-0.1V and Vds=3V. ***To get DC IV sweep setup shown below, please click on Insert->Template->FET Curve Tracer, insert the active device (FET) and connect the proper wires and modify the Sweep parameters as per the device selected.***

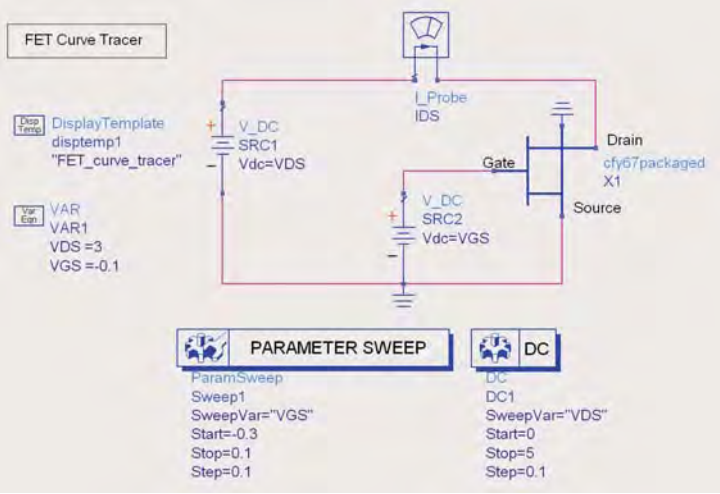


Fig. 5.1 DC Analysis setup for CFY67-08

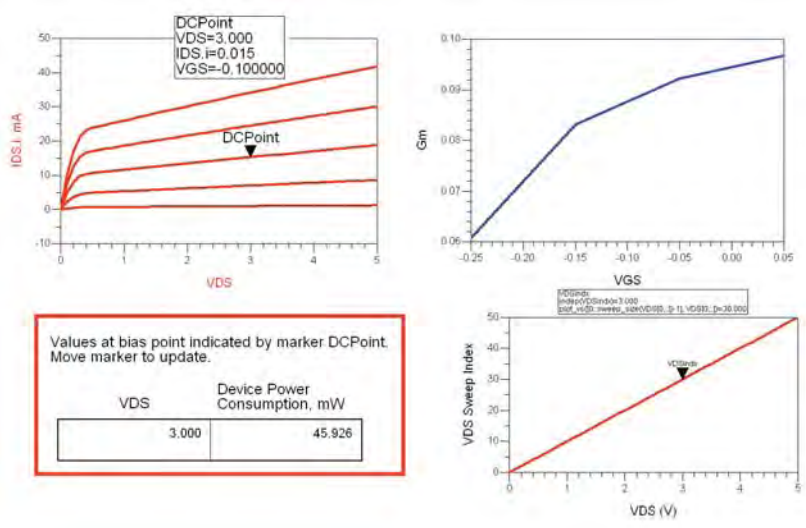


Fig. 5.2 DC Analysis Results

3b). Bias network design:

Bias network design for amplifier is dependent on the frequency range in which amplifier needs to be designed, that is to say if amplifier needs to be design for low frequency application then a choke (inductor) is used but getting discrete inductors at microwave frequencies is difficult so high-impedance quarter wavelength line (λ/4) at centre frequency is the best possible choice which designers can choose to design bias network. ***The thing that needs to be noted in bias circuit design is that more often than not this λ/4 is followed by a resistor or a bypass capacitor and these components adds extra length to the λ/4 line which designers sometime neglect and this could cause some desired RF frequency power to be dissipated in this branch which affects the gain and frequency response of the amplifier, so this***

calculated λ/4 line needs to adjusted by taking proper care of these extra elements and their footprints. One probable and commonly used method is to use Radial stub immediately after λ/4 high impedance bias line which will help to achieve proper isolation at desired RF frequency, no matter what component is added after λ/4 long bias line.

Fig. 5.30 shows the circuit design for bias circuit where it could be seen that high impedance λ/4 bias line is immediately followed by a Radial stub and then by a resistor and capacitor to ground. For more illustration layout of the bias network is shown in Fig. 5.31.

Fig. 5.4 shows the results for bias circuit and it can be seen that this design is acting as a near perfect bias network between 5.3 GHz – 5.5 GHz.

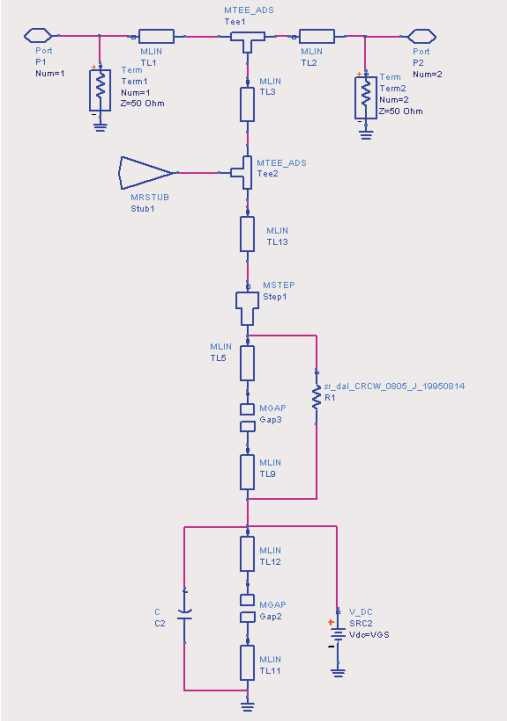


Fig. 5.30 Distributed Bias Network

Fig. 5.31 Layout of Bias Network

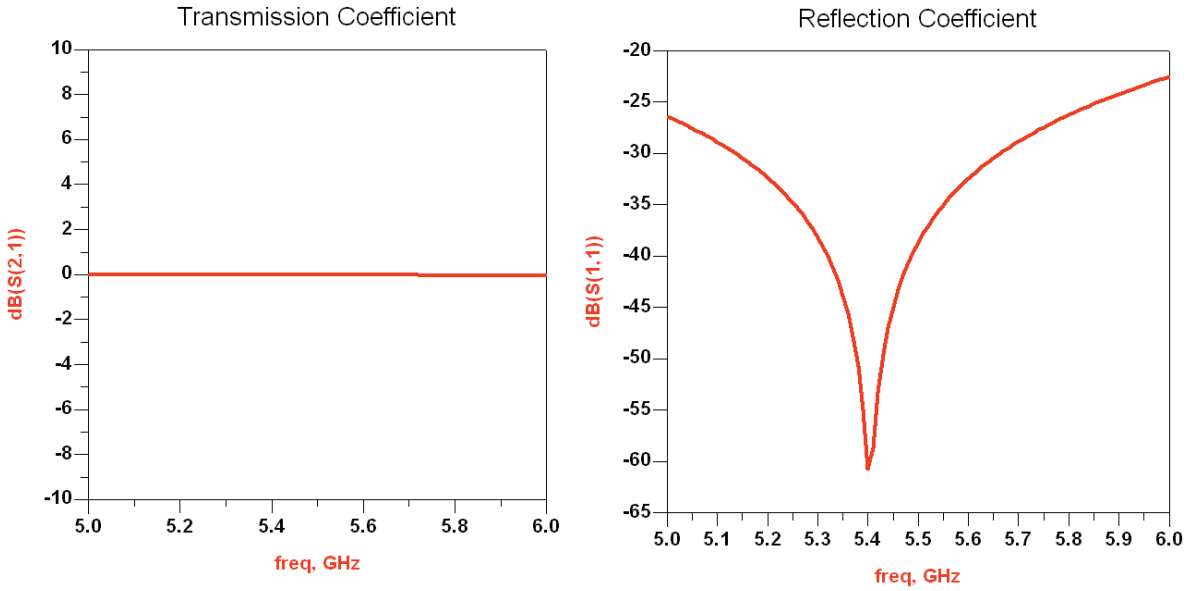


Fig. 5.4 Bias network response

3c). Stability Analysis:

Stability analysis is a very important aspect of any active circuit design and it is equally important in Amplifier design too. Fig 5.50 below shows the circuit that was obtained after adding input and output bias networks. ***Insert StabFact component from the Palette Simulation – S_Parameter to calculate the Stability Factor for the amplifier circuit as shown below.***

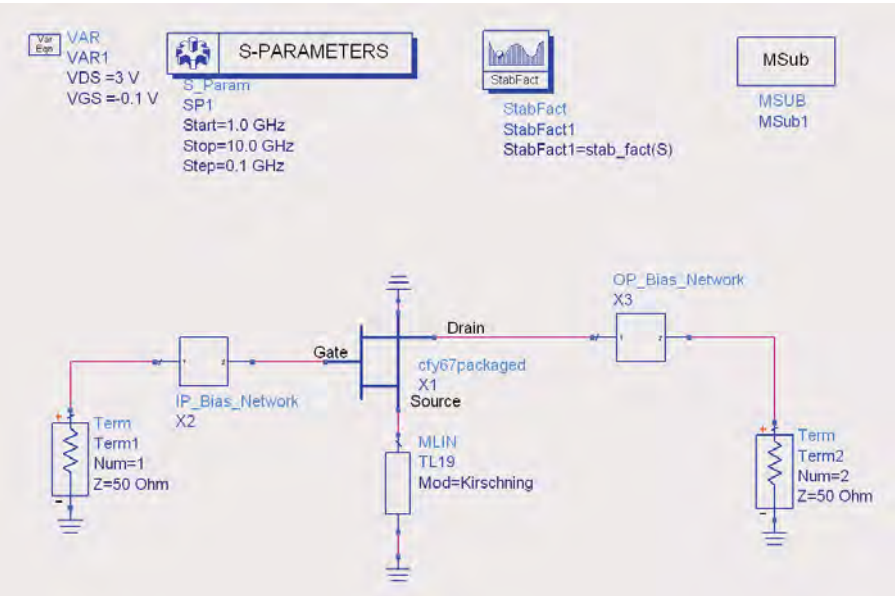


Fig. 5.50 Circuit with input and output bias networks added (shown as sub-circuits)

The results obtained from the circuit above is shown below in the Fig 5.51, which shows that circuit is unstable from ~ 2.1 GHz to 7 GHz and it needs to be stabilized before we can match input and output impedances.

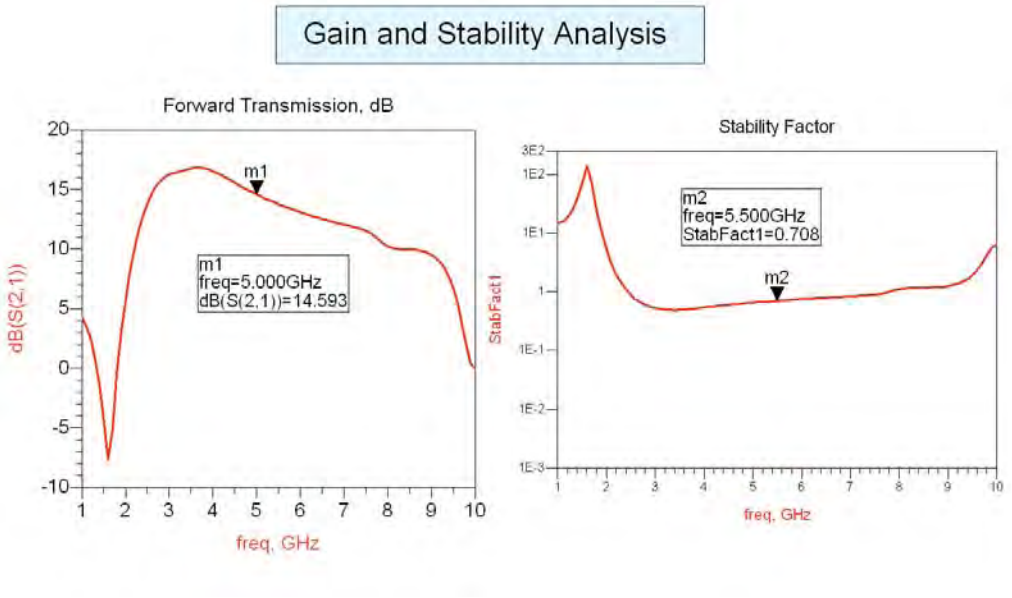


Fig. 5.51 Stability Analysis Results (showing circuit is unstable as K<1)

There are various stability configurations which could be used to stabilize the circuit, the most popular being using resistive loading of the circuit and choice is made depending upon the region of stability and type of amplifier being designed. Fig 5.52 shows one of the techniques to stabilize the circuit.

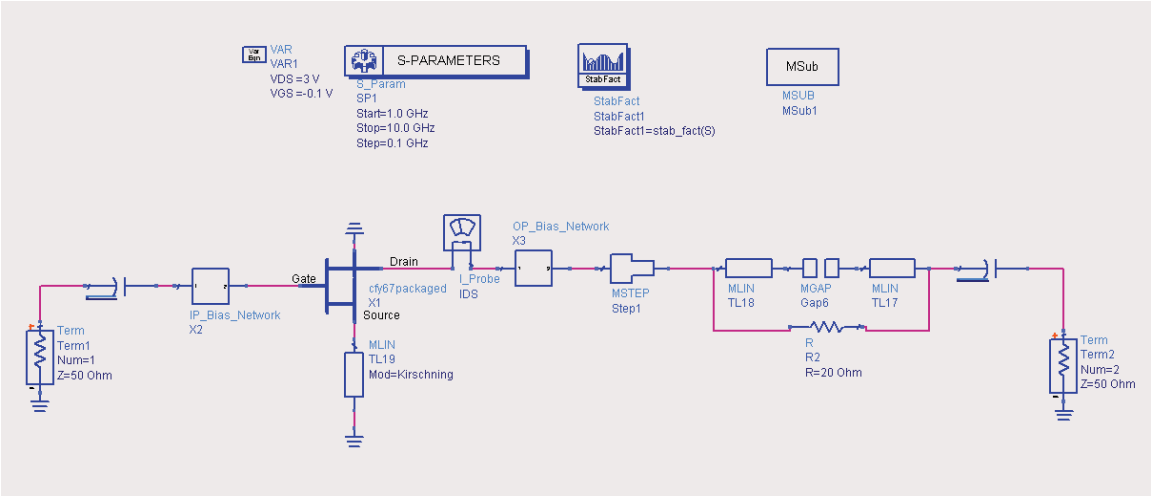


Fig. 5.52 Stabilized Circuit with Resistive loading at the output side (Please note the modeling of Resistor layout footprint which is connected in parallel to resistor, this will allow us to take care of mismatch or distortion introduced because of discrete component's footprint)

One output resistor was used at the output side of the amplifier and then the value of resistor was tuned to achieve the proper stability. Fig 5.53 below shows the results after stabilization.

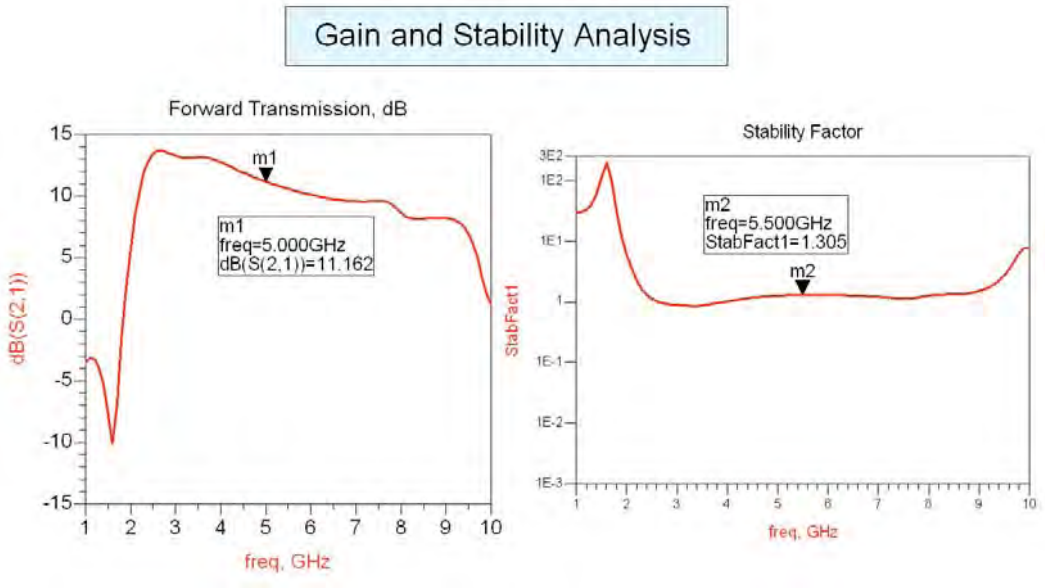


Fig. 5.53 Stabilized Circuit response

3d). Input and Output Matching Network Design:

After the circuit is stabilized in the broadband range, now we can start the design of the input and output matching networks so that we could achieve the desired specification of the amplifier. Fig 5.60 below shows the amplifier after adding bias networks, the stability components and the input and output coupling capacitors. Designers must note the proper layout footprint modeling for lumped components in schematic as shown in Fig. 5.60 below so as to take care of the discontinuities which signal will undergo in practical circuit and this should accompany each lumped components. This is quite important while designing amplifiers in the microwave range.

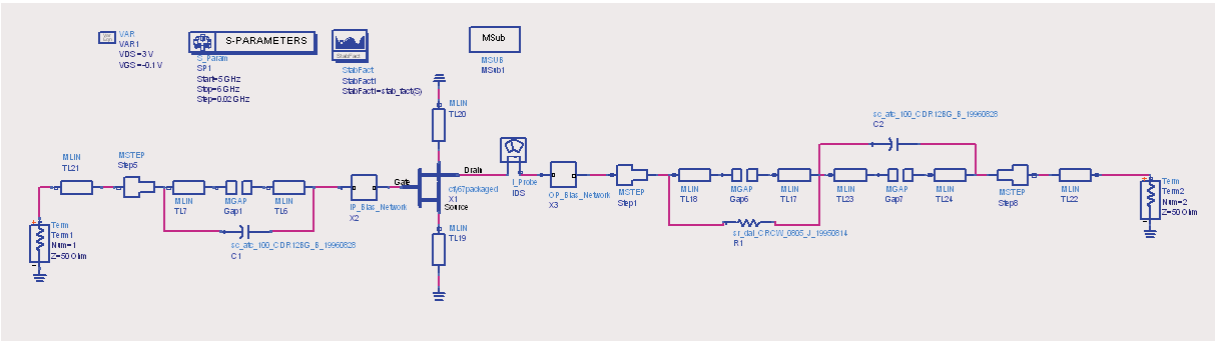


Fig. 5.60 Circuit used for designing input and output matching networks

The choice of the matching networks topology mainly depends on the bandwidth of the amplifier so that designer can choose between Single stub and double stub matching networks. Fig 5.61 below shows input and output impedances on the smith chart which needs to be matched with the 50-ohm impedance.

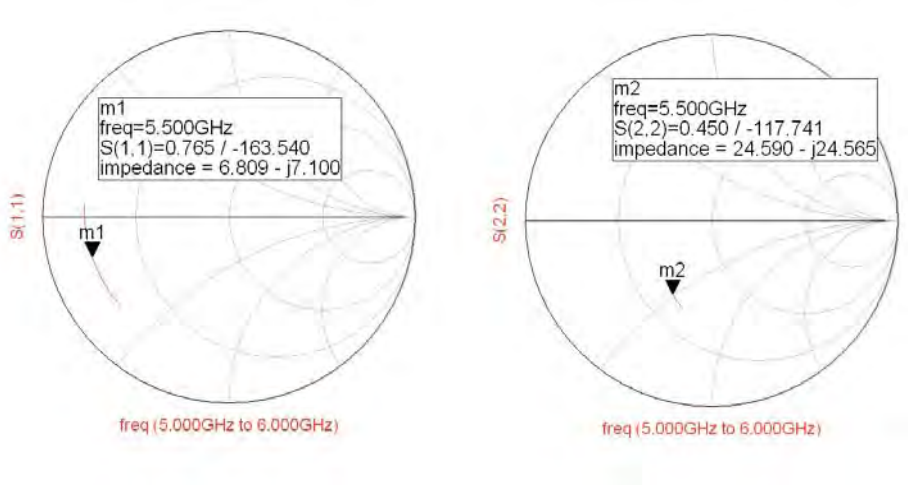


Fig. 5.61 Input and Output impedances on Smith Chart

For the present amplifier design a double stub approach was used to design the input and output matching networks to achieve the best possible input and output return losses. Fig 5.62 and Fig 5.64 below shows the input and output matching networks that were designed using Matching networks synthesis utility available in ADS software. Fig 5.63 and Fig 5.65 shows the results after connecting input and output matching networks to the amplifier circuit.

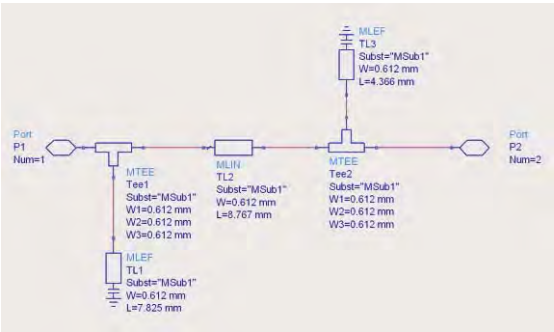


Fig. 5.62 Input Matching network

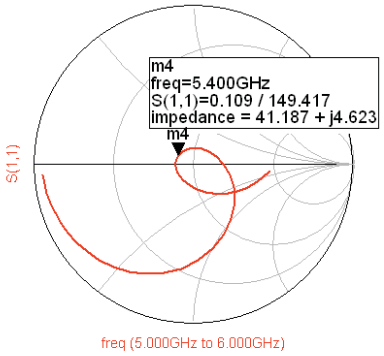


Fig. 5.63 Input Return Loss

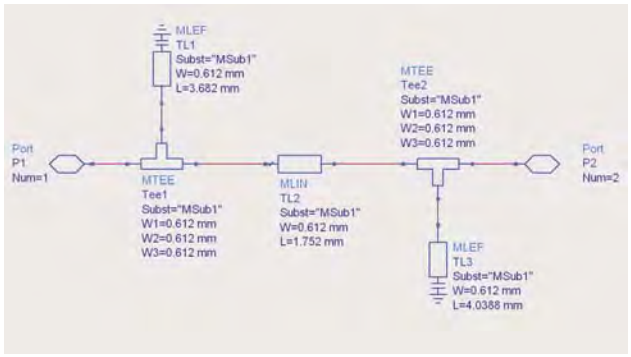


Fig. 5.64 Output Matching network

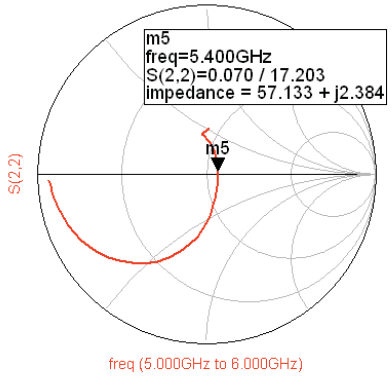


Fig. 5.65 Output Return Loss

3e). Overall Amplifier Performance Optimization:

The only thing remaining now in amplifier design is to connect all the sub-networks together and see the overall amplifier performance and to optimize the overall circuit if needed. Fig 5.70 shows the complete designed amplifier, Fig 5.73 shows the complete layout of the designed amplifier and Fig 5.74 shows the amplifier results and these were obtained after minimal manual tuning of the matching stub lengths to achieve the desired results after each of the blocks together. For clarity the input and output sections of the amplifier are shown in Fig 5.71 and Fig 5.72 respectively.

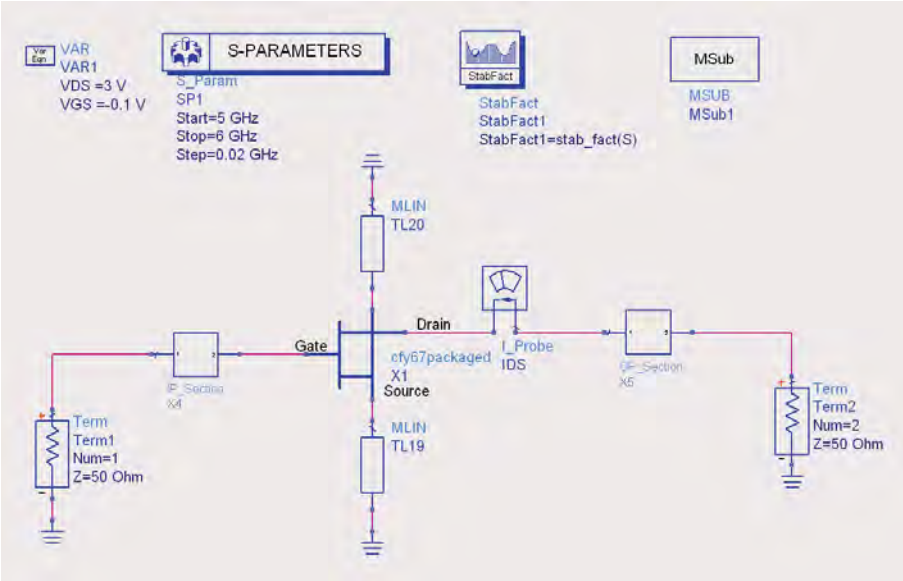


Fig.5.70 Complete Amplifier Schematic (Sub-circuits represents the Input and Output sections)

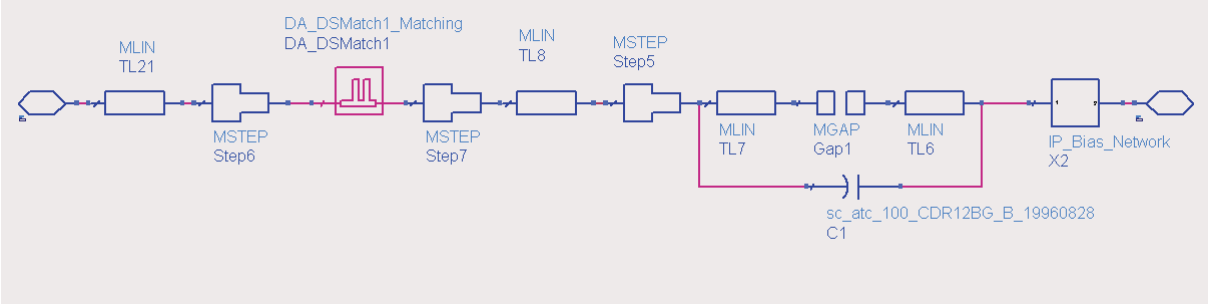


Fig.5.71 Input section of Amplifier

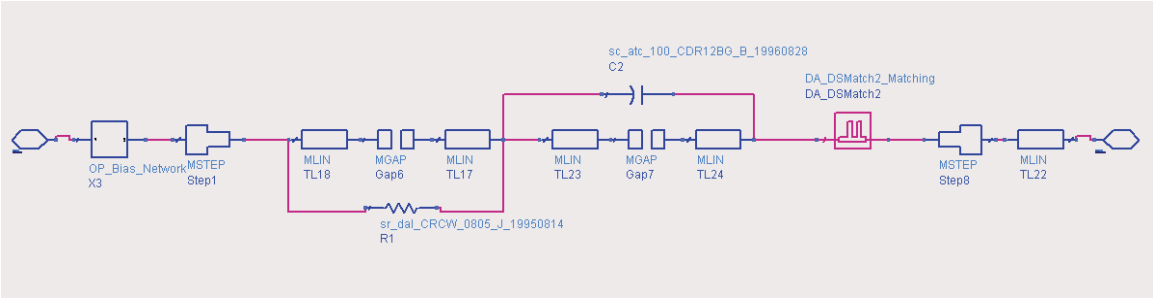


Fig. 5.72 Output Section of Amplifier

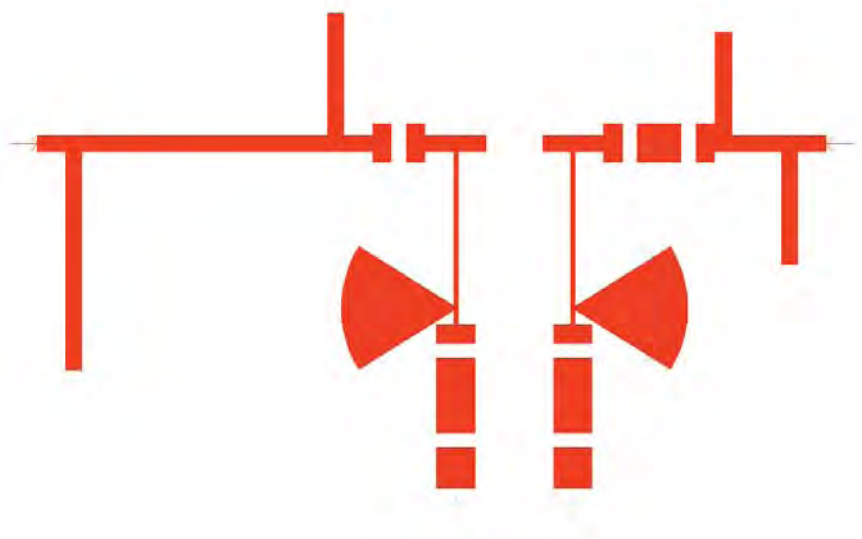


Fig. 5.73 Complete Amplifier Layout (Circuit size can be further reduced by folding the input match line)

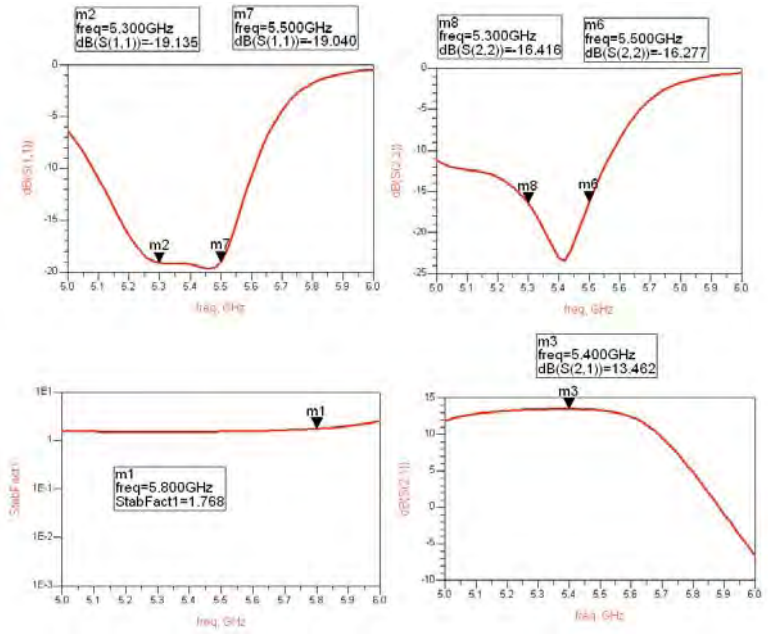


Fig. 5.74 Amplifier Results

4. Conclusion:

It could be seen from above that amplifier designs could be easily done if a well defined procedure is followed and designer could save lot of his time which is spent in fine tuning the amplifier performance optimization.

Chapter 11: Statistical Simulations (Monte Carlo and Yield Analysis)

Article originally published in High Frequency Electronics, January2007 issue with the title "Statistical Analysis of MW circuits predicts Real world performance. Reproduced with permission.

ADS Licenses Used:

- **Linear Simulation**
- **Statistical Design Package**

Chapter 11: Statistical Simulations (Monte Carlo and Yield Analysis)

Introduction:

To obtain good and predictable circuit performance with all the tolerance variations involved could be very challenging. These tolerances could be due to specific process used or because of discrete components used in circuit design and for robust circuit and system design these variations need to be accounted and examined during the circuit or system simulation stages to gain confidence on the design fidelity. This type of simulation is commonly referred to as Statistical analysis. This paper outlines the intricacies of Statistical analysis and makes designers aware about various types of statistical analyses which can be performed to gain additional confidence during the design process. To illustrate the various statistical simulations, a MIC based C-band amplifier design [1] is used.

Process Variations and Discrete component tolerance:

There are multiple sources of variations in the real microwave world which could be associated with Dielectrics, Etching Process and Discrete components etc.

a. **Dielectrics:** Dielectrics can have variations in their height, loss tangent and dielectric constant (Er) and this data can be obtained directly from manufacturer's datasheet.

b. **Etching:** Etching tolerance in printed circuit process is dependent upon the etching technique used and this tolerance mainly affects the width of the transmission lines.

   i. Chemical etching process can have tolerance level of +/- Metal Conductor Thickness (max.)**.**
   ii. Reactive ion etching can produce the excellent tolerance of +/-1um.
   iii. Metal deposition techniques could also produce tolerance of +/- 1-2um

c. **Discrete components:** Discrete components like Inductors, Capacitors, and Resistors etc have their inherent tolerances which could affect circuit performance. Different tolerances for discrete components are summarized in Table 1.

All of above mentioned tolerances should be included into circuit design process as far as possible so that circuit could be analyzed and optimized over these variations. In the present text a typical MIC Amplifier circuit is used for statistical simulations and the variations which are considered are the etching tolerances and discrete component's tolerances to keep the paper simple. Designer can then

take this concept and apply this technique to each variation (e.g. Dielectric parameter tolerances etc) they have in their respective processes.

The substrate which is used for Amplifier design in the present text has following specifications:

Dielectric Height: 25 mils

Dielectric Constant: 9.9

Loss Tangent: 7x10-4

Conductor Thickness: 8 µm

Conductivity: 4.1E+7 (Gold Conductor)

Typical discrete component tolerances are provided in Table1 below:

Component Class	Tolerance
B	+/-0.1 (absolute)
C	+/-0.25 (absolute)
D	+/-0.5 (absolute)
F	1%
G	2%
J	5%
K	10%
M	20%

Table 1: Discrete Component Tolerances

Statistical Design:

To perform the simulation which can take care of real world tolerance variation due to different reasons, designer needs to understand the statistical analysis which is discussed below.

Statistical analysis is the process of:

- Accounting for the random (statistical) variations in the parameters of a design.
- Measuring the effects of these variations.
- Modifying the design to minimize these effects.

Yield analysis is the process of varying a set of parameter values, using specified probability distributions, to determine how many possible combinations result in satisfying predetermined performance specifications.

Yield is the unit of measure for statistical design. It is defined as the ratio of the number of designs that pass the performance specifications to the total number of designs that are produced. It may also be thought of as the probability that a given design sample will pass the specifications.

Because the total number of designs produced may be large or unknown, yield is usually measured over a finite number of design samples or *trials* in the process known as *yield estimation*. As the number of trials becomes large, the yield estimate approaches the true design yield. Parameter values that have statistical variations are referred to as *yield variables*.

Three statistical design options which designer can use in ADS to analyze their circuits are:

a. Monte Carlo analysis:

Monte Carlo yield analysis methods have traditionally been widely used and accepted as a means to estimate yield. The method simply consists of performing a series of trials. Each trial results from randomly generating yield variable values according to statistical-distribution specifications, performing a simulation and evaluating the result against stated performance specifications.

The power of the Monte Carlo method is that the accuracy of the estimate rendered is independent of the number of statistical variables and requires no simplifying assumptions about the probability distribution of either component parameter values or performance responses.

The weakness of this method is that a full network simulation is required for each trial and that many trials are required to obtain high confidence and an accurate estimate of yield.

Monte Carlo Trials and Confidence Levels:

The following text discusses how to calculate the number of trials necessary for a given confidence and estimate error. Confidence level is the area under a normal (Gaussian) curve over a given number of standard deviations. Common values for confidence level are shown in the following table.

Standard Deviations	Confidence Level
1	68.3%
2	95.4%
3	99.7%

Table 2: Table for Confidence Level estimate

Error is the absolute difference between the actual yield, Y, and the yield estimate, $\tilde{Y}$, given by:

$E = |Y - \tilde{Y}|$

where E is the percent error. The low value limit of $\tilde{Y}$ is given by:

$\tilde{Y} = Y - E$

The sample or trial size, N, is then calculated from:

$$N = \left(\frac{C_\sigma}{E}\right)^2 * Y(1-Y) \quad \text{---------- (a)}$$

where, $\mathbf{C_\sigma}$ is the confidence expressed as a number of standard deviations.

Example

For a 95.4% confidence level (i.e. Standard Deviation=2), an Error = +/-2% and a yield of 80%

$$N = \left(\frac{2}{0.02}\right)^2 * 0.8(1-0.8)$$

N=1600 trials

b. Yield analysis:

This process involves simulating the design over a given number of trials in which the yield variables have values that vary randomly about their nominal values with specified probability distribution functions. **The numbers of passing and failing trials are recorded and these numbers are used to compute an estimate of the yield. In the nutshell Yield means how many percentages of circuits meet the desired specifications set as Goal by designer.**

Yield analysis is based on the Monte Carlo method. A series of trials is run in which random values are assigned to all of design's statistical variables, a simulation is performed, and the yield specifications are checked against the simulated measurement values. The number of passing and failing simulations is accumulated over the set of trials and used to compute the yield estimate.

Confidence Tables:

The confidence tables that can be followed to determine the number of trials suitable for yield analysis for different confidence levels and yield of 90% are given below, for more tables designers can refer to software documentation [2].

Confidence=68.3% ***Actual Yield=90%***

Error +/- %	Estimated % yield		Number of Trials
	Low	High	
1	89	91	900
2	88	92	225
3	87	93	100
4	86	94	56
5	85	95	36
6	84	96	25
7	83	97	18
8	82	98	14
9	81	99	11
10	80	100	9

Confidence=95% ***Actual Yield=90%***

Error +/- %	Estimated % yield		Number of Trials
	Low	High	
1	89	91	3457
2	88	92	864
3	87	93	384
4	86	94	216
5	85	95	138
6	84	96	96
7	83	97	70
8	82	98	54
9	81	99	42
10	80	100	34

Confidence=99% ***Actual Yield=90%***

Error +/- %	Estimated % yield		Number of Trials
	Low	High	
1	89	91	5967
2	88	92	1491
3	87	93	663
4	86	94	372
5	85	95	238
6	84	96	165
7	83	97	121
8	82	98	93
9	81	99	73
10	80	100	59

Table 3: Confidence Table for Yield Analysis

c. Yield optimization:

Yield optimization adjusts nominal values of selected element parameters to maximize yield. **Also referred to as design centering, yield optimization is the process in which the nominal values of yield variables are adjusted to maximize the yield estimate.**

To have control over the confidence level and hence the accuracy of the yield estimate, it is recommended that designer perform a yield analysis after the yield optimization is completed, using the nominal parameter values obtained from the yield optimization. Appropriate number of trials can be chosen based upon the formula mentioned in Eqn (1).

Performing Statistical analysis without good simulation tool is not possible and also this could be a time consuming process because of large number of trials involved. The simulation tool should have the capability to perform Yield Analysis, Monte Carlo Analysis and Yield Optimization which designers can use to make sure that the designed circuit has the capability to sustain real world variations.

Example - Statistical Analysis of C-band MIC Amplifier:

Fig.11a shows complete schematic design for C-band MIC amplifier and Fig. 11b shows optimized circuit performance.

Amplifier Specifications:

Frequency Band: 5.3 GHz – 5.5 GHz

Gain: 13 dB (min)

Input Return Loss: < -15 dB

Output Return Loss: < -15 dB

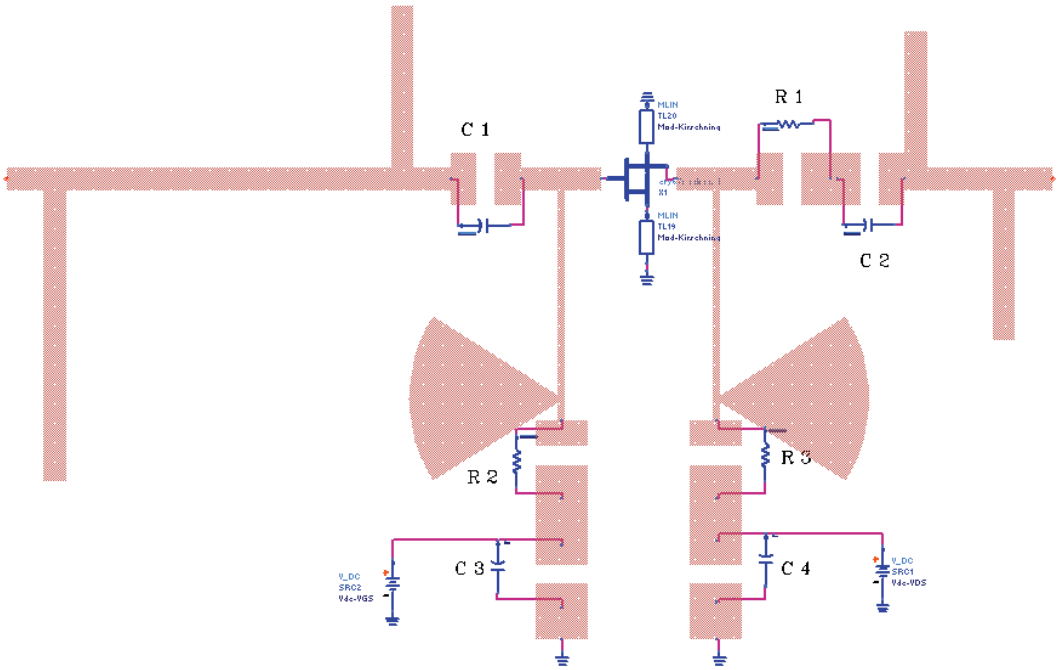


Fig.11a Complete Amplifier Layout

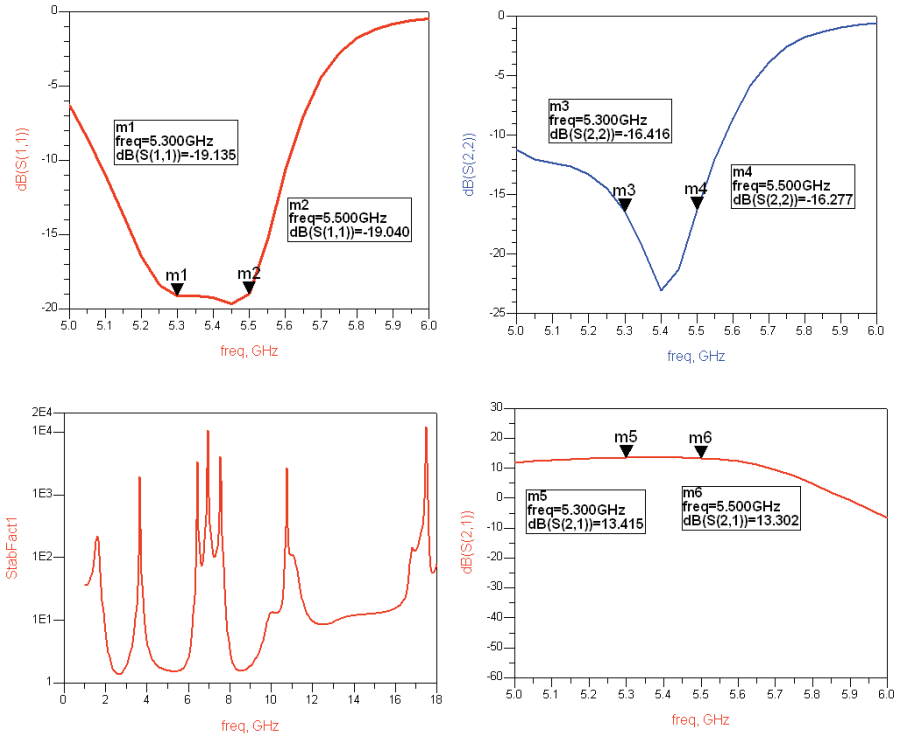


Fig. 11b Optimized Amplifier Performance

Amplifier is designed over 25-mils Alumina substrate as mentioned in (2) above and considering chemical etching process the maximum etching tolerance would be @+/-8um and it also uses few discrete components as given in Table 4.

Component	Value	Tolerance	Purpose
R1	24 ohm	5%	Stability
R2	300 ohm	5%	Stability (Input Bias Line)
R3	10 ohm	5%	Stability (Output Bias Line)
C1	2pF	+/-0.1pF	Coupling Capacitor (Input)
C2	2pF	+/-0.1pF	Coupling Capacitor (Output)
C3	560 pF	10%	Bypass Capacitor (Input)
C4	560 pF	10%	Bypass Capacitor (Output)

Table 4. Discrete Components Tolerance Table

Three steps are needed in order to perform statistical analysis:

a. Define tolerance on the components/transmission lines
b. Setup the performance yardstick to be met
c. Defining number of trials and selection of Statistical analysis method (Monte Carlo or Yield Analysis)

All the transmission line widths were given statistical variation of +/-8um using Gaussian distribution function and all the discrete components were provided with the mentioned tolerance as mentioned in Table 4 above.

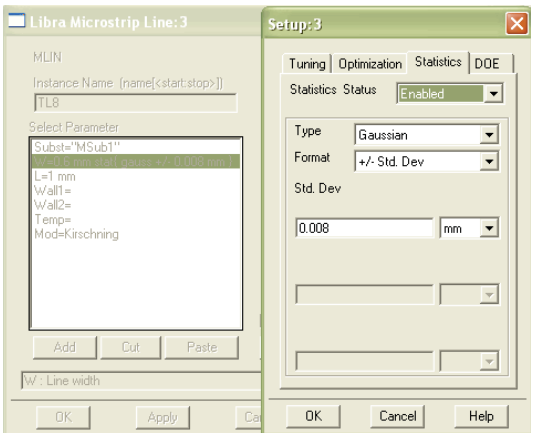


Fig 11c Statistical Variation definition setup for transmission lines

The performance yardstick to be met were set as mentioned under Amplifier Specification and shown in Fig.12.

Fig 12. Yield Analysis setup for statistical analysis in simulation

The numbers of trials were selected as 5000 and yield analysis method was selected to view the pass percentage after the statistical analysis. The initial results obtained are shown in Fig 13 which depicts the yield percentage to be @81% which pretty good for first iteration. The Fig 13 also shows number of circuits which passed the required specification and number circuits which failed during the specifications.

Yield	NumFail	NumPass
80.940	953.000	4047.000

Fig 13. Initial Yield Analysis Results

For the production type circuits this yield should be increased to atleast >90-95% after running initial yield analysis designer has the choice to perform the Yield Optimization or Sensitivity Analysis over the circuit to improve the yield which is not discussed in the present article. Designer with little bit experience can also take some alternative approach to find the reason for lower yield and once the reason is known they can always modify circuit a bit in order to improve the yield of the circuit.

To obtain the reason for lower yield, another yield analysis was performed with only 250 iterations and data for each iteration was saved so that we can have a closer look at the specifications which were not complying with the yield specifications and are shown in Fig 14.

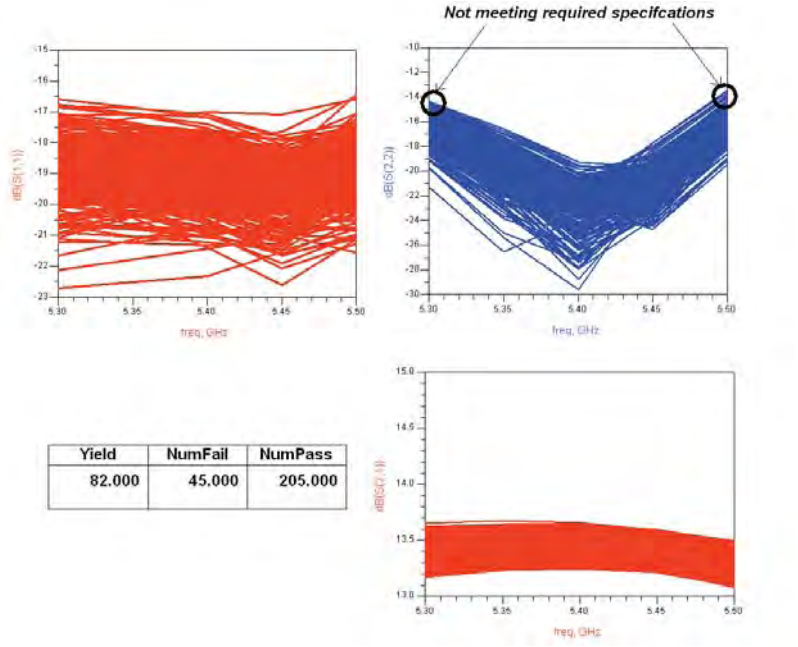


Fig 14 Yield Analysis Results (250 iterations)

It can be seen from Fig 14 that Input Return Loss and Gain specifications has no contribution in lower yield, the main culprit for lower yield is the Output Return Loss which is **slightly** below desired specifications on lower and upper band edges. Designers can perform Yield Optimization to centre the design to account for these statistical variations.

On the other hand taking a closer look at the results provided in Fig 14, it can be seen that although the yield percentage figure is not looking good as a percentage number but the output return loss is just a fraction lower than required specs, another round of yield analysis was performed with target specification for output return loss (S22) changed to -14 dB and excellent yield of 98.5% was obtained which is shown in Fig 15.

Yield	NumFail	NumPass
98.500	75.000	4925.000

Fig 15. Yield Analysis Results with S22 goal as -14dB

Conclusion:

It can be seen that performing yield analysis is pretty essential for the production type circuits and using sophisticated simulation tools designers have the flexibility to perform complex statistical simulation with great ease and they can increase the reliability of the designed circuits.

Additional Information on Yield Analysis:

Additional material and various Statistical simulation examples can be found at EEsof Knowledge Centre, designers using EEsof can register at:

http://www.agilent.com/find/eesof-knowledgecenter

Registered users can find additional technical notes and examples on Yield Analysis by clicking on link:

https://edasupportweb.soco.agilent.com/portal/page?_pageid=36,39974&_dad=portal&_schema=PORTAL&lang=1&search=yield&corner=1

Chapter 12: MESFET Frequency Multiplier Design

Article originally published in Microwave Journal, June2003 issue, reproduced with permission

ADS Licenses Used:

- **Linear Simulation**
- **Harmonic Balance**

Chapter 12: MESFET Frequency Multiplier Design

Abstract: *The design of nonlinear circuits is usually viewed as a challenge; the foremost reason being the difficulty in determining the accurate models that describe device behavior over a wide range of conditions, including varying frequency and power levels. The matters are made worse in microwaves due to high frequency issues (such as model complexity and dispersion).*

A practical and easiest approach to nonlinear microwave circuit development is to use any of the non-linear circuit simulators as a substitute to constructing many prototypes and thus saving lots of man-hours and effort. This paper intends to collect the theory of MESFET Frequency multiplier and to show how to design a MESFET Multiplier using simple simulation procedure without going into much of theoretical aspects of MESFET Multiplier design, still formulae to design multiplier are provided here for those who are interested in theoretical knowledge of the same. This paper will provide insights of MESFET multiplier design & simulation so that this could help the engineers working in this arena of Non-linear Microwave to design & develop MESFET Frequency Multiplier.

1. Introduction:

Fig.1 shows the generalized circuit schematic of a MESFET frequency multiplier. The basic principal of operation of a MESFET multiplier is that the device is operated for a particular conduction angle based on the harmonic frequency to be generated. Table 1 shows the Fourier components as function of conduction angle upto the 5^{th} harmonic. It can be seen that the generalized circuit shown here appears to be identical to the power amplifier; the only difference is that the output resonator is tuned to the n^{th} harmonic of the fundamental, not the fundamental frequency.

2. FET Multiplier over SRD Multipliers:

Unlike diodes, MESFET's currents cannot be described by a single equation and thus require a more complex treatment to describe their nonlinear operation. Comparison of MESFET and Schottky diode multipliers is not simple and requires engineering judgment for the specific application. For instance, frequency doublers built with Schottky-barrier diodes, are lossy (in general >10dB), require no tuning elements, and can operate over octave bandwidth, a performance that cannot be attainable with MESFETs. On the other hand, if bandwidth is less than 50%, MESFET multiplier has great advantage over SRD multipliers and that is, FET multipliers can achieve conversion gain that is greater than unity (generally kept as unity) depending upon the bandwidth while maintaining good dc-RF efficiency

However, by intuition we can conclude that transistors offer several other advantages compared to diodes viz., isolation from input to output so that usually it suffices to match the input at the fundamental frequency, and the use of only bandpass filter at the output. They also require much less drive power for generating significant output power level. An additional advantage of MESFET is that they are a natural part of MMIC's where power efficient frequency multipliers can be designed to fit a

specific need and that would save weight, size and power consumption. These factors are always of great importance in Deep Space Missions or even in terrestrial satellites.

3. Non-linearities involved in MESFETs:

There are three non-linearities, which can be utilized to generate harmonic frequencies.

Gate-Source Capacitance (C_{gs}):

The first is the use of the FET gate-source capacitance (C_{gs}), this non-linearity has been analyzed as a lossy varactor that resulted in harmonic frequency signal levels of -18 to -11 dB below the expected fundamental frequency output power level. [5]

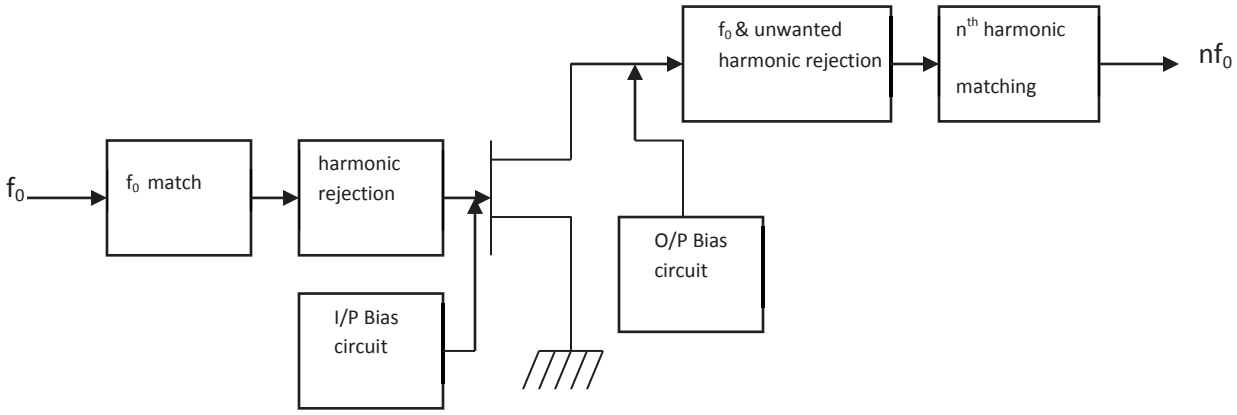


Fig.1 Generalized block diagram of a FET Frequency Multiplier

Fourier Frequency Components						
n	θ_t	I_1/I_p	I_2/I_p	I_3/I_p	I_4/I_p	I_5/I_p
1	**360°**	**-6.0 dB**	**-----**	**-----**	**-----**	**-----**
2	**120°**	**-8.4 dB**	**-12.0 dB**	**-17.0 dB**	**-32.0 dB**	**-----**
3	**76°**	**-12.0 dB**	**-13.2 dB**	**-15.4 dB**	**-18.4 dB**	**-24.0 dB**
4	**65°**	**-13.4 dB**	**-15.4 dB**	**-15.9 dB**	**-18.0 dB**	**-20.0 dB**
5	**48°**	**-14.7 dB**	**-14.9 dB**	**-16.4 dB**	**-18.2 dB**	**-18.4 dB**
pinch-off	**180°**	**-6.0 dB**	**-13.2 dB**	**-----**	**-27.0 dB**	**-----**
squarewave	**360°**	**-3.9 dB**	**-----**	**-13.5 dB**	**-----**	**-17.9 dB**

Table 1. Fourier Components as Function of Conduction Angle[6]

Drain-Source characteristics:

The second non-linearity arises from clipping of the I_{ds} waveform. This effect can be induced by biasing the device at **0 V or at pinch-off** and causing a half-wave rectified sinusoidal output voltage which has a theoretical second harmonic level of 7.4 dB below the fundamental frequency output signal. [5]

V_{gs}-I_{ds} transfer characteristics:

The third non-linearity is due to the non-linear V_{gs}-I_{ds} transfer characteristic. FET devices generally exhibit good linearity and as a result, this feature does not contribute significantly to multiplier performance.

Simulations using a unilateral FET model[5] have shown that the non-linearity which is the largest contributor to harmonic generation is the clipping of the I_{ds} waveform with less significant contributions from the C_{gs} and transfer non-linearities.

In order to optimize the harmonic generation of the frequency multiplier, attention must be paid to the terminations [3-6] that are presented at the device output to the fundamental and n^{th} harmonic frequency signals. Biasing the gate at 0 V (or pinch-off) to create a half-wave rectified output will provide better conversion efficiency if the fundamental frequency signal is terminated in an open circuit and the n^{th} harmonic frequency is extracted by a matched load. This allows a maximum voltage swing of the rectified sinusoidal waveform, which is rich in n^{th} harmonic signal content.

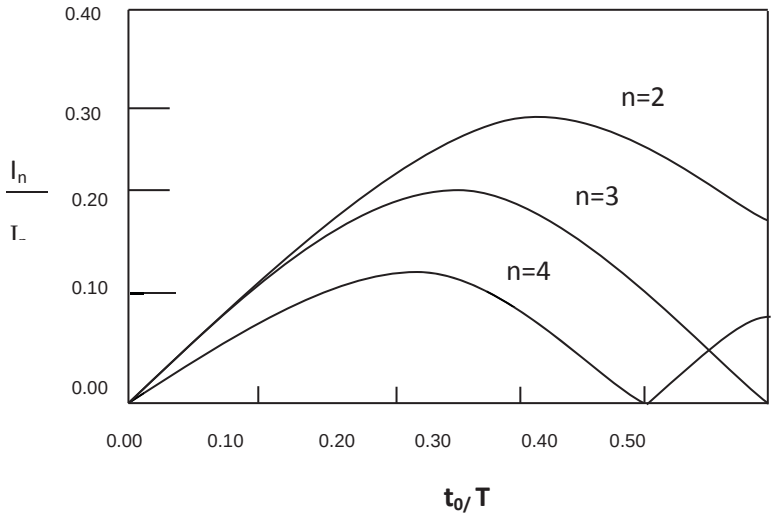


Fig. 2 Harmonic drain-current components as a function of t_0/T when the drain-current waveform is a half-sinusoidal pulse train.

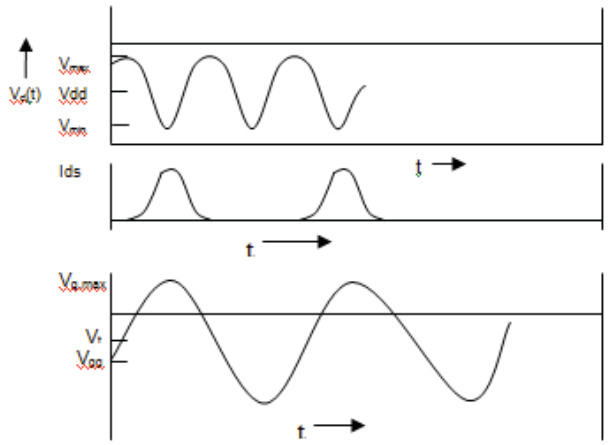


Fig.3. Voltage and Current waveform of an ideal MESFET Frequency Multiplier

4. Selection of Non-linear model for MESFET:

Selection of the proper non-linear model for device to be used for Simulation purposes plays a very important role in designing a Non-linear circuit accurately. The choice is available for choosing appropriate nonlinear MESFET device models such as Statz, Curtice Cubic, TOM etc. Distinctions of these three models are given below and user can select a appropriate device model which characterizes the intended device to be used to the good accuracy. Also, there may be slight differences in the way a model is implemented in commercial simulators. Although the same model exists in multiple simulators, each simulator may use slightly different variable names. For example, most GaAs FET models contain a zero bias gate-source junction capacitance. In PSPICE and MDS this capacitance is defined as the variable CGS; in LIBRA and COMPACT it is defined as CGSO. These differences require the user to translate model parameters to conform to the syntax of their specific simulator to be used for circuit simulation purpose.

4.1. Statz Model:

The Statz model is more accurate when the I_{ds} for a device behaves quadratically (square-law approximation) for the small values of (V_{gg} - V_p) and linearly for large value of (V_{gg} - V_p).

4.2. Curtice Model:

The Curtice model is useful when extracting a model at a single bias point.

4.3. Triquint's Own Model (TOM):

TOM is more accurate when the square-law approximation does not predict device performance well and when the device drain conductance varies with gate-source bias.

Note: More details on Non-Linear models can be obtained from ADS software documentation

5. Design of FET Frequency Multiplier:

➢ Design of frequency multiplier can be initiated by selecting the appropriate Gate voltage to control the conduction angle of the FET keeping in mind the prominent harmonic to be generated and the appropriate Drain voltage needs to be selected. The peak reverse voltage across gate has to be taken into account if the MESFET is being biased much below pinch-off voltage (i.e. if $V_{gg} << V_t$). The typical reverse voltage across gate can be approximated by the expression $2Vgg - V_{g,max}$, a relatively high reverse voltage.

➢ The input bias network typically includes a high impedance line of $\lambda/4$ length at f_o (fundamental frequency) so that no fundamental power goes into the DC bias which is connected via a bypass capacitor to ground in parallel. The high impedance line of $\lambda/4$ length at f_o becomes $\lambda/2$ length at $2f_o$ (second harmonic) frequency so it acts as a short circuit at second harmonic frequency.

The Gate's short circuit at the second harmonic frequency is less critical, a shorted stub $\lambda/4$ long at fundamental frequency is adequate to provide the termination. Similarly, a high impedance line of $\lambda/4$ length at the output centre frequency (nf_o) was used for Drain biasing purposes which was connected via a bypass capacitor to ground in parallel.

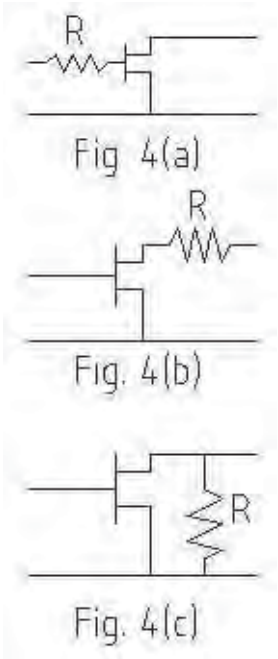


Fig. 4 Stabilization Techniques

The most important thing, which needs to be addressed carefully, is the stability of the circuit. If the circuit is not stable over the full frequency band then it needs to be stabilized, any of the stabilization techniques shown in Fig. 4(a), 4(b) and 4(c) can be used to serve the purpose. Although any of the topology can be used but care must be taken in employing the best possible configuration according to

the stabilizing requirement of the circuit and also keeping the RF power dissipation to the minimal extent due to stabilization components.

The stability of the circuit is of utmost importance and under any circumstances the stability factor (K) of the circuit has to be greater than '1' no matter if some of the conversion gain of the multiplier needs to be sacrificed.

➢ Rejection of the other unwanted harmonics present in the output can be accomplished by proper open or short-circuited stub arrangement. These stubs could be open or short-circuited stubs based on the convenience and the size of the circuit. The open-circuited stubs of $\lambda/4$ length on various harmonic frequencies can be connected in shunt to the drain so that drain see short circuit load at unwanted harmonics. The nominal widths of these shunted stubs could be 50 ohms or other depending on circuit requirement.

If multiplier needs to be realized for a moderate bandwidth, then a Bandpass filter could be connected at the output to get the best possible flatness over the entire output band. The open or short-circuited stubs that are used for rejection of unwanted harmonics in the output tend to limit the bandwidth due to their dispersive effect. The choice of the topology of the Bandpass filter depends on the individual's judgment and the system lineup requirements. For example if the output frequency is high (near Ku-band) then a **half wave filter** which consists of cascaded alternate lines of high and low impedances of length $\boldsymbol{\lambda/2}$ at desired harmonic frequency would be a good choice. This filter will provide moderate to high bandwidth without consuming too much of space in the circuit and if the output frequency lies in the C-band then a Hairpin bandpass filter topology will be a good choice to get the required rejection of the harmonics present in the output, also the space occupied will be less than that in the case of Coupled line bandpass filter topology. If the size requirement of the circuit is not that critical then a Coupled line filter can be used in the output.

It is now remaining to match the input and output sections of the circuit to the 50-ohm source and load terminations.

For this purpose, the use of Large Signal S - parameter simulation technique which is available in all the RF/Microwave Non-linear simulators is needed, these are power dependent parameters and the required power source needs to be connected at the input of the device.

The circuit can be re-optimized for better performance like Conversion gain, input / output return loss etc using the Non-linear simulator.

6. Simulation of MESFET Frequency Multiplier:

The simulated design presented here is for the MESFET Frequency Tripler using Non-linear model of ATF21170 MESFET available in Agilent ADS RF transistor library at the input frequency of 1500 MHz with a input bandwidth of $\pm$ 50 MHz. The gate and drain bias was fixed based on the maximum output power at the required 3rd harmonic after simulating the MESFET for an input power of +4dBm using Harmonic

Balance analysis of ADS software. The peak reverse voltage across the gate was also taken into account so that it doesn't cross the maximum specified limit of the MESFET used for design.

The input and output bias network was then designed by using a high impedance quarter wavelength ($\lambda/4$) line at input and output centre frequencies respectively.

The first thing that was established was the stability of the circuit after deciding the Gate and Drain voltages and designing the input and output bias network. The linear S-parameter simulation of the ADS was used for this purpose. The circuit was not stable over full frequency band so a resistor was connected in series with the gate (Rs1) and one series resistor (Rs2) and capacitor (Cs1) combination was connected in shunt with the gate. The values of Resistors were tuned till the stability factor of greater then '1' was achieved. The care was taken to keep the value of resistor in series with Gate to be as minimum as possible so that it doesn't consume much of input power and also the value of shunt resistor was kept as maximum as possible.

A 3-section coupled line Bandpass filter at the center frequency of 4500 MHz (3^{rd} harmonic) was connected at the output to provide nominal rejection of the unwanted harmonics in the output. The topology of the Bandpass filter was selected as Coupled line because of available space for the circuit, any other topology will also serve the purpose if size of the circuit is of major concern.

Large signal S-parameter of the circuit was simulated using ADS software and the input and output matching network was designed so as to match the Gate and Drain impedance with 50 ohms source and load terminations. In the present case single open circuited stub on each side (input & output) was sufficient to match the circuit over the entire bandwidth.

The circuit was re-optimized for better conversion gain, input and output return loss and passband flatness in the output after completing all the sub-networks design. Complete layout for the frequency tripler circuit is shown in fig. 5.1 and the actual fabricated tripler is shown in fig. 5.2.

The circuit was designed and fabricated on 25-mil Alumina substrate with a dielectric constant (Er) of 9.90.

7. Design Formulas for Multiplier:

The drain current of a FET is given by

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gg}}{V_p}\right)^2 \text{ ----------(1)}$$

The conduction angle of the FET can be calculated using the following expression

$$\theta = 2\cos^{-1}\left(\frac{2V_t - V_{g,\max} - V_{g,\min}}{V_{g,\max} - V_{g,\min}}\right) \quad \text{---------- (2)}$$

The bias voltage which achieves this value of θ is

$$V_{gg} = \left(\frac{V_{g,\min} + V_{g,\max}}{2}\right) \quad \text{---------- (3)}$$

The current in the load resistor, R_L, is I_n. For

the voltage V_L across the load to vary between V_{max} and V_{min}

$$\left|V_L(t)\right| = I_n R_L = \left(\frac{V_{\max} - V_{\min}}{2}\right) \quad \text{---------- (4)}$$

The Optimum load resistance is

$$R_L = \left(\frac{V_{\max} - V_{\min}}{2I_n}\right) \quad \text{---------- (5)}$$

R_L in a multiplier is usually much greater.

The output power at the n^{th} harmonic, $P_{L,n}$ is

$$\mathrm{P}_{\mathrm{L,\,n}} = \frac{1}{2} I_n{}^2 R_L = \frac{1}{2} I_n \frac{V_{\max} - V_{\min}}{2} \quad \text{---------- (6)}$$

As with a power amplifier, the dc drain bias voltage is halfway between V_{max} and V_{min} that is,

$$V_{dd} = \frac{V_{\max} + V_{\min}}{2} \quad \text{---------- (7)}$$

The dc power is given by the expression

$$P_{dc} = V_{dd} I_{dc} = \frac{1}{2} V_{dd} I_o \quad \text{---------- (8)}$$

So, the dc-RF efficiency can be written as

$$\eta_{dc} = \frac{P_{L,n}}{P_{dc}} \quad \text{---------- (9)}$$

The input power can be approximated by the expression

$$P_{av} = P_{in} = \frac{1}{2}(V_{g,\max} - V_{gg})^2 \omega_p^2 C_{gs}^2 (R_s + R_i + R_g) \text{ ---------- (10)}$$

$$\text{Conversion Gain} = \frac{P_{L,n}}{P_{av}} \quad \text{---------- (11)}$$

The power added efficiency of a FET multiplier is

$$\eta_a = \frac{P_{L,n} - P_{in}}{P_{dc}} \quad \text{---------- (12)}$$

$$\text{or,} \quad \eta_a = \eta_{dc}(1 - \frac{1}{G_p}) \quad \text{---------- (12a)}$$

The maximum drain-gate voltage is approximately V_{max} - $V_{g,min}$, so we have the limitation V_{max} - $V_{g,min}$ < V_a , where V_a is the drain-gate avalanche voltage.

Where, G_p is the power gain ($P_{L,n}/P_{in}$) of the multiplier.

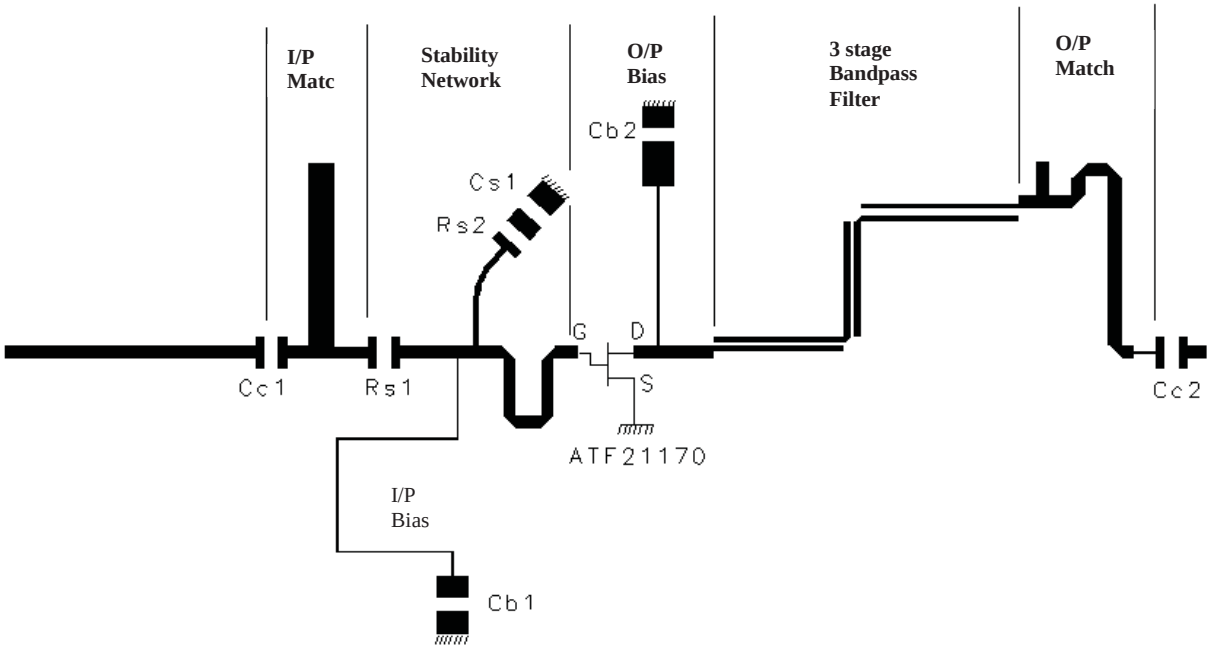


Fig. 5.1 Complete Layout of simulated MESFET Frequency Tripler using ATF21170 under bias condition of Vgg=-0.5 V and Vdd=3.0V and input power of +1 dBm.

8. Simulated and Measured Results:

All the simulated results obtained using Agilent's ADS for the Frequency Tripler are shown in Fig.6.1, 6.2, 6.3 and 6.4. Figures 6.5 & 6.6 shows the measured results.

Fig. 6.1 shows the simulated time domain waveform of the Fundamental and 3rd harmonic current at the output of MESFET. Third harmonic current waveform is shown by thick curve and the amplitude is on left Y-axis. Fundamental current waveform is shown by thin curve and the amplitude is shown on right Y-axis.

Fig. 6.2 shows the simulated time domain waveform of the Fundamental and 3rd harmonic voltage at the output of MESFET. Third harmonic voltage waveform is shown by thick curve and the amplitude is on left Y-axis. Fundamental voltage waveform is shown by thin curve and the amplitude is shown on right Y-axis.

Fig. 6.3 shows the simulated Power Spectrum of the ATF21170 Frequency Tripler. The conversion loss of –1.6 dB was achieved in the simulation for the required third harmonic and the Sideband rejection achieved was greater than 20 dB.

Fig. 6.4 shows the simulated output band flatness of the 3rd harmonic that was achieved to ±0.36 dB in simulation.

Fig. 6.5 shows the measured Power Spectrum of the Frequency Tripler. The conversion loss of –2 dB was measured (which is –0.4 dB more than the simulated results). The sideband rejection of greater than 20 dB was measured.

Fig. 6.6 shows the measured output band flatness of the 3rd harmonic. The measured flatness achieved was ±0.30 dB

Simulated Results:

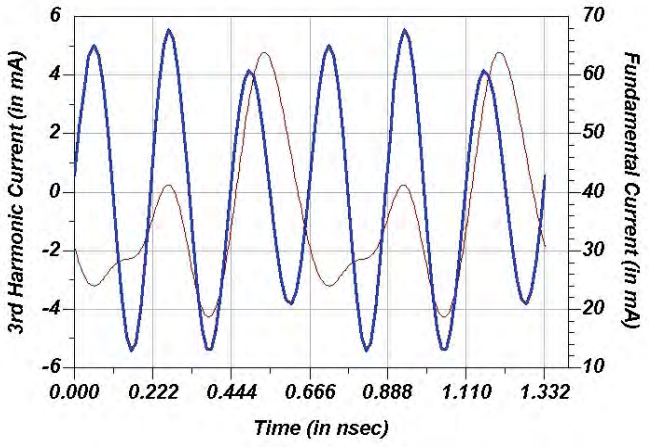


Fig. 6.1-Simulated Time Domain Fundamental & 3rd Harmonic Current waveform

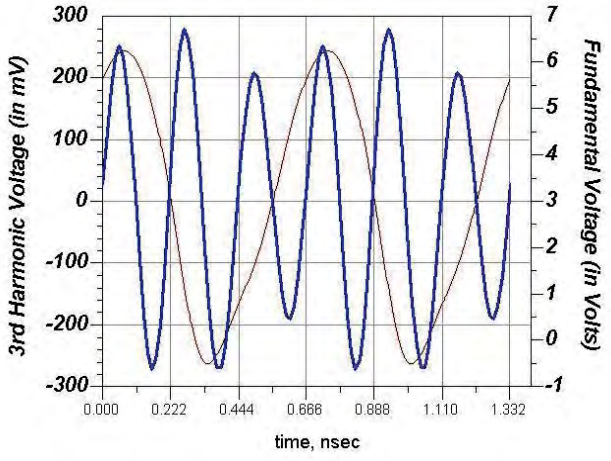


Fig. 6.2- Simulated Time Domain Fundamental & 3rd Harmonic Voltage waveform

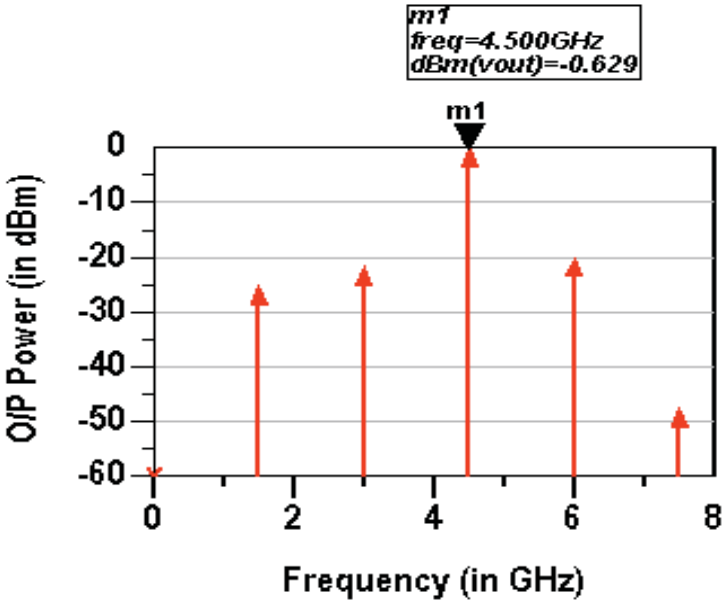


Fig. 6.3-Simulated Output Power Spectrum of Frequency Tripler

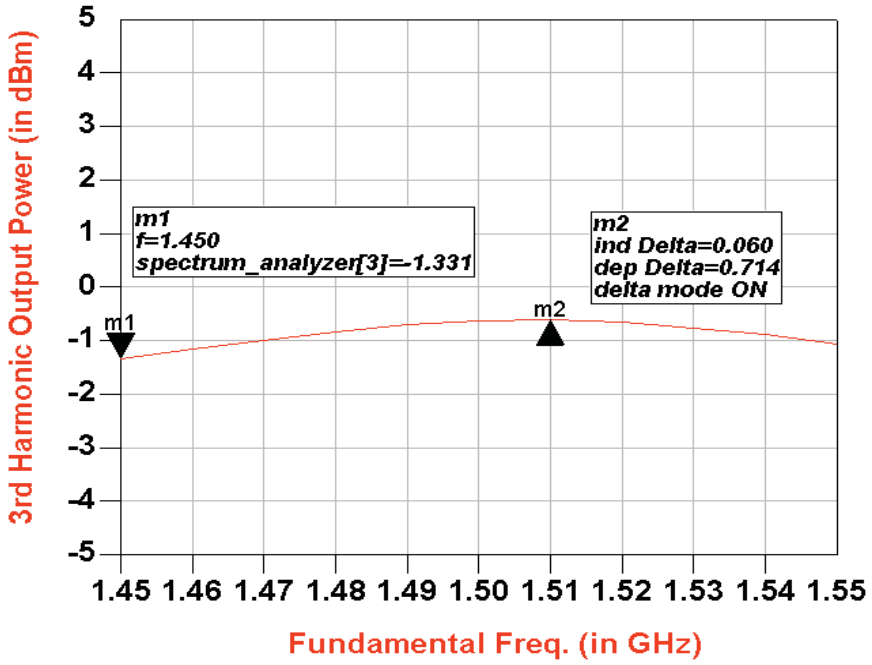


Fig. 6.4-Simulated Output band Flatness of Frequency Tripler

Measured Results:

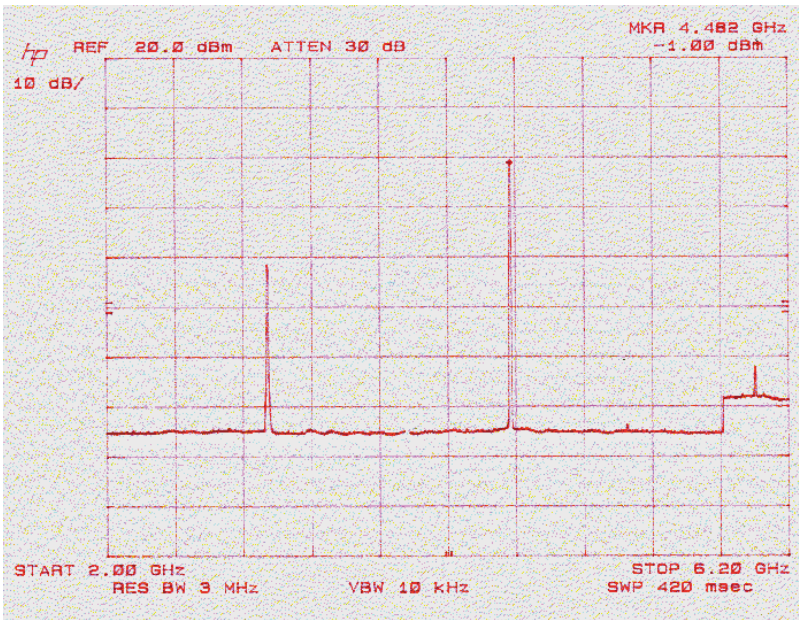


Fig. 6.5-Measured Output Spectrum of Frequency Tripler

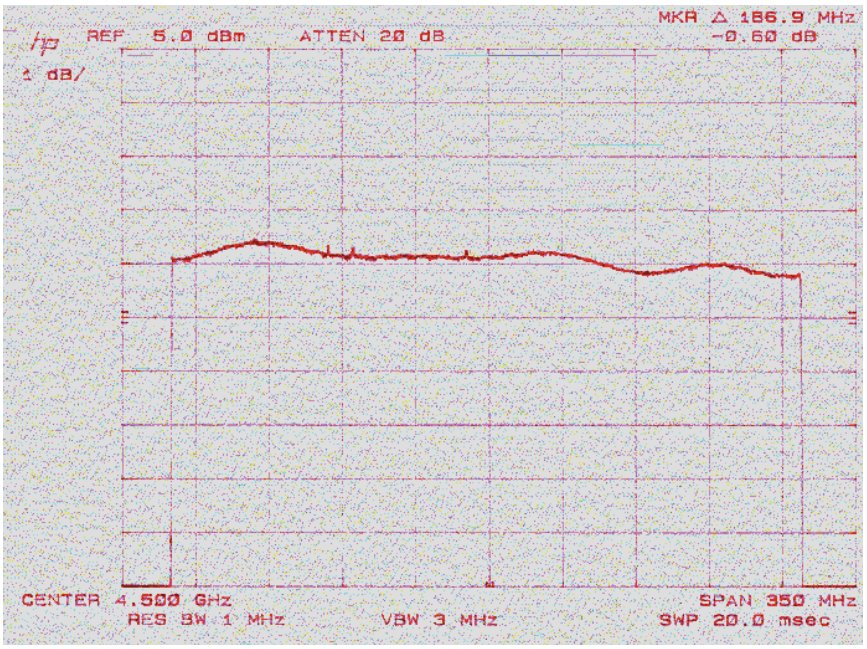


Fig. 6.6-Measured Output band Flatness of Frequency Tripler

List of symbols used:

I_{ds}	**:**	**Drain current**
I_p	:	Peak Drain current
θ_t	:	Conduction Angle
V_p	:	Pinch-off voltage
V_{gg}	:	Gate bias voltage
$V_{g,max}$	:	Max. gate voltage
$V_{g,min}$	:	Min. gate voltage
R_L	:	Load resistance
I_n	:	Current in nth harmonic
$P_{L,n}$	:	O/P power at nth harmonic
V_{dd}	:	Drain bias voltage
P_{dc}	:	DC power
η_{dc}	:	dc-RF efficiency
η_a	:	Power added efficiency
G_p	:	Conversion gain
P_{in}	:	Input power
E_r	:	Dielectric constant
C_{gs}	:	MESFET Gate-Source Capacitance
V_t	:	Turn on voltage of MESFET
$P_{L,n}$	:	n^{th} harmonic output power
P_{dc}	:	DC Power
t_o/T	:	Duty cycle
K	:	Stability Factor

References:

[1] Stephen A. Mass, "*Nonlinear Microwave Circuits*", Artech House

[2] Erik Boch, "A High Efficiency 40 GHz Power FET Frequency Doubler", *Aug.1989, Microwave Journal*.

[3] E. Camargo, R. Soares, R.A. Perichon and M. Goloubkoff, "Sources of Nonlinearity in GaAs MESFET Frequency Multipliers", *IEEE MTT-S Digest, 1983, pp. 343-345.*

[4] C. Rauscher, "High-Frequency Doubler operation of GaAs Field-Effect Transistors", *IEEE MTT, Vol. MTT-31, No.6, June 1983, pp. 462-473.*

[5] A. Gopinath and J.B. Rankin, "Single Gate MESFET Frequency Doublers", *IEEE MTT, Vol. MTT-30, No.6, June 1982, pp. 869-875*

[6] Camargo, Edmar, "*Design of FET Frequency Multipliers and Harmonic Oscillators*", Artech House

[7] Gonzalez, Guillermo, "*Microwave Transistor Amplifiers Analysis and Design*", Prentice-Hall, Inc.

[8] CEL Application note 'AN1023'

Chapter 13: Active Mixer Design

ADS Licenses Used:

- **Linear Simulation**
- **Harmonic Balance**
- **Layout**

Chapter 13: Active Mixer Design

Taken from Agilent EEsof Technical Note: Low Power Mixer Design Example using HP Advanced Design System

Introduction

This note describes a method for designing a low-power single-transistor active mixer using Agilent EEsof Advanced Design System (ADS). It includes details on the design steps,

simulation setups and data displays. The workspace file discussed in this lab is available under the ADS example directory */examples/RF_Board/MixerPager_wrk.7zap*. Unarchive the workspace in working directory by selecting File->Open->Example->RF_Board->MixerPager_wrk.7zap and selecting the working directory to unarchive the example workspace.

Circuit Specifications

The mixer is an upper-sideband downconverter, with an RF of 900 MHz RF, and a 45 MHz IF. The simplified specifications supplied for this design call for it provide 10dB conversion gain, operating from a 1 volt DC supply at 600uA current. This very low power consumption is typical of applications such as pagers and cellular phones, where battery lifetime is critical. Low cost is another driving factor in such applications. Other typical specifications a mixer would have to meet in a "real-world" design, such as linearity, port-to-port isolation, spurious response and noise figure, are not included in this particular example. See */examples/RFIC/Mixers_wrk.7zap* for examples of how to include these simulations in your design.

Device Selection

One of the first steps in the design process is to select the device. The device used for this example is the Motorola MMBR941, a bipolar junction transistor (BJT) packaged in a standard SOT-23 plastic package. While bipolar devices do not generally have as good mixing properties as field-effect transistors, the low operating voltage precludes using FETs in this case. The chosen device has acceptable performance for this application, and offers several other advantages: it is extremely low cost, and accurate models are readily available. As a rule of thumb in high-volume, low-cost applications is to use the least expensive device that will accomplish the job, the MMBR941 is a good choice for this mixer. ***It is equally true that, no matter how good a device is, if there are no models to simulate it with, it becomes impossible to use in a design.***

The device model, taken from the ADS RF Transistor Library, is a Gummel-Poon model where the parameters were extracted by the manufacturer, Motorola. Initially, the model's DC performance is verified by comparing DC I-V curves. Next, a bias network will be designed to establish the desired operating point. The model's RF behavior will then be checked by comparing the simulated S-parameters with measured S-parameters taken at the same bias conditions. Finally, the model's nonlinear performance is verified by simulating gain compression and comparing to measured results.

Device Model DC Verification (Cell: DC_curves)

DC_curves.dsn (see Figure 1) shows one way to set up a swept-parameter DC analysis. The DC voltage supply at the collector is set to a variable, VCE, which is initialized in the VAR block. The VAR block also initializes the variable, IBB, used in the DC current source at the base of the BJT. The actual values used for VCE are determined in the DC simulation controller (DC1). In this example, VCE is swept from 0V to 6V, so that the model can be verified over a relatively wide operating range. The DC controller can only sweep a single variable, so the values for IBB are swept using the ParamSweep component. The range chosen for the base current, IBB, is set to 50uA to 350uA. ***This IV characteristics simulation setup is available as a default template in ADS and designers can obtain the same under Schematic page by selecting: Insert->Template->BJT Curve Tracer, it can be used after setting IBB and VCE values as desired by designers.***

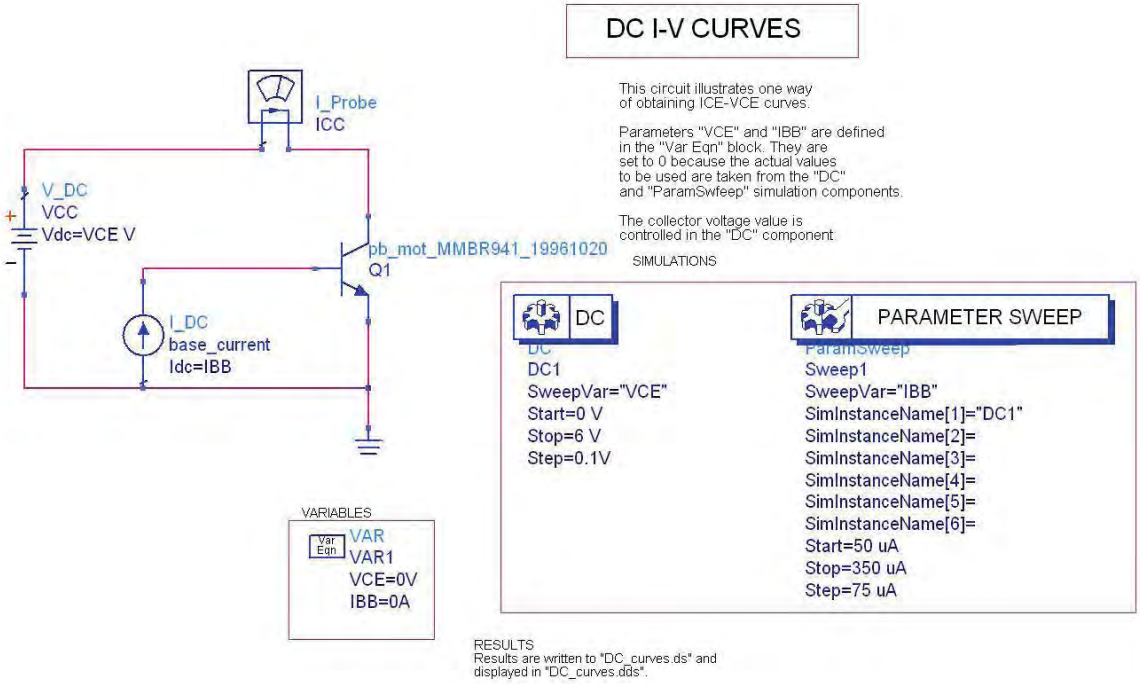


Figure 1. Transistor Swept-Parameter DC Analysis Setup

Results from this simulation are displayed in “DC_curves.dds”. The available output variables can be viewed by either placing a new plot or selecting the existing plot for edit, which open the Insert Plot dialog window shown in Figure 2. Notice that voltages at each of the named nodes are automatically supplied, as is the current at the DC supply (VCC.i).

The data from the current probe, ICC.i, is redundant in this case. The numbered nodes are used to store information for DC back annotation, discussed in the section on Device Model RF Verification (page 6).

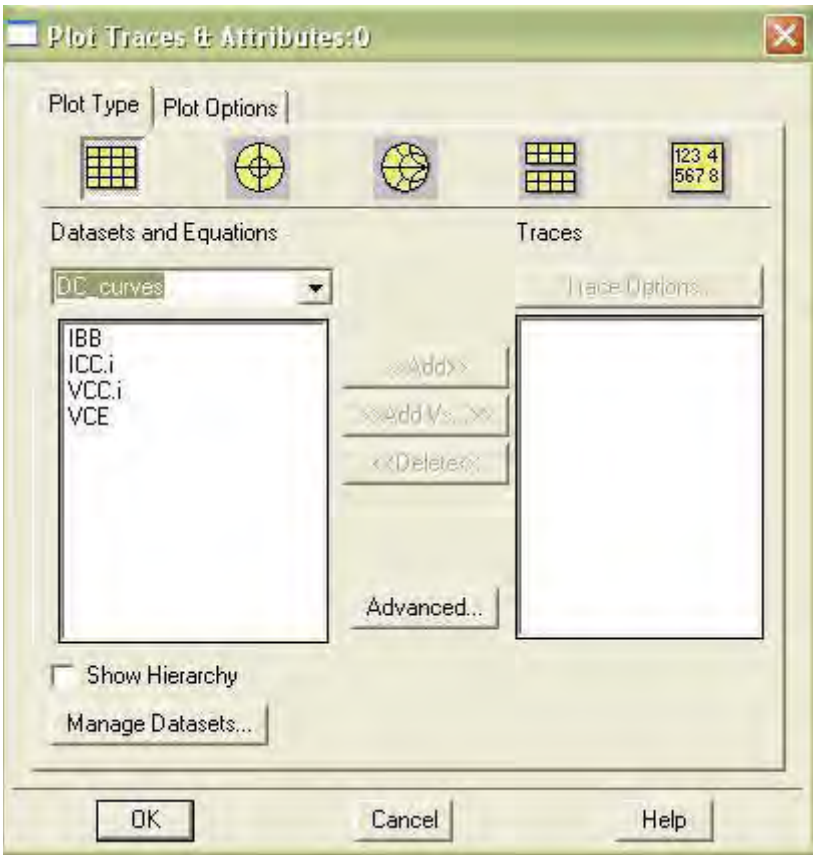


Figure 2. Insert Plot Dialog Box

Figure 3 shows there is good agreement between simulated and measured results. Measured data may be read in to ADS from either data files or instruments by selecting Window>New File/Instrument Server. ADS will convert files in Touchstone, MDIF, Citifile or ICCAP formats to ADS datasets, which can then be displayed alongside simulated results. The I-V curves clearly show that, at the specified operating point of VCE=1V, ICE<0.6mA, the device will be operating in a low current regime. If designers do not have measure datafile, this step can be omitted.

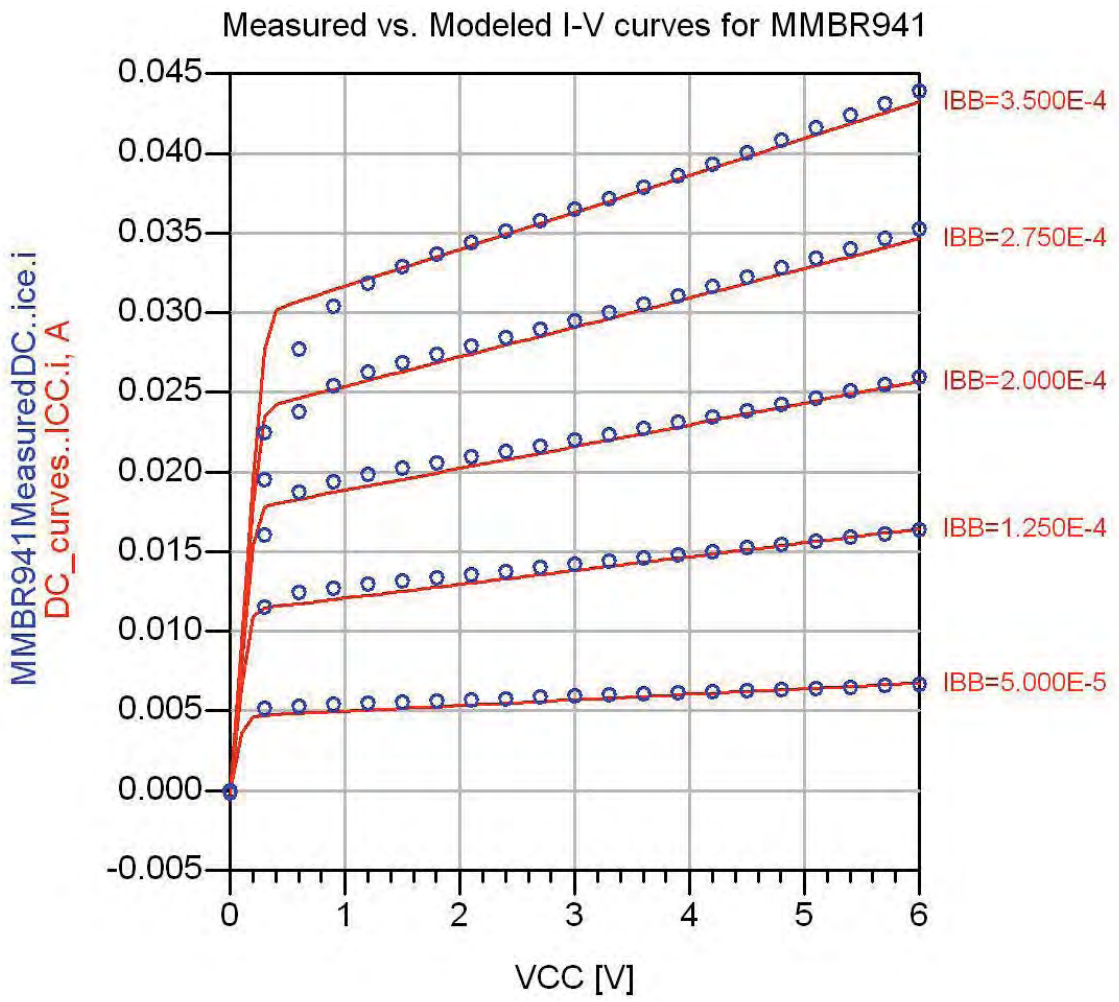


Figure 3. Comparison of Measured (symbols) and Simulated (Solid line) DC I-V Curves for MMBR941

Bias Network Design (Cell: BiasPoint)

The next step, selecting the device operating point and calculating the required bias resistors, is done using the set-up in BiasPoint.dsn as shown in Figure 4. Since the collector voltage and current have been specified, only the base current needs to be determined. In the schematic, VCC is fixed at 1V and IBB is swept from 1uA to 10uA, using the DC controller.

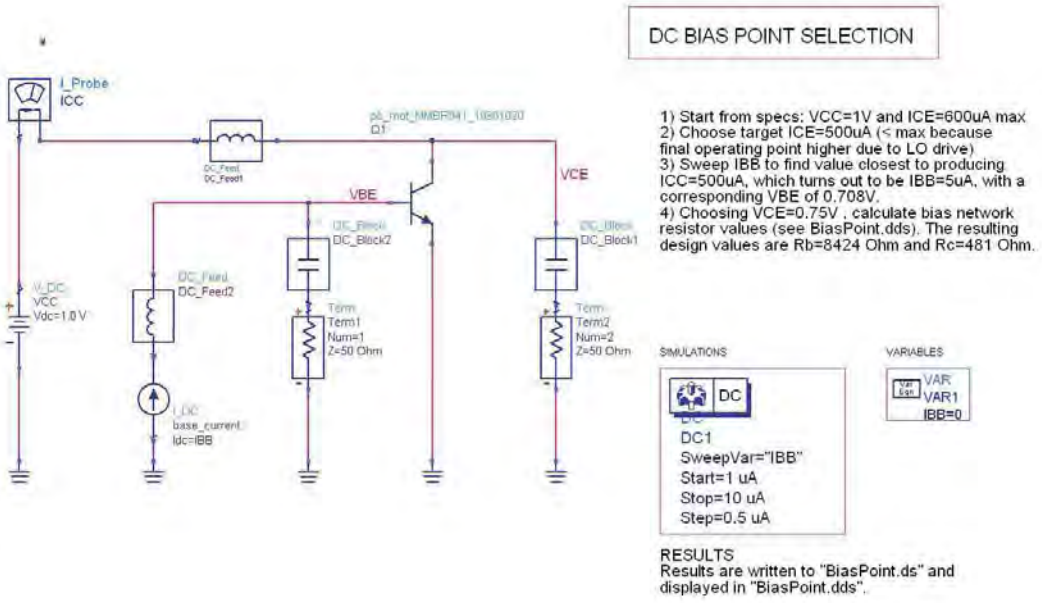


Figure 4. Calculation of Bias Point

The schematic contains bias tee components (the DC_Feed and DC_Block components) and 50 Ohm terminations that mimic the actual test setup used to measure the device. However, since the DC simulation does not include any RF signals, they are not necessary at this point, and can be omitted without changing the results. The results are displayed in tabular format in BiasPoint.dds (see Figure 5), so the appropriate base current can be selected. Note that the bias point current is actually lower than the specified final value. This is because the device will be pumped with a relatively large LO signal, causing a shift in the DC component of the collector current.

This shift will be calculated more precisely later on but, for now, IBB is selected to be 5uA so that the corresponding collector current (514uA) is well below the specification.

Table 1: ICE and VBE vs. IBB, VCC=1V

IBB	BiasPoint..ICC.i	BiasPoint..VBE
1.000E-6	102.7 uA	665.5 mV
1.500E-6	154.5 uA	676.2 mV
2.000E-6	206.3 uA	683.8 mV
2.500E-6	257.9 uA	689.6 mV
3.000E-6	309.4 uA	694.4 mV
3.500E-6	360.8 uA	698.5 mV
4.000E-6	412.2 uA	702.0 mV
4.500E-6	463.4 uA	705.1 mV
5.000E-6	514.6 uA	707.9 mV
5.500E-6	565.7 uA	710.4 mV
6.000E-6	616.8 uA	712.7 mV

Sweeping IBB shows we need IBB=5uA to have ICC~=500uA. The corresponding VBE is 0.708V.

Fig 5. Device Operating Point Selection

The bias resistor values, shown in Figure 6, are calculated next. Base current, collector current and VCC are known, but the designer must make an assumption about the voltage drop across Rc to be able to solve for Rc and Rb. In this case, a collector-emitter voltage of 0.75V is chosen, providing a reasonable working voltage at the output and realizable resistor values. The equations, written in the data display page, calculate the exact values required for each value of base current, but of course the nearest standard values must be chosen. The next step is to confirm bias operation using these standard values and then verify the S-parameters of the model against measured values.

Table 2: Calculated Rb and Rc

IBB	Rb	Rc
1.000E-6	84529.635	2410.638
1.500E-6	49209.429	1602.222
2.000E-6	33115.916	1200.472
2.500E-6	24143.233	960.191
3.000E-6	18520.552	800.304
3.500E-6	14716.285	686.232
4.000E-6	11998.583	600.741
4.500E-6	9976.677	534.280
5.000E-6	8424.296	481.125
5.500E-6	7202.032	437.642
6.000E-6	6219.680	401.408
6.500E-6	5416.501	370.749

Eqn Rb= (0.75-VBE)/IBB

Eqn Rc=(0.25)/(ICC.i+IBB)

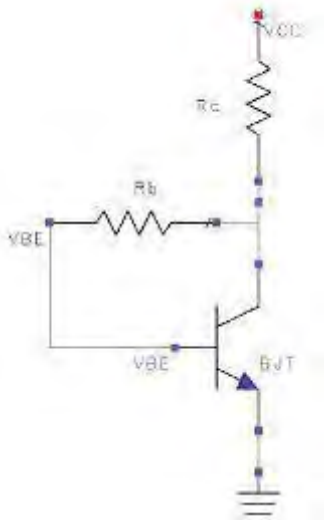


Figure 6. Calculation of Bias Network Resistors

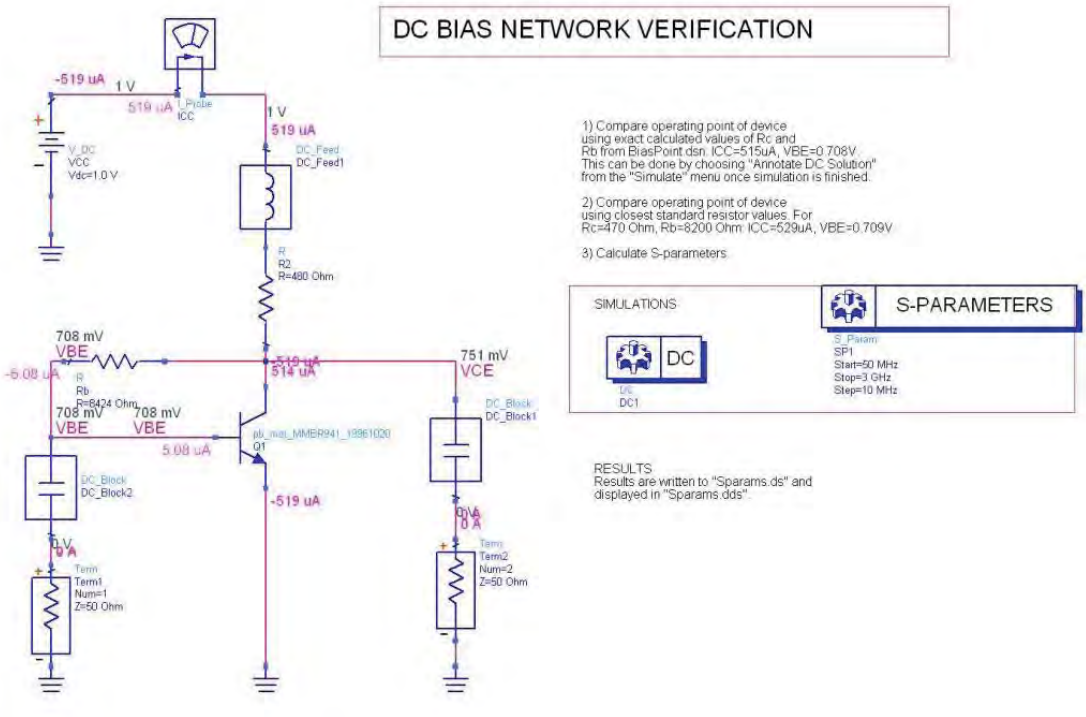


Figure 7. DC and S-Parameter Simulation Setup

Device Model RF Verification (Cell: BiasNet)

BiasNet.dsn, shown in Figure 7, includes both DC and S-parameter simulations so, in this case, bias tee components (DC feeds and blocks) are required to ensure proper RF performance. DC results are displayed directly on the schematic page, using the DC back annotation feature: once the simulation has been run, select Simulate>Annotate DC Solution to see the DC voltages and currents at each node. This simulation can be done with both the exact resistor values and nearest standard values (Rc=470 Ohm, Rb=8.2 kOhm) to confirm that the operating point is correct.

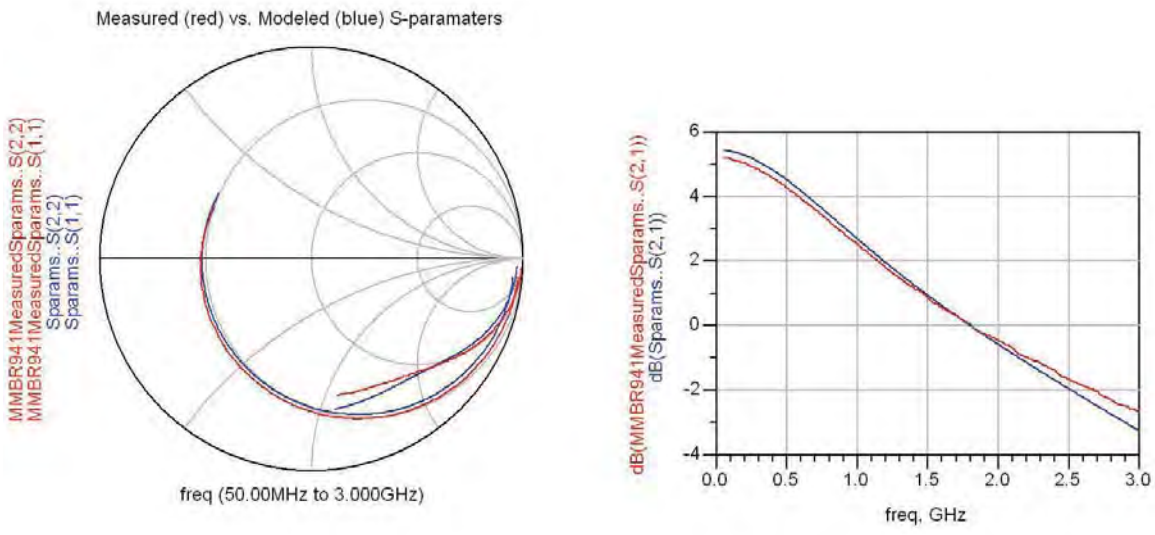


Figure 8. Comparison of Measured and Simulated S-Parameters for MMBR941

The device S-parameters are calculated at this operating point and displayed, together with measured data, in Figure 8. The good agreement obtained here verifies the small-signal RF performance. The device compression point will be simulated next to confirm large-signal operation.

Device Model Large-Signal Verification (Cell: Compression)

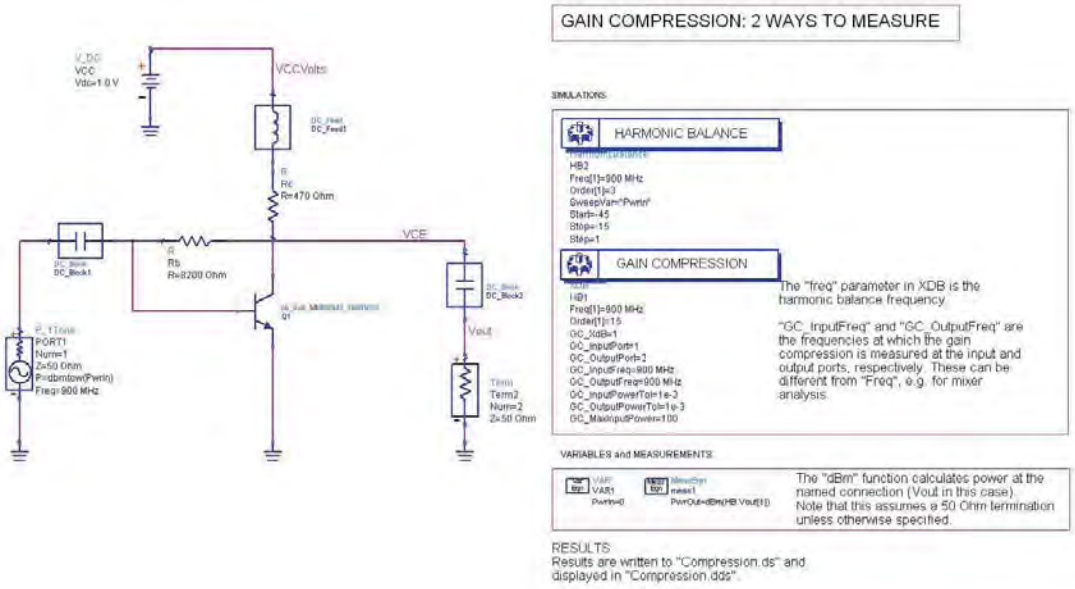


Figure 9. Device Compression Measurement Setup

Compression.dsn (Figure 9) shows two ways of calculating the device output compression at the RF frequency of 900 MHz. The conventional way, implemented here with the Harmonic Balance controller, is to sweep the input power level from low (i.e. small-signal) to high values until the output power compresses (the ratio Pout/Pin starts to fall off from its small-signal value). The input power variable, "PwrIn" is swept from -45 to -15dBm and a Measurement Equation component is used to define the output power at 900 MHz, in dBm. Notice that the dBm function assumes the power is being delivered to a 50 W load, unless otherwise specified by the user. The argument of the function, "HB.Vout[1]", specifies the fundamental frequency. Figure 10 shows the equation and graph used to determine the 1dB compression point, and includes the measured results as well.

The second method, unique to ADS, is more direct and does not require graphs or sweeping variables. The Gain Compression controller "XDB" performs a harmonic balance analysis that directly calculates and outputs the input and output power levels at the specified compression point. The default setting is 1dB, but the user can specify any amount of compression. Figure 10 also shows the output from this method: the input and output power levels at 1dB compression are listed in dBm.

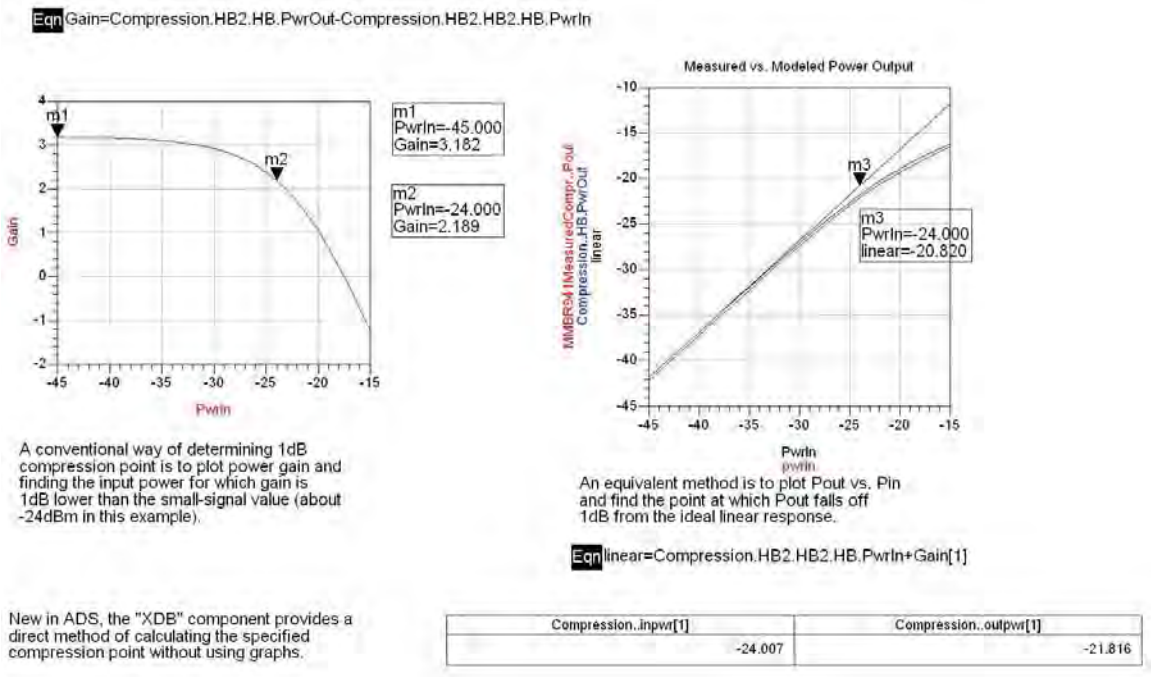


Figure 10. Two Methods of Determining 1dB Compression - both show input P1dB is -24 dBm

ADS offers a great deal of flexibility in where and how output data are defined. To take a simple example, "PwrOut" has been defined on the schematic page using a MeasEqn component, but it could equally well have been defined on the data display page as an equation. An advantage of defining outputs on the schematic is that they can be used in optimizations. On the other hand, defining them on the data display page is useful for setting up templates (where complex calculations can be easily applied to many different schematics). Also, any outputs that were overlooked before the simulation was run can be calculated afterwards by adding them on the data display page.

Notice that, at this point, the design still uses ideal bias tee components to isolate the DC and RF signal paths. These will be replaced with the real components that make up the matching networks in the next stage of the design.

Mixer Matching Circuit Design (Cell: RFIFmatch1)

An important step in mixer design is determining what impedances are seen at each port for both the RF and IF. The finished input network will match the device base to 50 W at the RF and present a short circuit at the IF (to prevent any noise at the input being amplified and interfering with the IF at the output). Similarly, the output network will match the collector to 50 W at the IF, while presenting a short circuit to the RF. Thus, for each frequency, the terminations seen at the input and output of the device are completely different. Since the device is not unilateral, the presence of a short circuit on one side of the device will affect the impedance seen at the other side for matching purposes.

The first step in designing the input matching network, then, is to determine the device input impedance at the RF when the output is terminated in a short circuit. For the output matching network, the designer needs to know the BJT's output impedance at the IF when the input is terminated in a short circuit. In ADS, equation-based 1-port Zparameter components are used to simulate this sort of idealized frequency-dependent termination, as seen in RFIFmatch1.dsn (see Figure 11).

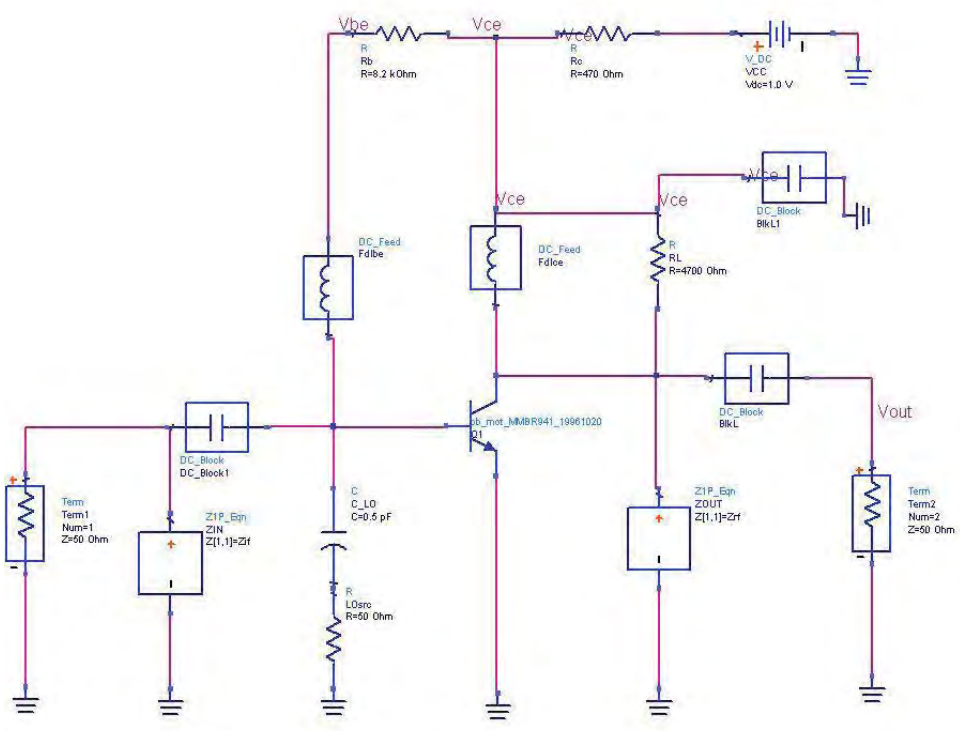


Figure 11. Calculating Device Impedance for Matching Network Design

The Z1P_Eqn components are defined in a VAR block. The one at the input, ZIN, is set to be a short-circuit at the IF and an open at the RF. This provides the required termination for S22 at the IF, while leaving S11 unperturbed at the RF. Similarly, ZOUT, at the output, is set to be a short at the RF and an open at the IF. Notice also that the LO source is represented at this point as an ideal 50 Ohm termination, coupled to the mixer through a 0.5pF capacitor. The capacitor was chosen to be so small in order to isolate the LO source from the RF input signal. The return loss looking back through the capacitor towards the LO source is only 0.33dB at RF, so that it almost appears like an open circuit to the incoming RF signal. The penalty is that the LO, which is close in frequency to the RF, is also isolated from the circuit, meaning that a higher LO drive level is required. For example, when the LO source is set at -10dBm, only -22dBm reaches the mixer.

The resulting S-parameters at the RF show that the input impedance is (11.5 - j51.4) Ohm with a short-circuit on the output. At the IF, the output impedance is (2065-j2010) Ohm. These values can be used to decide on matching network topologies and component values. The designer always has several topologies to choose from in developing a matching network, and which one is best will depend on factors such maximizing yield (some topologies are more sensitive to component variation than others), minimizing component count (to reduce cost) and combining functions where possible (incorporating the bias decoupling components into the matching, in this case).

To illustrate, Figure 12 shows that, starting at the device input impedance (A), a shunt inductor followed by a series inductor will move the circuit impedance successively from B1 to 50 W. The resulting network “A” has some advantages: the shunt inductor will 10 provide a short to the IF at the input, as required, and it can be used in the bias decoupling network (to replace the ideal DC_feed). However, network “B” is even better: using a smaller value of shunt inductance brings the impedance to B2, where a match is achieved using a series capacitor. C2 can also serve as the DC blocking capacitor, thereby saving a component, so this network is used for the mixer. ***ADS provides interactive Smith Chart tool utility which can be used for designing Matching Networks with lot of ease.***

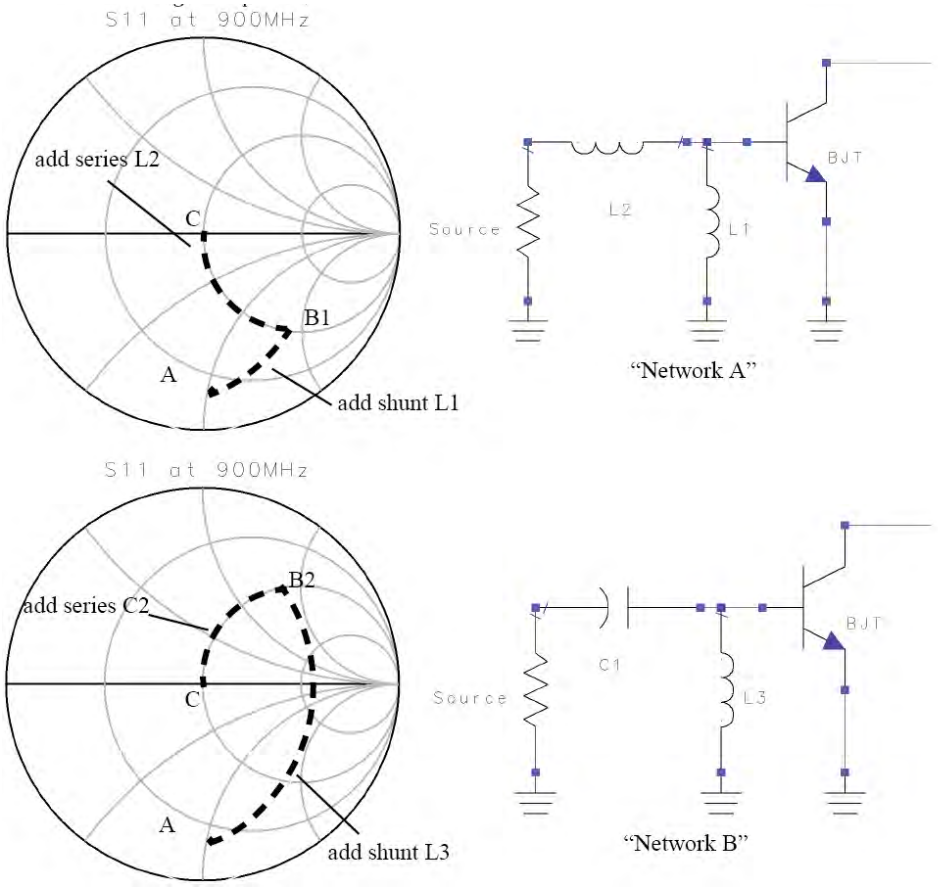


Figure 12. Choosing an Input Matching Network Topology

The output matching network was developed using a similar approach: starting from the Smith Chart, a matching network consisting of a shunt inductor followed by a series capacitor was designed. However, this topology would result in any RF at the output being dumped to the load instead of being short circuited as intended. To solve this, the shunt inductor (originally nearly 910nH, a very high impedance at RF) is replaced by an equivalent parallel LC combination. The capacitor must be large enough to provide a near-short for the RF, and a value of 33pF is chosen. The shunt inductor is then decreased, so the total reactance provided by the LC pair at the IF the same as that of the original inductor.

Although it was not done in this example, the actual component values for the network can be calculated using ADS, as illustrated in examples like */examples/MWCkts/ LNA_1GHz_prj*. In this case, components were calculated manually from the Smith Chart, and the resulting circuit is shown in LOdrive.dsn. The final matching networks are shown in Figure 13. Notice that, in addition to components for the matching and bias networks, a load resistor, RL has been added to control the mixer's conversion gain. The initial value of 4.7kOhm was chosen to be high enough not to have an effect on the mixer's performance, and will be adjusted as required once the conversion gain is known. Also, two large RF bypass capacitors (BlkL1 and BlkL2) are added to provide RF ground to the output load resistor and inductor and to the input shunt inductor, respectively.

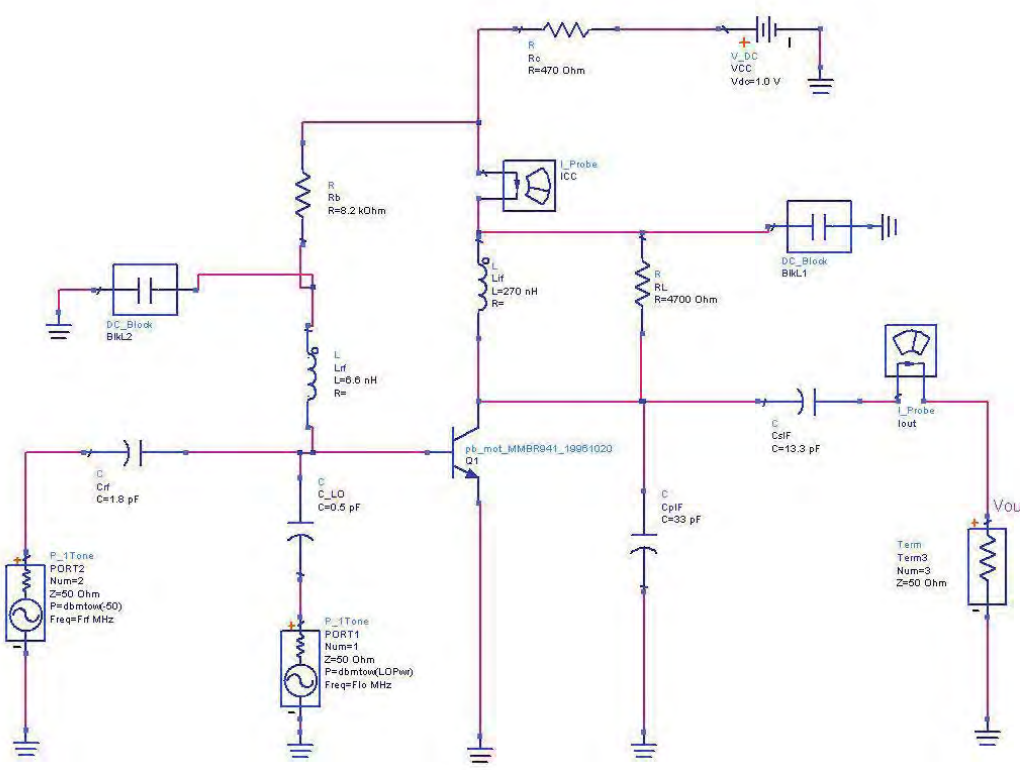


Figure 13. Mixer Matching Networks

Mixer Conversion Gain versus LO Drive Level (LOdrive.dsn)

LOdrive.dsn (Figure 14) shows how to simulate conversion gain for the mixer and how to determine the effect of LO drive level on gain and DC bias. The RF and LO frequencies and the LO power level have been defined as variables. The RF drive level is specified at -50dBm, while the harmonic balance controller is set up to sweep the LO drive level from -30m to -5dBm. (The controller has many parameters, and the user can control which are visible on the schematic by editing the component and choosing the "Display" page in the edit dialog window). A simulation measurement equation defines the output power, in dBm, at the IF. Defining it here instead of the data display page makes it possible to optimize for output IF power, if needed. The "mix" function will return the component of the Vout spectrum defined by {-1, 1}, meaning {-Freq[1]+Freq[2]} or -LO+RF= IF (45MHz).

The P_IF equation calculates the dBm value of the mix function.

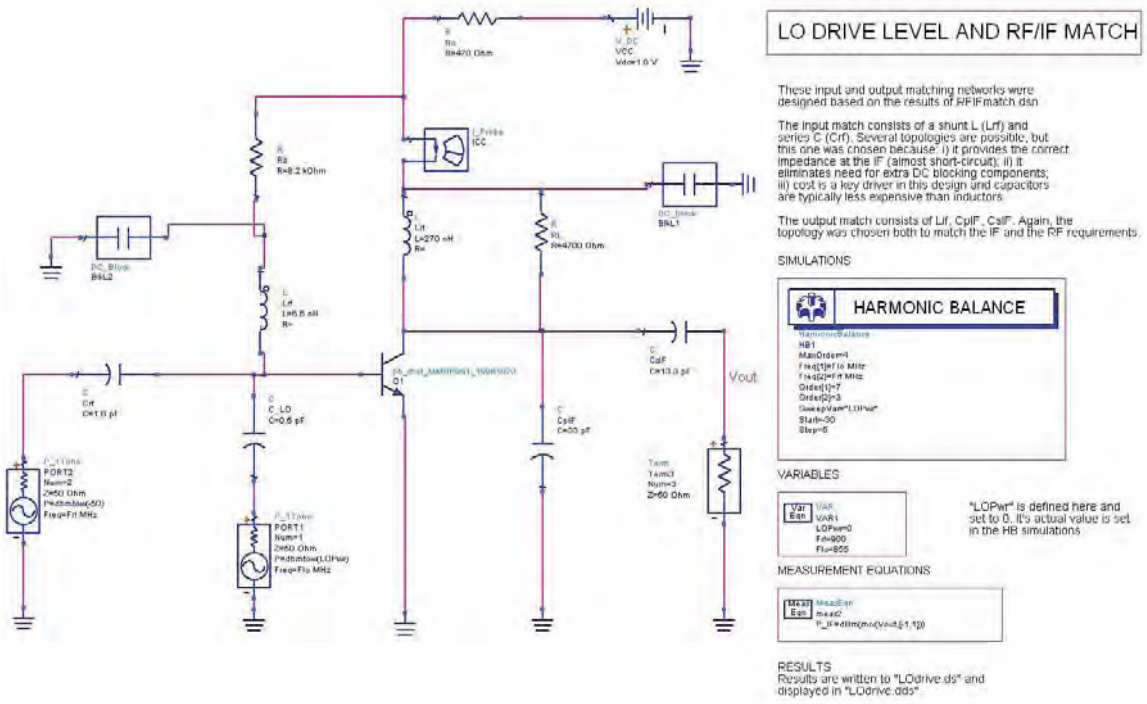


Figure 14. Set-up for Swept LO Drive Level Mixer Simulation

The data display shows the effect of the load resistor (Figure 15). Since the conversion gain is the difference between P_IF and the RF, and the RF power is fixed at -50dBm, the conversion gain can be calculated with a simple expression. Note that the default dataset, LODrive, contains results for a 4.7kOhm load resistor, and the conversion gain for this simulation is calculated by the equation "ConvGain". The conversion gain for a -10dBm LO drive is 17dB, which is unacceptably high. A second simulation was run with the load resistor reduced 1.5kOhm, which creates a lossy mismatch on the output. The results for that simulation were output to dataset LOdrive15, and equation "ConvGain_Rl5kOhm" shows the conversion gain is reduced to 13.7dB. This is still higher than the specification of 10dB, but will be left at this value for now since conversion gain can be expected to decrease further when non-ideal surface mount components replace the ideal components.

The second graph in the data display shown in Figure 15 illustrates the effect of the LO drive level on DC bias. Increasing the LO signal at the base drives the output swing on the collector harder, shifting the DC component higher (see Figure 16). In practice, a 5 to 15 percent shift in collector bias current typically gives good performance for a mixer of this type.

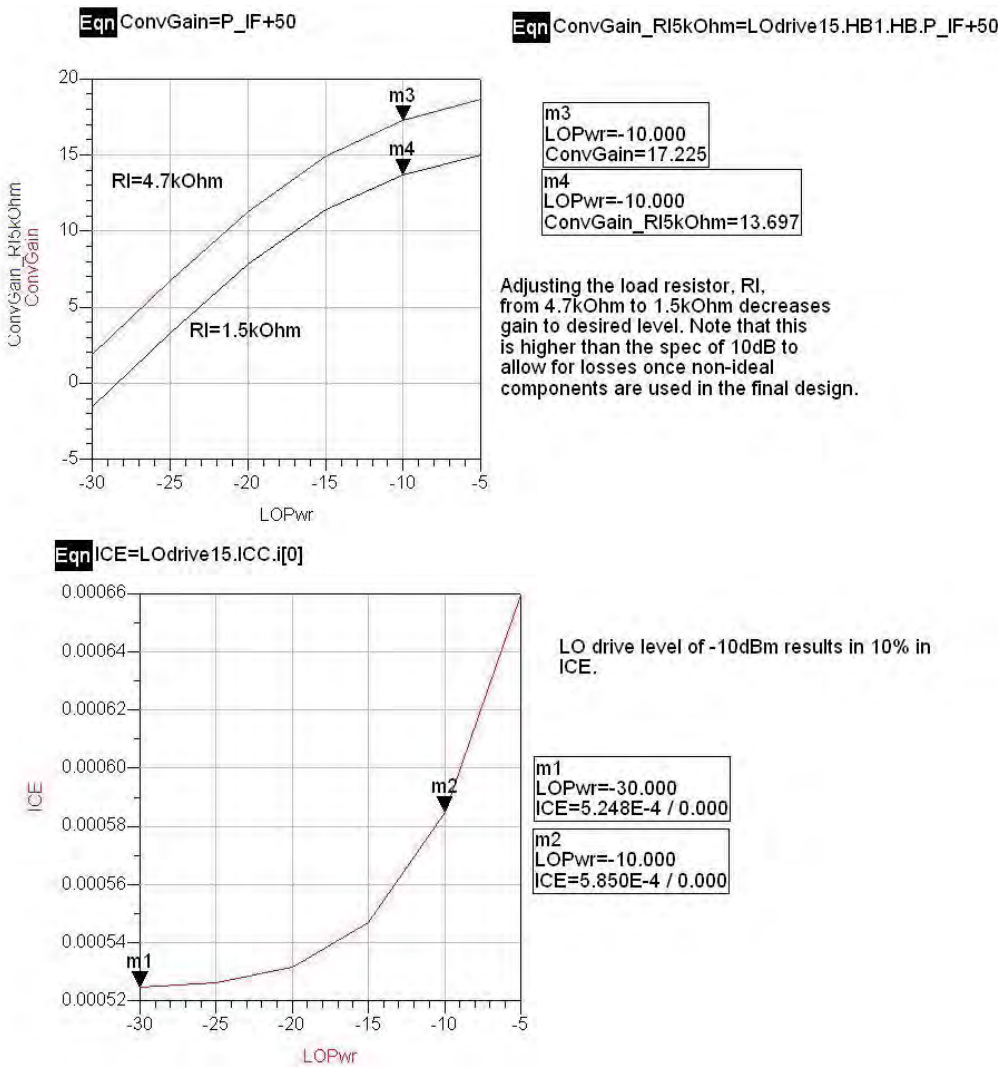


Figure 15. Conversion Gain and Bias Current Vary with LO Drive Level

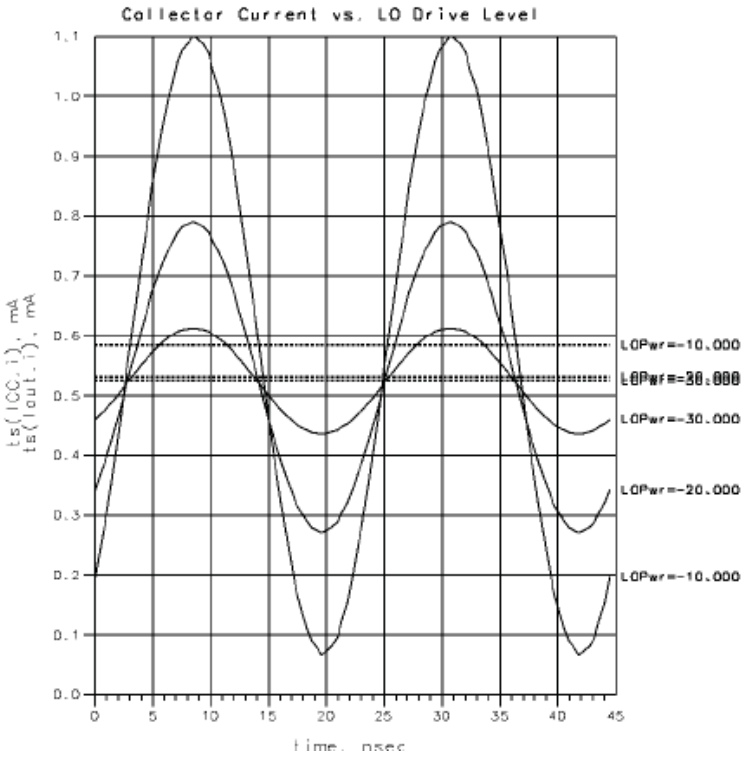


Figure 16. Variation in Output Collector Current with LO Drive Level

Mixer Conversion Gain versus RF Signal Level (Cell: MixCompr)

The set-up for measuring mixer compression used in MixCompr.dsn is very similar to LOdrive.dsn except that the LO power level is now held constant at -10dBm, while the RF power is swept from -50dBm to 0dBm. As the results in Figure 17 show, the mixer's conversion gain reaches 1dB compression at an input signal level of -27dBm.

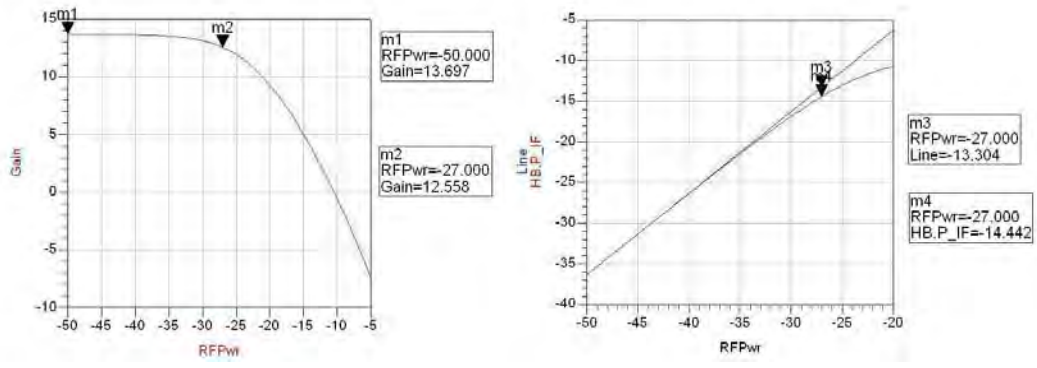


Figure 17. Mixer Conversion Gain Compression

Now that the mixer's performance is verified, the next step is to replace the ideal passive components with realistic models of the surface-mount resistors, capacitors and inductors that will be used in the actual circuit.

Creating the Mixer Layout (Cell: MixerLayout)

The design file MixerLayout.dsn contains a layout as well as a schematic. There are many possible ways to create layouts, and the best method will depend on the application. In this example, the first step was to convert all the components in the schematic to their nearest equivalent SMT part from the Passive Component Library. Next, these parts were placed in the layout window in their approximate locations. Interconnects were made in the layout window using the Trace command or microstrip components, and the final positioning of the components was adjusted. Finally, the schematic was updated using the design synchronization function.

MixerLayout.dsn was created by saving MixCompr.dsn under a new name and modifying it. Since the finished circuit will be simulated using the layout representation, it will have to be placed as a subnetwork in another schematic. This is because the layout file cannot contain simulator controllers, sources or terminations. The first step is to remove those components from the schematic and add ports to each point in the circuit that will be connected externally, either to sources, grounds or other circuits. The labels for each port will appear on the schematic symbol used when the design is placed in another schematic, so meaningful names should be provided. At this stage, the designer may also create a custom symbol for the circuit by selecting View>Create/Edit Schematic Symbol.

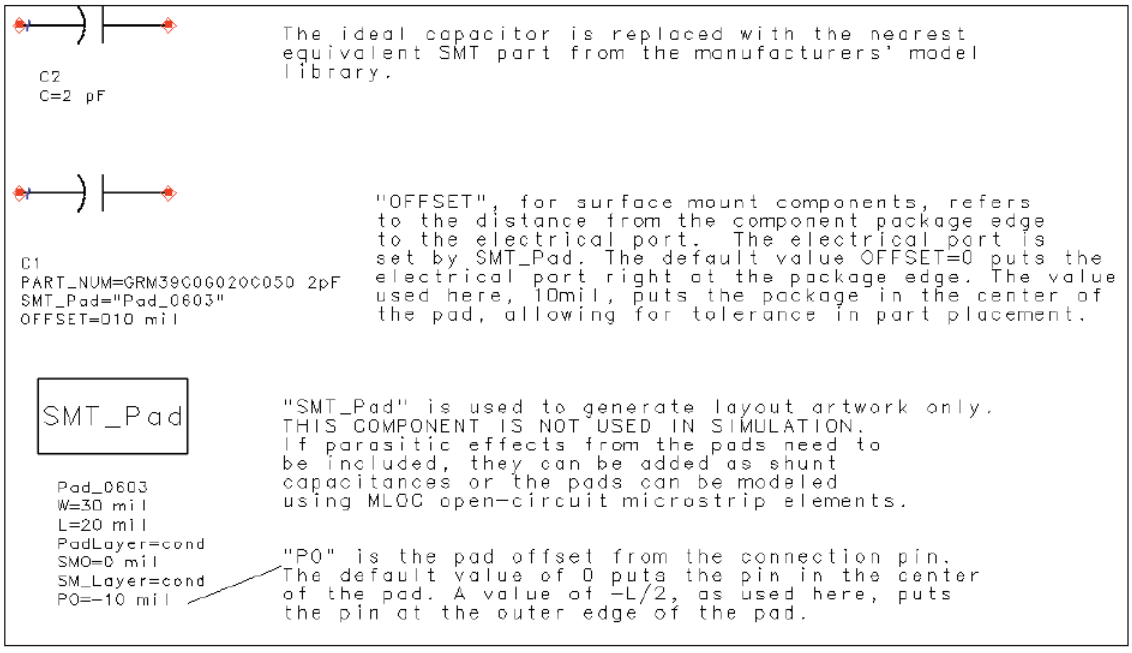


Figure 18. Substitution of SMT component for ideal component requires use of SMT_Pad

The next step is to replace each resistor, capacitor and inductor with a model of the SMT component that will be used in the actual circuit. The models are all found in the SMT Component Libraries by selecting the Browse and Search function in the Component Library List window. In this case, all the capacitors are MuRata Erie parts: the matching and bias capacitors are all MuRata Erie series GRM39 parts, while the RF bypass capacitors are GRM36 series. The resistors are taken from the Dale CRCW series and the inductors are Coilcraft parts. Where possible, parts are chosen to have a standard 0.060”x 0.030” footprint, although the inductors and RF bypass capacitors have different dimensions. Note that each SMT component specifies the name of the SMT_Pad component it uses. This SMT_Pad defines the pad-size to be used in layout, as shown in Figure 18. The designer must define these on the schematic page to ensure the pads appear correctly in the layout. Since each user will define the pads to suit their own board-fabrication process, the models do not include pad parasitics.

Once the components are placed and the pads defined, the designer can select Layout>Place Components from Schematic to Layout and place each part in its approximate location in the layout window. Traces are a convenient way to create the interconnects. They can be converted to equivalent microstrip components using the Edit>Path/Trace/Convert Traces command. In general, when moving back and forth between the schematic and layout representations, it is best to work on small sub-sections

and synchronize the two representations manually. Synchronization ensures that both layout and schematic describe the same circuit: for example, if the designer has made some changes to the layout, the schematic can be updated to reflect them by selecting Schematic>Generate/Update Schematic in the layout window. Changes made to the schematic can be similarly transferred to the layout by choosing Layout>Generate/Update Layout in the schematic window.

Figure 19 shows the finished layout. A ground-plane has been added to the top-side metallization to eliminate the need for vias, thus reducing fabrication costs. This can be easily created in ADS by drawing a rectangle the size of the final circuit board and using the Edit>Create Clearance feature to generate the required spacing around transmission lines and component footprints.

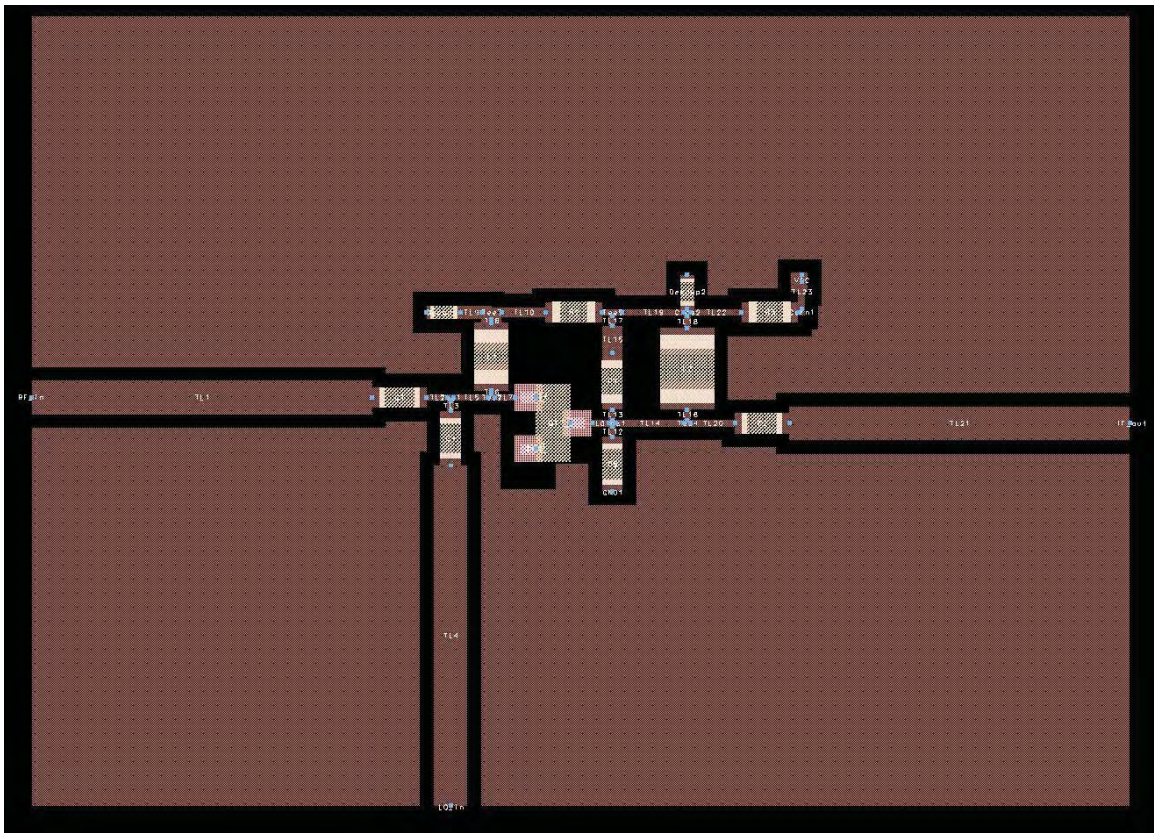


Figure 19. Finished Layout for Mixer Circuit

Finally, in this example the design will be simulated from layout, so the “SimLay” option is selected in the File>Design/Parameters dialog box. This allows the designer to see the effects of changes in the layout directly, without having to re-enter parameters in the schematic. Notice that components in the schematic can be modified (or even deleted entirely) without affecting the simulation, as long as the layout remains intact. Simulation from Layout (SimFromLayout.dsn)

SimFromLayout.dsn contains MixerLayout, together with the simulation controller, sources and terminations required to simulate it. The simulation setup is identical to the one used in LOdrive.dsn so the results using the non-ideal components may be compared directly. MixerLayout uses microstrip lines, so an “MSub” component is also included (Figure 20).

Figure 21 shows the mixer conversion gain as a function of LO drive level when simulated using both the ideal components and the SMT model components. As expected, the conversion gain has drops significantly, due mainly to the resistive losses in the inductors. This can be verified by replacing individual components with their ideal counterparts and re-simulating. The load resistor can now be adjusted to compensate for these losses:

changing Rl from 1.5kOhm to 3.3kOhm restores the simulated conversion gain to 10.76 dB, providing a 0.76dB margin over the specification. Note that these changes must be made in the layout file in order to be reflected in the simulation results. Once any such final corrections have been made to the layout, the circuit board is ready to be exported for fabrication.

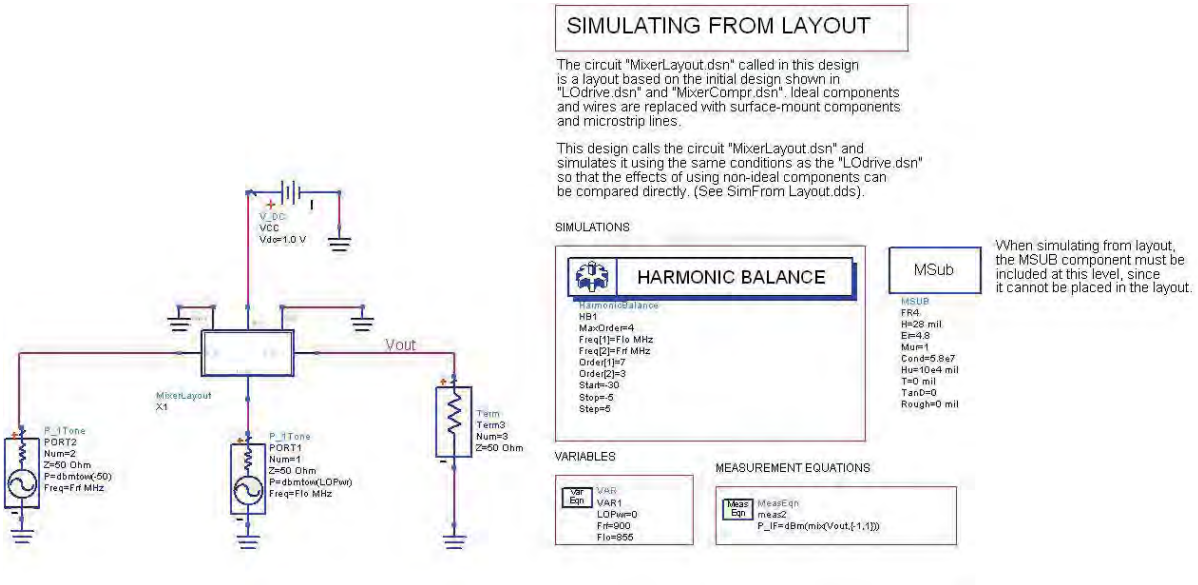


Figure 20. MixerLayout called as a sub-network in SimFromLayout.dsn

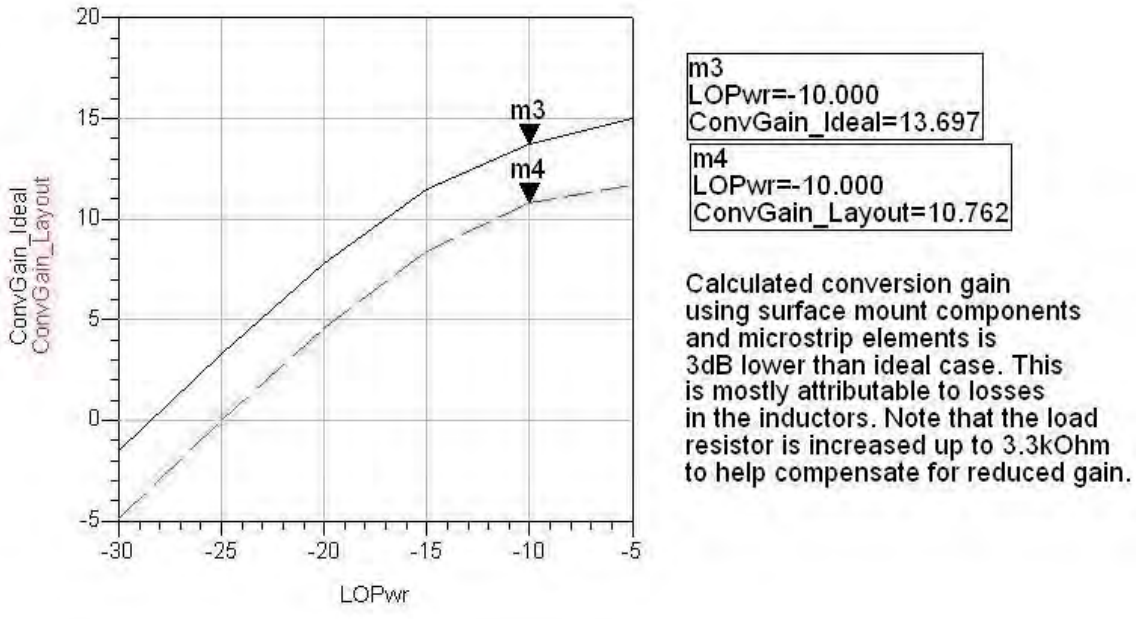


Figure 21. Comparison of Mixer Conversion Gain Using Ideal and SMT Components

Summary

An example of mixer design using Agilent ADS has been presented, including details of the design process and simulation set-ups. This example is included with Agilent ADS and can be readily copied and modified by users for their own projects.

Additional Information on Mixer Design:

Additional material and various Mixer design examples can be found at EEsof Knowledge Centre, designers using EEsof can register at:

http://www.agilent.com/find/eesof-knowledgecenter

Registered users can find additional technical notes and examples on Mixers by clicking on link:

https://edasupportweb.soco.agilent.com/portal/page?_pageid=36,39974&_dad=portal&_schema=PORTAL&lang=1&search=mixer&corner=1

Chapter 14: Microwave Oscillator Design (1 GHz VCO)

Included with due permission from original author J.P. Silver

Original Author: J.P. Silver, E-mail: john@rfic.co.uk

ADS Licenses Used:

1. **Linear**
2. **Harmonic Balance**

Chapter 14: Microwave Oscillator Design (1 GHz VCO)

Abstract

This paper discusses the design of a basic feedback oscillator, using a lumped element resonator with varactor control. A design center frequency of 1GHz has been chosen, with a tuning bandwidth of 50MHz (i.e. 10% or 5.5MHz/V) and a required phase noise performance of better than –70dBc/Hz at 10 KHz offset.

Introduction

This tutorial describes the design of a 1GHz feedback oscillator building on the theory from the oscillator basics tutorial. Throughout the design Agilent ADS circuits and simulations are given to verify each design stage and show the predicted performance.

Lumped Resonator Design

Normally simple two element resonators provide a zero phase shift while 4 element resonators such as the one shown in Figure 1 provide a 180-degree phase shift. The additional 180° phase shift in a microwave oscillator is usually provided by a length of transmission line used to complete the closed loop that is

$$\frac{c}{f} = \lambda_{air}$$

$$\therefore \text{Required transmission line length (180 degrees)} = \frac{\lambda_{air}}{2\sqrt{\varepsilon_r}}$$

where ε_r = the effective dielectric constant of the material.

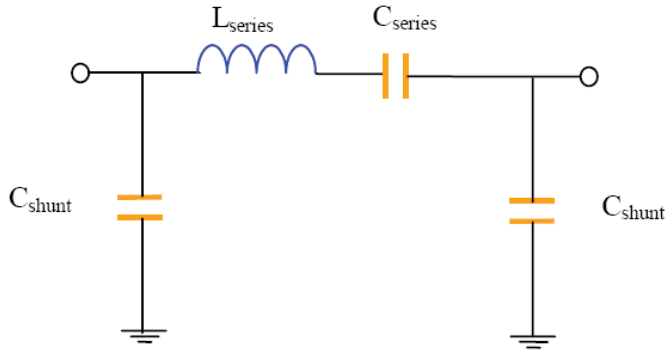


Fig 1. 4-Element lumped resonator. The L-C series elements determine the resonant frequency of the oscillator and hence the oscillating frequency.

The shunt capacitors are required to set the loaded Q of the resonator to at least 15 to ensure a compliant phase noise response.

.

Effective capacitance which resonates with the series inductor L_{series} is : -

$$C_e = \frac{1}{\frac{1}{C_{series}} + \frac{2C_{shunt}(\omega_o R_o)^2}{(\omega_o R_o C_{shunt})^2 + 1}}$$

R_o = input/output load resistance

Required inductance to resonate at f_o is given by : -

$$L_{series} = \frac{1}{\omega_o{}^2 C_e}$$

We can now calculate the circuit elements required to form the resonator using the equations above. If for ex-ample we require a phase noise of say –70dBc/Hz at 10KHz (using a narrow-band (~50MHz) VCO frequency of 1GHz) we can use the ADS simulation shown in Figure 2 to find out the Loaded Q we require

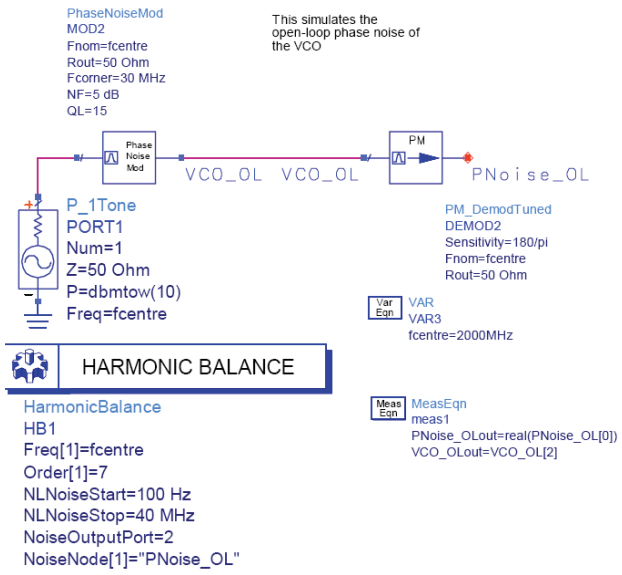


Fig 2. ADS simulation used to 'predict' phase noise performance given the resonator loaded Q, NF, Flicker corner frequency, centre frequency and output power.

From the resulting simulation shown in Figure 3 we can see we require a loaded Q of greater than 15 to ensure a phase noise of –70dBc/Hz at 10 KHz frequency offset.

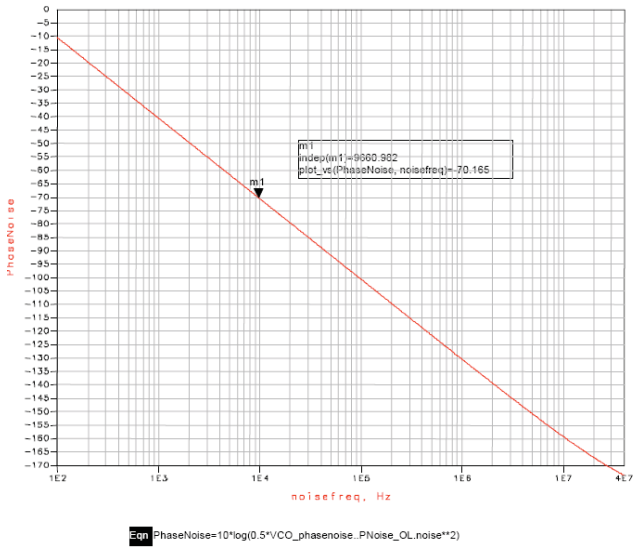


Fig 3. Resulting simulation from Figure 2 show-ing the resulting phase noise prediction with a marker set to 10KHz frequency offset and VCO loaded Q to 15.

If we assume an unloaded Q of 120 for the inductor, therefore the effective Q, Qe is given by : =

$$Q_e = \frac{1}{\frac{1}{Q_L} - \frac{1}{Q_U}} = \frac{1}{\frac{1}{15} - \frac{1}{120}} = 17$$

The required shunt reactance assuming an inductor value of 10nH gives $X_L = 2\pi f * 10^{-8} = 63\Omega$

$$X_{shunt} = R_o\left(\frac{2R_oQ_e}{X_L} - 1\right)^{-1/2}$$

$$= 50\left(\frac{2 * 50 * 17}{63} - 1\right)^{-1/2} = 9.8\Omega$$

$$C_{shunt} = \frac{1}{2\pi f X_{shunt}} = \frac{1}{2\pi * 1E^{9} * 9.8} = 16.2pF$$

Required inductance to resonate at f_o is given by : -

$$L_{series} = \frac{1}{\omega_o{}^2 C_e} \text{ therefore assuming}$$

$$L = 10nH \; C_e = \frac{1}{\omega_o{}^2 L} = 2.53pF$$

$$C_e = \frac{1}{\frac{1}{C_{series}} + \frac{2C_{shunt}(\omega_o R_o)^2}{(\omega_o R_o C_{shunt})^2 + 1}}$$ Re - arrange to get C_{series} ie

$$C_{series} = \frac{1}{\frac{1}{C_e} - \frac{2C_{shunt}(\omega_o R_o)^2}{(\omega_o R_o C_{shunt})^2 + 1}}$$

$$= \frac{1}{\frac{1}{2.53E^{-12}} - \frac{2 * 16.2E^{-12}(2\pi * 1E^{9} * 50)^2}{(2\pi * 1E^{9} * 50 * 16.2E^{-12})^2 + 1}} = 3.6pF$$

The calculated circuit element values for a 1GHz resonator Q ~ 16 are shown in the diagram Figure 4.

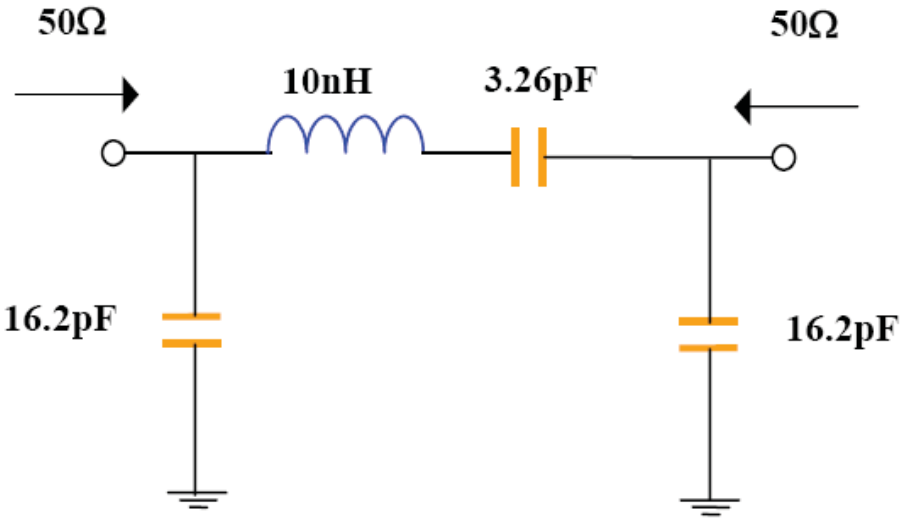


Fig 4. Final component values for the 4-element resonator designed to have a resonant frequency if 1GHz with a loaded Q of > 15 in a 50 ohm system.

Figure 5 shows the ADS simulation setup for verifying the feedback filter network. Note that a 180 degree phase shift has been inserted to simulate the phase shift of the feedback amplifier described later. The output plot of this simulation showing amplitude, phase, group delay and loaded Q is shown in Figure 6.

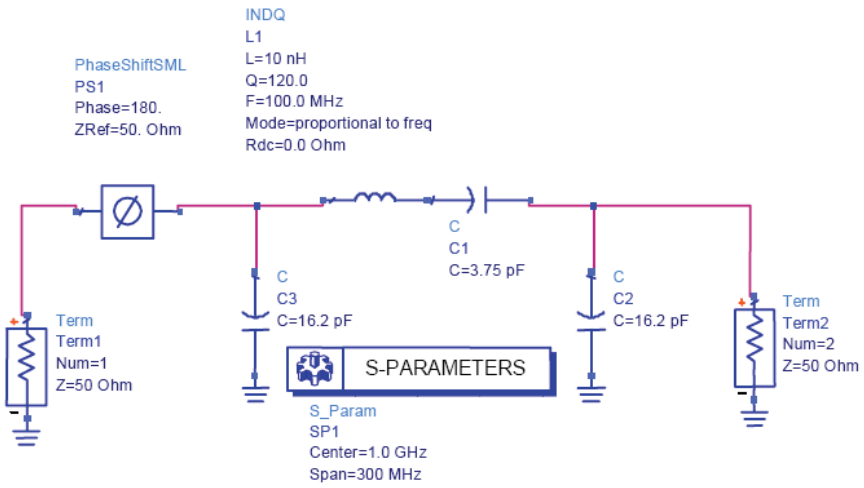


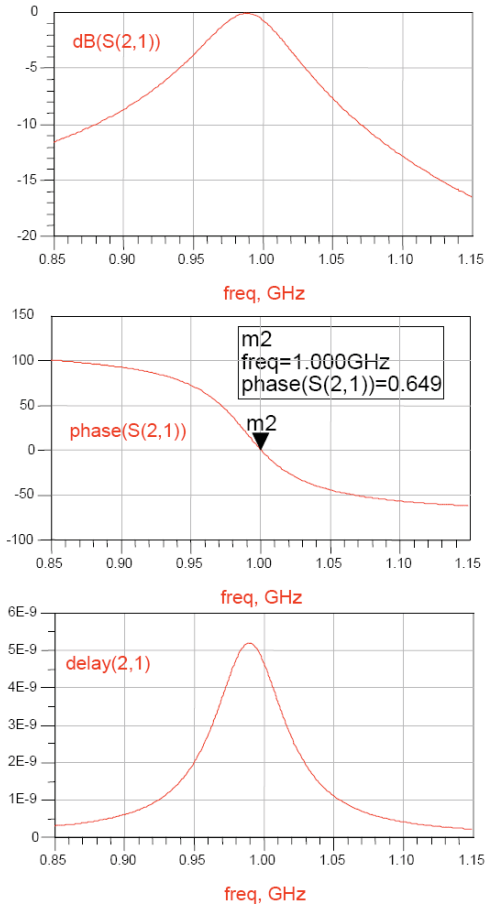
Fig 5. ADS S-parameter simulation for verifying the loaded Q of the feedback filter network.

The resonant frequency was slightly high so the series capacitor was increased from 3.26pF to 3.75pF. The measured Q from the plot was found to be ~16.2 (slightly off frequency – this can be adjusted later) i.e. within our specification. We now need what values of this capacitor we need (from a combination of the varactor and a varactor coupling capacitor) in order to give us our 50MHz tuning bandwidth. It is easier to find this value by simulation, rather than trying to work back through the earlier equations. Using simulation we find the capacitor value needs to vary from 3.4 to 4pF.

For this design the varactor chosen is the BB131 –

http://www.semiconductors.philips.com/acrobat/datasheets/BB131_3.pdf.

This has a capacitance of 11pF at 1V, 9pF at 4V and 3pF at 10V. To give us a capacitance swing of ~1pF we need to add a series coupling capacitor of 3pF. This will give us a combined capacitance of 2.25pF at a control voltage of 4V.



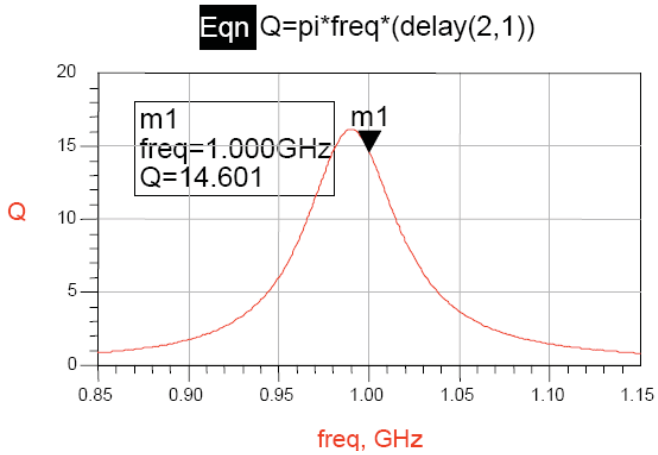


Fig 6. Simulation plot of the simulation of Figure 5, showing amplitude, phase, group delay and loaded Q. Loaded Q is > 15 slightly off frequency.

The data sheet of the varactor gives a series resistance (Rs) of 3 ohms at 470MHz. We can therefore calculate the unloaded Q of the varactor:

$$Q_U = \frac{1}{2\pi.f.Rs.Vcap}$$

Where

$Vcap = 6pF; Rs = 3\Omega$ &

$f = 470MHz.$

Therefore, $Q_U = 18.8$

To give us the correct resonant frequency another capacitor of 1p5 is connected in parallel with the varactor network as shown Figure 7. Note ADS will scale the Q factor of the diode when simulating at 1GHz even though the specified Q is at 470MHz.

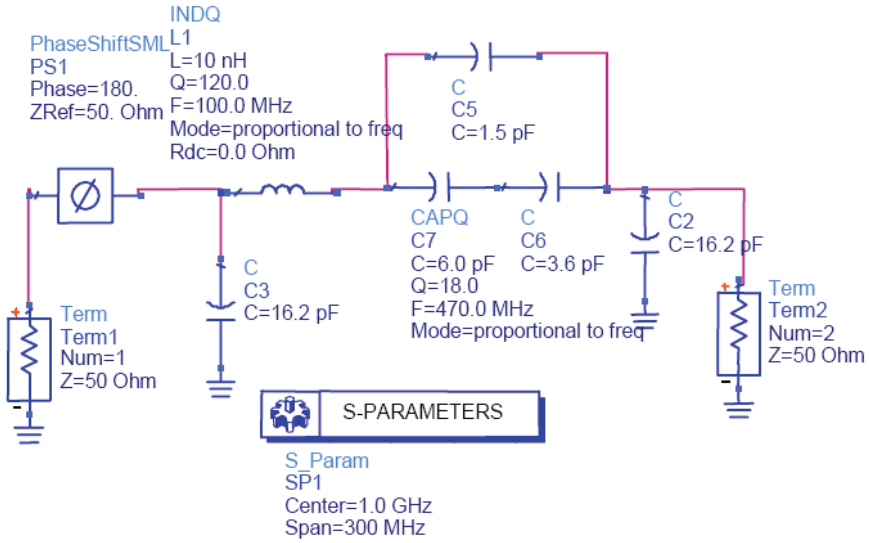


Fig 7. ADS simulation of the voltage controlled resonator. The varactor is given a Q of 18 at 470MHz although ADS will calculate the Q at 1GHz as part of the simulation.

The resulting Q plot of the above circuit is shown in Figure 8.

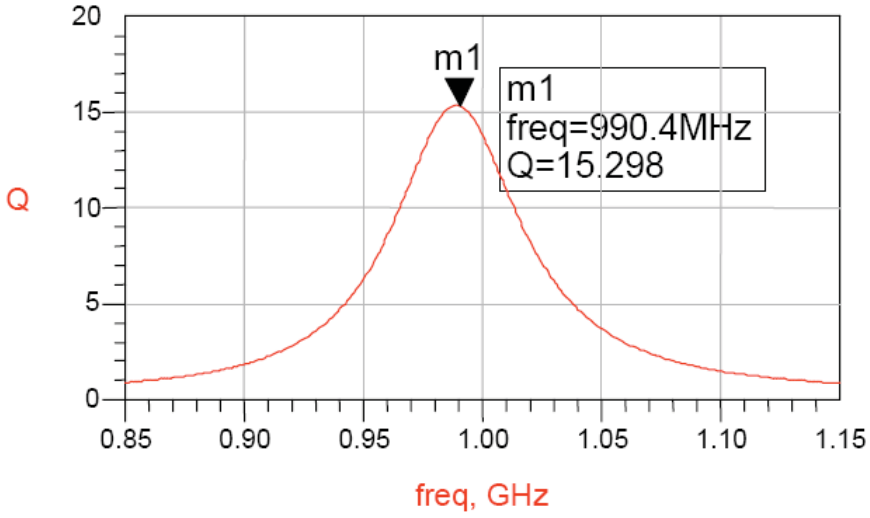


Fig 8. Q simulation plot with the varactor network and loaded Q of the varactor added to the simulation shown in Figure 7.

Feedback Amplifier Design

A suitable device to use as the feedback amplifier for this frequency is the Agilent AT-41486 - http://cp.literature.agilent.com/litweb/pdf/5968-2031E.pdf.

The data sheet shows that the unmatched gain at 1GHz is quite high and therefore there is a possibility of instability. The main way of determining the stability of a device is to calculate the Rollett's stability factor (K), which is calculated using a set of S-parameters for the device at the frequency of operation. The calculations are long winded and it is much quicker to simulate under ADS. To check the values of K, a simulation was run using the S-parameter model (8V at 10mA) with 50-ohm terminations. The ADS simulation for checking the stability factor (K) and maximum available gain (MAG) is shown in Figure 9. The tabulated results of the simulation are shown in Table 1.

Note For stability the Rollett's stability factor (K) must satisfy K > 1.

Clearly, in our un-matched simulation K<1 showing that the device is only conditionally stable and may oscillate (without the resonator!) under certain source/load conditions.

There are a number of ways of increasing K to be >1 which all result in reducing the MAG. In this example shunt feedback has been used to reduce the gain and increase stability with a view of making the amplifier unconditionally stable! However we still need to en-sure adequate gain margin is available as the resonator when designed using 'real' component models will be lossy.

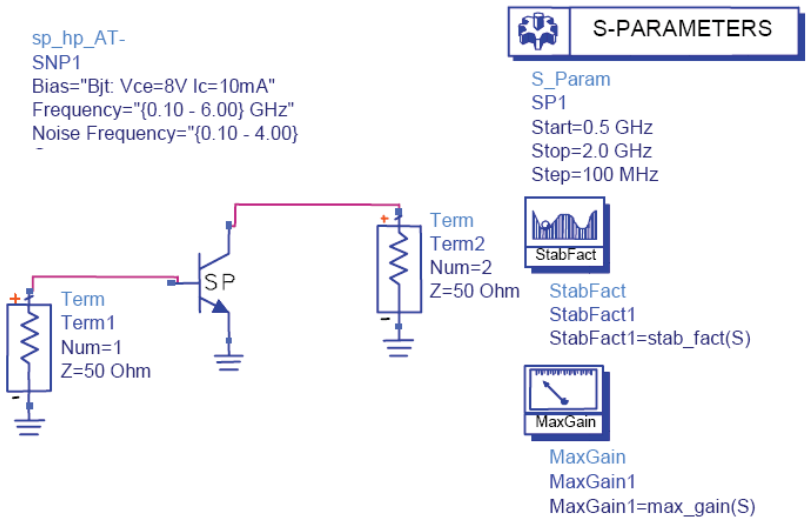


Fig 9. ADS simulation to determine the stability factor (K) and maximum available gain for the un-matched bipolar device.

freq	S(2,1)	StabFact1	MaxGain1
500.0MHz	12.630 / 1...	0.501	26.100
600.0MHz	11.488 / 1...	0.536	25.417
700.0MHz	10.346 / 9...	0.582	24.707
800.0MHz	9.204 / 93...	0.642	23.958
900.0MHz	8.062 / 88...	0.721	23.154
1.000GHz	6.920 / 84...	0.831	22.273
1.100GHz	6.480 / 81...	0.855	21.822
1.200GHz	6.040 / 78...	0.886	21.356
1.300GHz	5.600 / 75...	0.926	20.873
1.400GHz	5.160 / 72...	0.975	20.369
1.500GHz	4.720 / 69...	1.037	18.659
1.600GHz	4.498 / 66...	1.035	18.323
1.700GHz	4.276 / 63...	1.037	17.931
1.800GHz	4.054 / 61...	1.041	17.479
1.900GHz	3.832 / 58...	1.050	16.970
2.000GHz	3.610 / 56...	1.063	16.410

Table 1. Stability factor (K) and maximum gain simulated results from the ADS simulation shown in Figure 9. At 1GHz K = 0.831 with a maximum associated gain of 22dB.

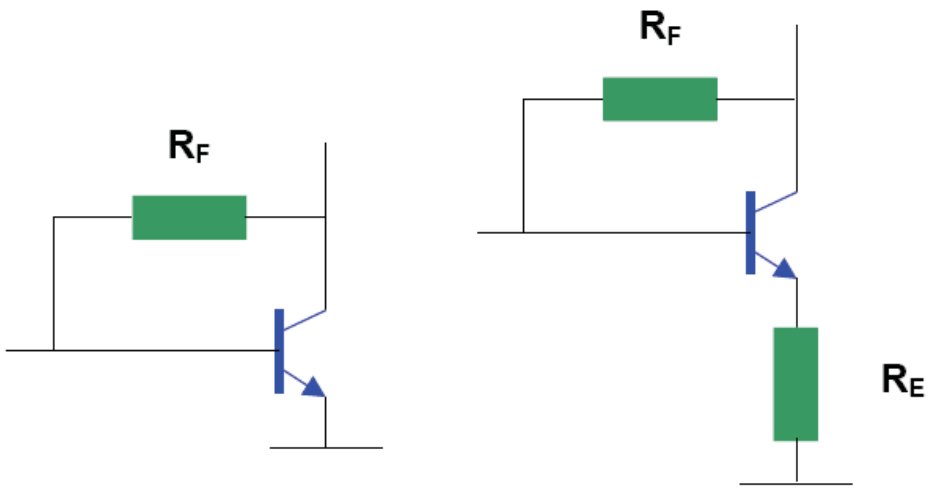


Fig 10. Topologies for broadband amplifiers, where feedback lowers gain but increases band-width.

The topologies for a broadband amplifier [1] using feed-back to lower the gain and increase stability are shown in Figure 10. The design equations for calculating the bias resistors are shown below:

$$S_{21} = \frac{Zo - R_F}{Zo} \text{ Rearrange to get } R_F$$

$$R_F = Zo(1 + S_{21})$$

$$gm' = \frac{gm}{1 + gm.R_E} = \frac{R_F}{Zo^2}$$

$$RE = \frac{Zo^2}{R_F} - \frac{1}{gm} = \frac{Zo^2}{R_F} - re$$

$$re = \frac{1}{gm} = \frac{V_T}{I_E} \quad \text{Where } V_T = 25mV$$

Design for a gain ($S21^2$) of 10dB

$$S21mag = 10^{\frac{10}{10}} = 10$$

$$R_F = Zo(1 + S_{21}) = 50\left(1 + \sqrt{10}\right) = 208\Omega$$

$$re = \frac{1}{gm} = \frac{V_T}{I_E} = \frac{25E^{-3}}{10E^{-3}} = 2.5 \quad \text{Where } V_T = 25mV$$

$$RE = \frac{Zo^2}{R_F} - \frac{1}{gm} = \frac{Zo^2}{R_F} - re = \frac{50^2}{208} - 2.5 = 9.5\Omega$$

The simulation for the small-signal feedback amplifier is shown in Figure 11, with the tabulated results shown in Table 2.

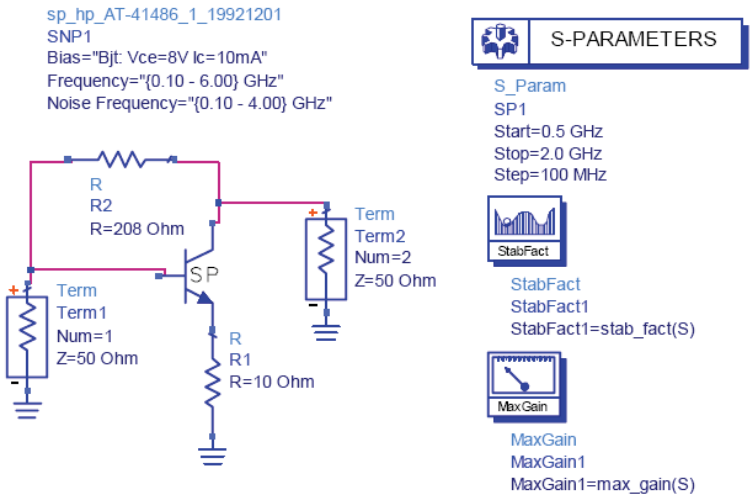


Fig 11. Small signal S-parameter simulation of the feedback amplifier circuit

freq	S(2,1)	StabFact1	MaxGain1
500.0MHz	2.909 / 158....	1.159	9.366
600.0MHz	2.922 / 155....	1.156	9.430
700.0MHz	2.934 / 152....	1.153	9.501
800.0MHz	2.943 / 148....	1.151	9.576
900.0MHz	2.941 / 143....	1.149	9.644
1.000GHz	2.917 / 137....	1.148	9.683
1.100GHz	2.934 / 133....	1.141	9.817
1.200GHz	2.947 / 129....	1.132	9.959
1.300GHz	2.951 / 125....	1.121	10.108
1.400GHz	2.941 / 120....	1.108	10.262
1.500GHz	2.910 / 115....	1.091	10.418
1.600GHz	2.927 / 111....	1.063	10.758

Table 2. Table of results for the feedback amplifier shown in Figure 11, showing the desired gain of 10dB and a unconditionally stable design with K>1.

The feedback amplifier was then simulated using a spice model with its associated bias circuit as shown in Figure 12. The 190 ohm resistor was designed to drop ~ 2V, so that ~ 10V is applied across the emitter-collector junction as per the data sheet. The base bias of R3 & R4 was set up to ensure that 10mA flows through the collector-emitter junction. To ensure that >10dB gain was achieved R2 was increased to 360 ohms. The resulting table of results is shown in Table 3.

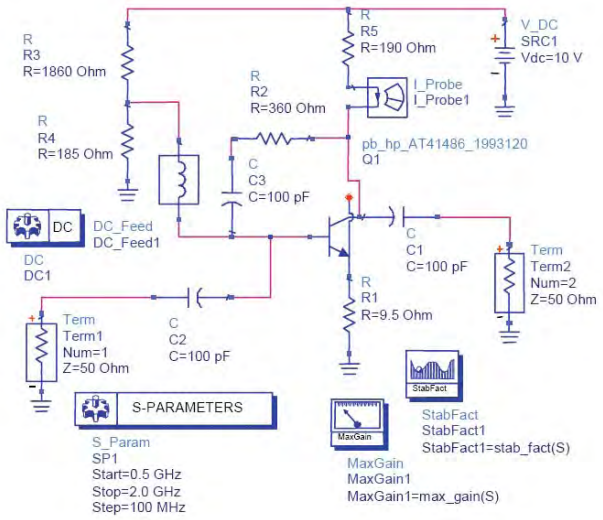


Fig 12. ADS simulation of the feed-back amplifier using a AT41486 spice model. The 190 ohm resistor is designed to drop ~ 2V so that ~ 10V is applied across the emitter-collector junction as per the data sheet. The base bias of R3 & R4 is set up to ensure that 10mA flows through the collector-emitter junction. To ensure that >10dB gain was achieved R2 was increased to 360 ohms.

freq	MaxGain1	S(2,1)	StabFact1
500.0MHz	10.922	3.301 / 153.173	1.304
600.0MHz	10.782	3.244 / 147.097	1.324
700.0MHz	10.627	3.180 / 141.287	1.344
800.0MHz	10.464	3.112 / 135.704	1.364
900.0MHz	10.293	3.040 / 130.327	1.383
1.000GHz	10.119	2.966 / 125.144	1.398
1.100GHz	9.944	2.891 / 120.143	1.410
1.200GHz	9.770	2.816 / 115.315	1.418
1.300GHz	9.599	2.742 / 110.652	1.420
1.400GHz	9.431	2.669 / 106.144	1.418
1.500GHz	9.269	2.598 / 101.782	1.411
1.600GHz	9.113	2.529 / 97.559	1.399
1.700GHz	8.965	2.462 / 93.464	1.383
1.800GHz	8.824	2.398 / 89.490	1.363
1.900GHz	8.692	2.337 / 85.627	1.341
2.000GHz	8.569	2.278 / 81.869	1.317

I_Probe1.i
10.29mA

Table 3. Results for the feedback amplifier shown in Figure 12. The table shows the desired gain of >10dB and an unconditionally stable design with K>1. The current probe confirms the designed Ic of 10mA.

Open Loop Analysis

With the feedback amplifier and resonator designed the whole circuit can be simulated to check that at center frequency the phase is zero with ~10dB of transmission gain.

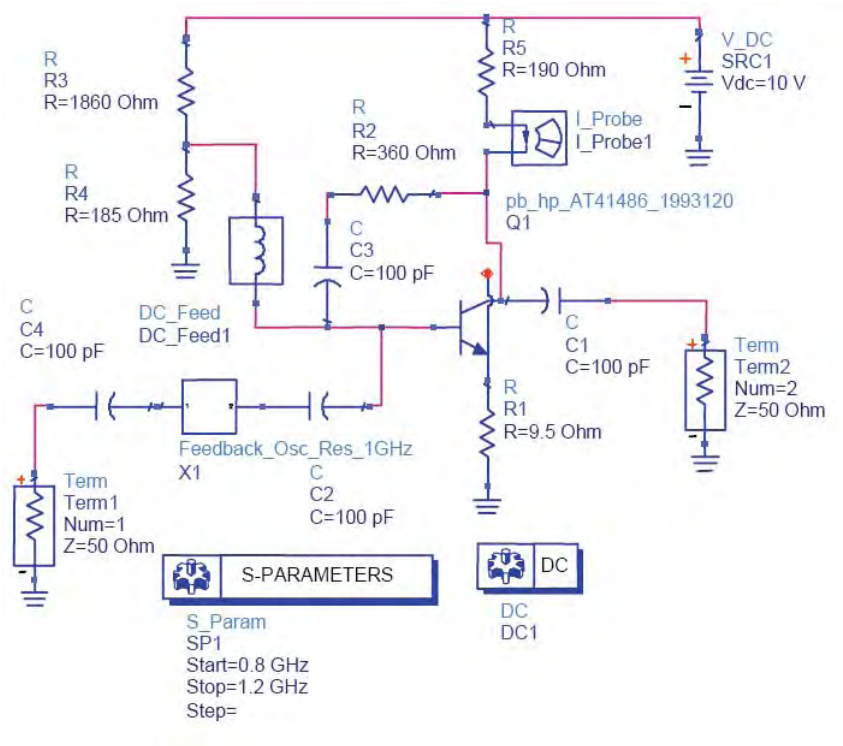


Fig 13. ADS open-loop simulation of the VCO, the sub-circuit of the resonator is shown Figure 14.

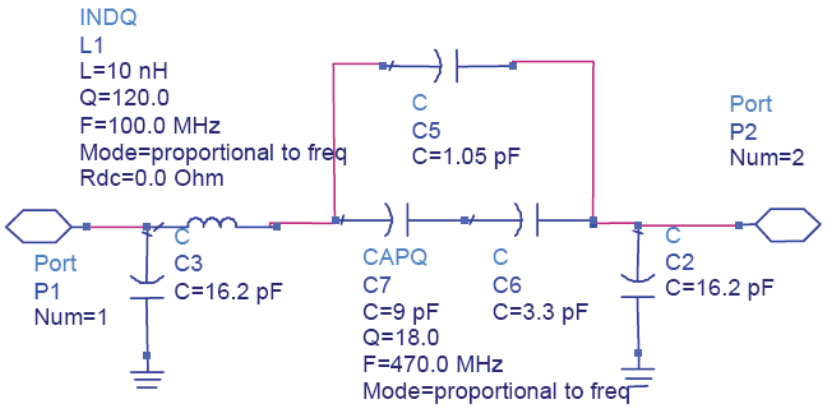


Figure 14 Sub-circuit showing the resonator section

The resulting simulation plot of magnitude and phase at 4V varactor control voltage is shown in

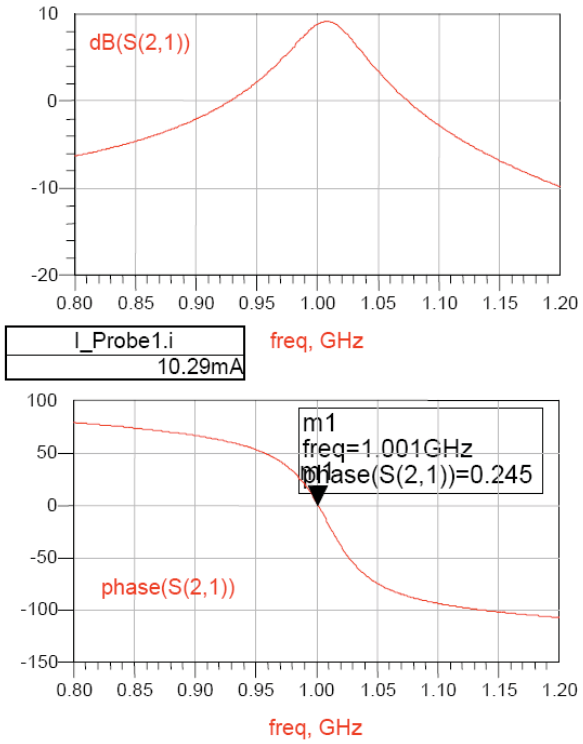


Fig 15. Results of the simulation shown in Figure 13. The insertion phase is zero degrees with a corresponding magnitude of ~ 10dB. Therefore, the circuit should oscillate at 1GHz.

Closed Loop Analysis

Small signal open-loop analysis is useful in checking that the resonator and amplifier are set at the correct frequency. However, when the loop is closed the amplifier will be forced into compression and as a result many of the RF parameters will alter including the oscillating frequency. Performing a Harmonic Balance simulation of the oscillator will allow us to determine the operating frequency, output power, phase noise and harmonic levels.

The Harmonic balance ADS simulation for this VCO is shown in Figure 16 with the resulting plots of phase noise, output RF spectrum and oscillating frequency in Figure 18.

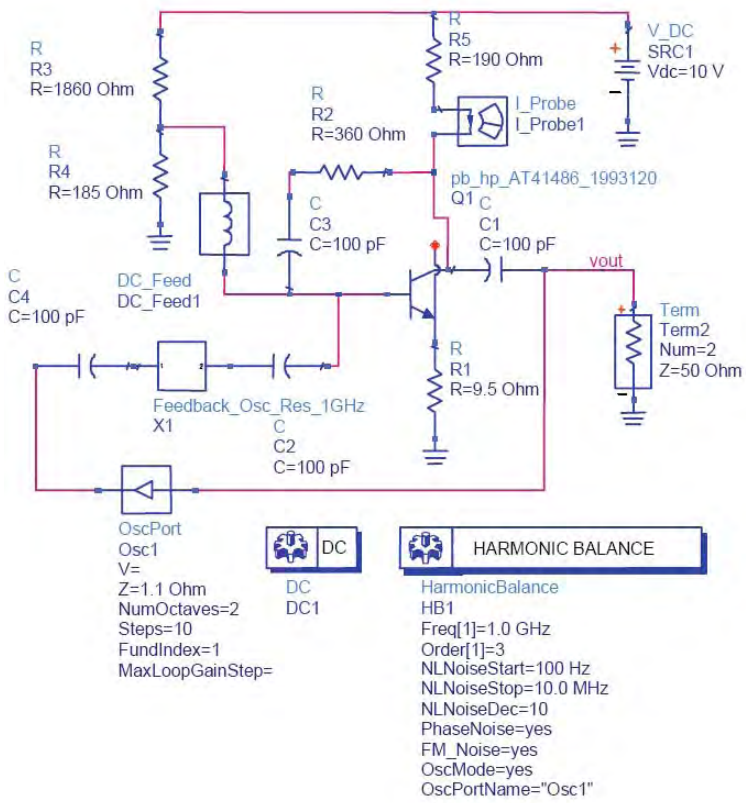


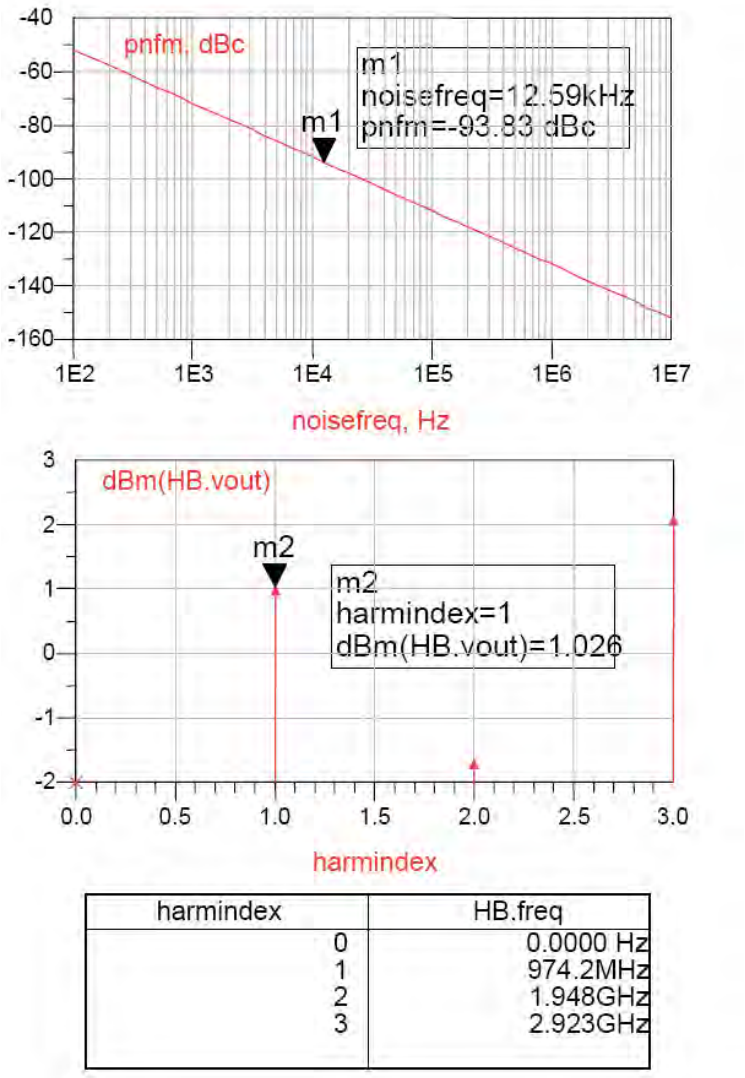
Fig 17. Harmonic balance large-signal closed-loop simulation of the VCO. Note the output port is given the node name 'vout' and must be entered in the harmonic balance setup on the 'noise(2)' section.

Note the frequency has shifted from that estimated in the open-loop simulations as a result large signal effects of the transistor. The resonator requires some 'tweaking' to bring it back on frequency and simulations performed at the maximum and minimum varactor control voltages to determined the simulated tuning bandwidth.

Altering the varactor values (after resetting the center frequency) shows that the tuning bandwidth is too wide at ~ 160MHz (see Table 4).

Control V	Vcap	Freq (MHz)
1	11pF	985
4	9pF	1000
10	3pF	1147

Table 4. First run tuning bandwidth of the VCO showing a value of ~ 160MHz.



harmindex	HB.freq
0	0.0000 Hz
1	974.2MHz
2	1.948GHz
3	2.923GHz

Fig 18. Resulting simulation plots from the HB circuit shown in Figure 17, showing the phase noise performance of –93dBc/Hz, with an output frequency of 974MHz and an associated output power of 1dBm. Note the frequency has shifted from that estimated in the open-loop simulations as a result large signal effects of the transistor. The resonator requires some 'tweaking' to bring it back on frequency.

In order to reduce the tuning bandwidth the coupling capacitor in series with the varactor diode needs to be reduced (it will be necessary to adjust the overall parallel capacitor to re-centre the VCO center frequency).

By altering the values of the capacitors shown in the resonator circuit of Figure 19 Modified resonator de-signed to give a narrower tuning bandwidth. This circuit has a tuning bandwidth of ~60MHz.

A summary of the simulated VCO frequency with varactor control voltage is shown in Table 5.

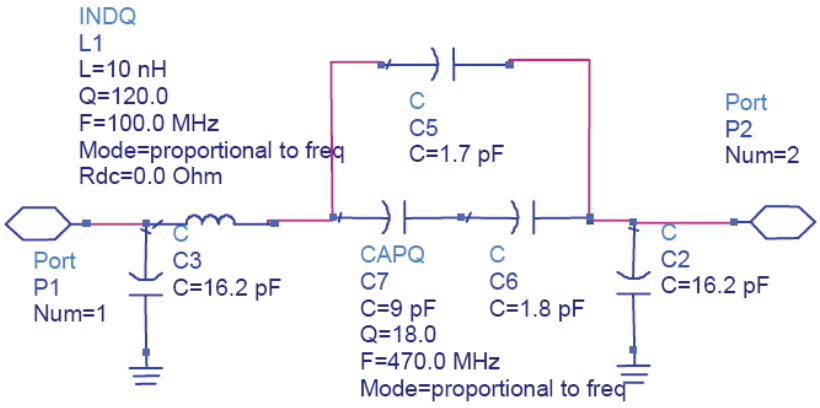


Fig 19. Modified resonator designed to give a nar-rower tuning bandwidth. This circuit has a tuning bandwidth of ~60MHz.

Control V	Vcap	Freq (MHz)
1	11pF	995
4	9pF	1002
10	3pF	1055

Table 5. Tuning range of the modified VCO with control voltage.

Simulations so far have shown that the Rf output power is quite low at ~ 0dBm. Examination of the circuit shows that at the moment we have large 100pF capacitors connected to the 50-ohm load. This will cause large loading of the loop resulting in a frequency shift and loss of power. Therefore, the 100pF capacitors were reduced from 100pF to 10pF, to lighten the coupling to the 50-ohm load.

The simulation result of the modified circuit is shown Figure 20. The VCO output power has now increased by almost 10dBm.

Table 6 shows the predicted summary of the VCO design.

Parameter	Result	Units
Centre Frequency	1000	MHz
Tuning bandwidth	62	MHz
Ko	6.8	MHz/V
Power	152	mW
Voltage	10	V
Phase Noise @ 10KHz	-106	dBc/Hz
Output Power	11.78	dBm

Table 6. Predicted Summary of the VCO design

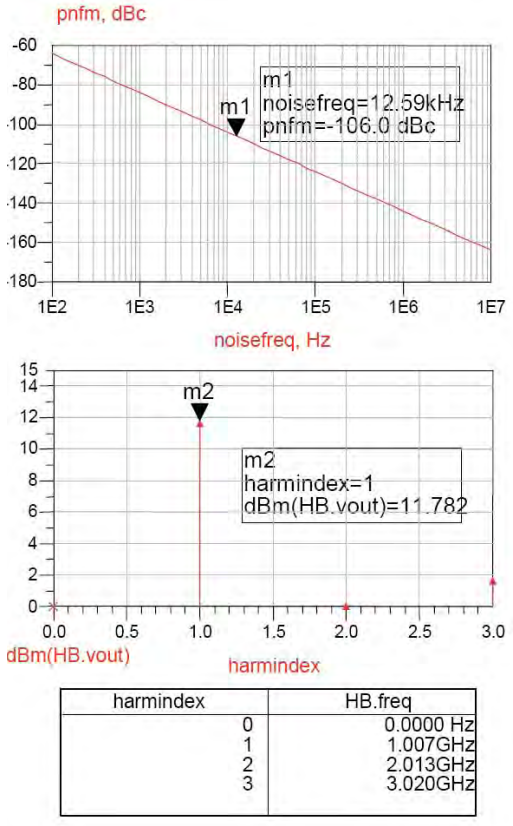


Fig 20. Simulation result of the modified VCO circuit with the coupling capacitors reduced from 100pF to 10pF. Also the parallel varactor capacitor was in-creased from 1.7pF to 1.95pF

Conclusion

This tutorial described the design of a simple voltage controlled oscillator using a lumped element filter as the feedback element. The design process began with a fixed resonator design, followed by the addition of the varactor and its associated padding network. With the resonator designed the amplifier section was designed using resistive shunt and series feedback to ensure a stable amplifier design with K>1 at 1GHz. The final stages of the design involved, open-loop small signal analysis, followed by closed-

loop large signal harmonic balance simulations. These harmonic balance simulations allowed the following parameters to be simulated i.e. phase noise performance, tuning bandwidth, Ko, out-put power and harmonic levels.

Additional Information on Oscillator Design:

Additional material and various oscillator examples can be found at EEsof Knowledge Centre, designers using EEsof can register at:

http://www.agilent.com/find/eesof-knowledgecenter

Registered users can find additional technical notes and examples on Oscillators by clicking on link:

https://edasupportweb.soco.agilent.com/portal/page?_pageid=36,39974&_dad=portal&_schema=PORTAL&lang=1&search=oscillator&corner=1

References

[1] Microwave Circuit Design, George D Vendelin, Anthony M Pavio, Ulrich L Rhode, Wiley-Interscience, 1990, ISBN 0-471-60276-0, Chapter 6

[2] Oscillator Design & Computer Simulation, Randell W Rhea, Noble Publishing, 1995, ISBN 1-884932-30-4, p36, p191 – p211.

[3] Fundamentals of RF Circuit Design (with Low Noise Oscillators), Jeremy Everard, Wiley Interscience, 2001, ISBN 0-471-49793-2, p156

Chapter 15: Power Amplifier Design

ADS Licenses Used:

1. **Linear**
2. **Harmonic Balance**
3. **Circuit Envelope**
4. **PTolemy**

Chapter 15: Power Amplifier Design

Power Amplifiers are inherent part of a transmitting chain which required to boost the signal to overcome channel losses between transmitter and receiver.

Power amplifiers are the prime consumers of the power in a transmitter hence during design stage designers need to look for the efficiency which is the figure of merit to know how efficiently DC power can be converted to RF power which is known as PAE (Power Added Efficiency). Also notice that efficiency translates either into lower operation costs e.g. Cellular Base Station or longer battery life e.g. Wireless handheld device such as Mobile Phone.

PA linearity is another important aspect of PA design so as to preserve the input and output power relationship to maintain the signal integrity. The design of PA often requires trade-off between linearity and efficiency.

There are many texts available for Power Amplifier Fundamentals, Classes of operation etc and this chapter mainly provides the guideline to design a RF power amplifier in a step by step manner to help RF designers to take up the PA design task rather easily by knowing all the key steps involved.

Power Amplifier Design Case Study:

Parameters	Specifications
Centre Frequency	1 GHz
Bandwidth	+/- 50 MHz
Output Power (PEP)	25 Watts
Gain	> 10 dB
Input/Return Loss	< -10 dB
PAE	> 50%
3rd Order IMD	< -30 dBc

Table 1: Power Amplifier Specification for Case Study

In this case study, we shall design PA for specifications as shown in the Table1 and use GaN (Gallium Nitride) based FET RF3931 from RFMD (www.rfmd.com). Designers can obtain transistor library of GaN components for ADS2011 (or later) by contact their local RFMD representatives.

Non-Linear Model for Power Amp Design:

Having a good non-linear model is essential for having a good start for PA designs. Designers should contact their respective device manufacturers to obtain good non-linear model for the device they are using in their designs.

There are various ways in which vendor can provide non-linear model to designers:

a. SPICE model: This can be easily imported into ADS
b. Non-Linear model card: Vendors provide device parameters for standard model cards such as Curtice Cubic, Statz, BSIM etc and these can be used directly in ADS
c. Design Kit: These kits contain the non-linear models for devices and these are usually encrypted to protect the IP.

In case of non-availability of a non-linear model there are few alternatives which manufacturers can give to designers such as:

a. **Optimum Zin and Zout over the frequency range:** Problem with this approach is that designers can only perform input and output matching network design for the mentioned impedances in the datasheet but full non-linear characterization of PA cannot be performed.

b. **Measured Load Pull data:** This file better than Zin and Zout because this also allows designers to characterize Output Power, Efficiency, IMD etc as long as these are included in the measured load pull file. Again, measured load pull file provides additional data but still it doesn't allow designers to perform all the characterization which might be needed by them.

If Non-Linear model is not available:

1. **Agilent ICCAP:** Designers can use software like Agilent ICCAP to perform non-linear modeling themselves. Usually ICCAP is used with rack of instruments as may be needed for respective measurements but this approach requires good understanding of the semiconductor physics and device behavior. More information about ICCAP can be found on www.agilent.com/find/eesof-iccap
2. **X-Parameters:** Lot of vendors has started to provide measured X-parameter based models or designers can measure their devices and create X-Parameter models themselves. This technique is more suitable as this is purely based on measurement without having the need to have understanding on semiconductor physics etc. Accuracy of the modeling depends on the accuracy of the measurements which is easier to control for most of RF/uWave test engineers. X-Parameters can be extracted for any prebuilt amplifier i.e. Amplifier or Mixer modules which is called as 50-ohm X-parameters and these kinds of models can be used for system level simulations for bringing in accurate non-linearities of these components onto the system level.

For devices the X-parameters have to be extracted over an impedance range by using Impedance Tuners at source and load alongwith rest of the accessories for high power handling. Typical measurement setup for High Power X-parameter measurement is shown in figure 1.

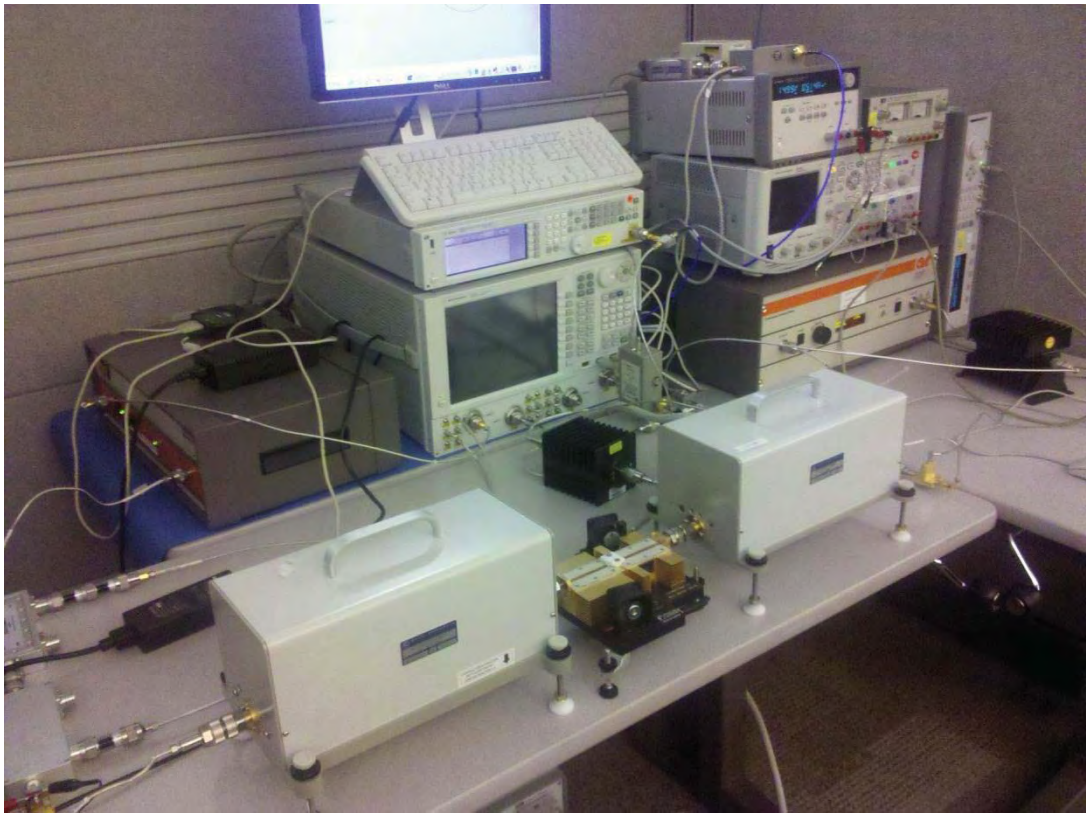


Fig 1: High Power X-Parameter measurement bench

For more details on X-parameters, see: www.agilent.com/find/nvna

In this case study we have assumed that non-linear model for the device is available with the designers.

Steps for Power Amplifier Design:

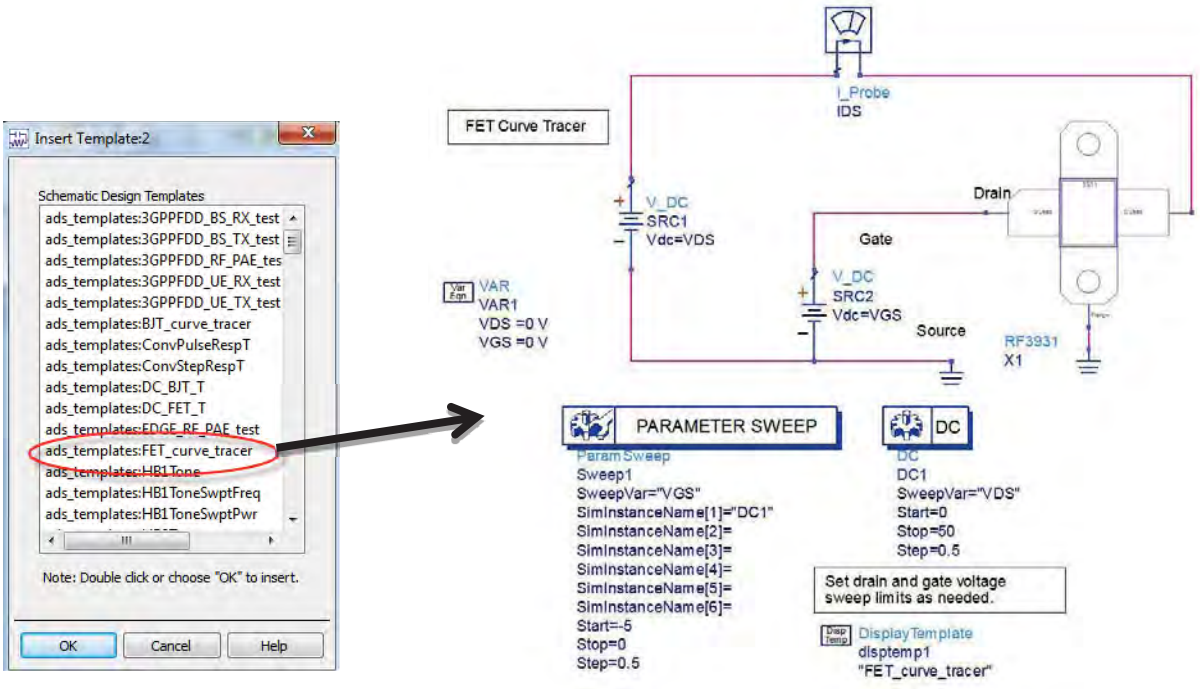
Key steps to be followed in designing a power amplifier are as follows:

- DC and Load line analysis
- Bias and Stability
- Load Pull Analysis
- Impedance Matching
- Source Pull (Optional Step)
- PA Final Characterization – Did we meet the specification?
- Optimize/Fine Tune the design
- Test Design with real world modulated signals (Optional Step)

Step 1: DC IV characteristics

Create a new workspace in ADS and make sure we include **lib.defs of RFMD GaN library (or any other vendor for which design kit is available)** during or after the workspace is created so that we have the access to the non-linear models for devices like RFMD RF3931 which is a GaN power device (https://estore.rfmd.com/RFMD_Onlinestore/Products/RFMD+Parts/PID-P_RF3931.aspx?DC=25) which we shall use for our amplifier design in this chapter.

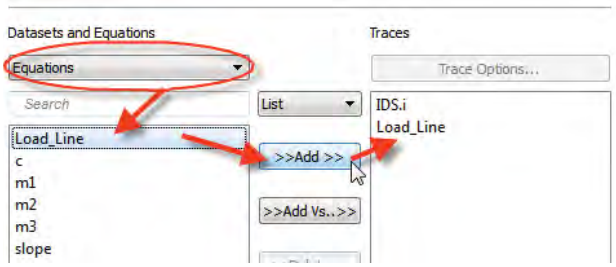
a. Create a new schematic cell with a name "Step1_DCIV" and insert a DC IV template by going to Insert->Template->FET Curve Tracer as shown below
b. Insert RF3931 device from the RFMD library palette and modify following parameters on template:
    a. VDS=0 to 50V in step of 0.5V
    b. VGS=-5 to 0V in step of 0.5V



c. Simulate the design and observe data display where IV characteristics of the device will be shown.
d. Do following operations on data display page:
    a. Insert 2 markers on the IV plot and place m1 and the IDSS point (near to peak current) and m2 marker near cutoff at Vgs=-5V & VDS=50V

    b. Using the Equation block, insert 3 equations on the data display to compute the load line:
        i. slope=(m1-m2)/(indep(m1)-indep(m2))
        ii. c=m2-slope*indep(m2)
        iii. Load_Line=slope*VDS[0,::]+c

c. Double click on the graph, change the dataset to Equations and select Load_Line and click on >>Add>> as shown here



d. Place marker m3 at VDS=48V & VGS=-4V and note the readout for DC power consumption. This is the bias which we shall use for our PA for Class AB operation.

e. Once finished data display page will look as shown below in fig 2.

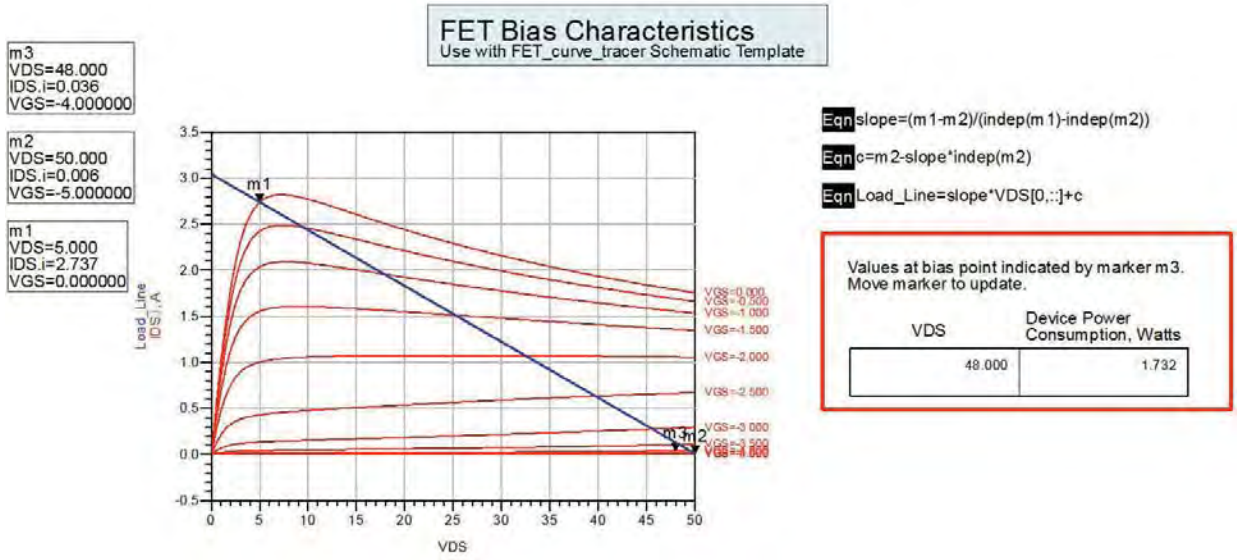


Fig 2: DC IV characteristics with Load Line

Step 2: Bias Network Design:

Proper Bias network design is essential for any non-linear circuit design as it is essential to ensure that right amount of bias reaches the device and also it doesn't load/leak the desired RF energy. Choice of bias network topology is pretty much dependent on the frequency of operation. For lower frequencies designers can use Inductors/Choke in the DC bias path and for higher frequencies high impedance quarter wavelength line is the preferred choice.

In the bias network design shown in Fig 3, various sections are marked and zoomed view of each section are provided for designers for easy understanding in Fig 3(a) – Fig 3(e). Open a new schematic cell with name "Device_with_BiasNW" and place components as shown in Bias network design or design your own bias network.

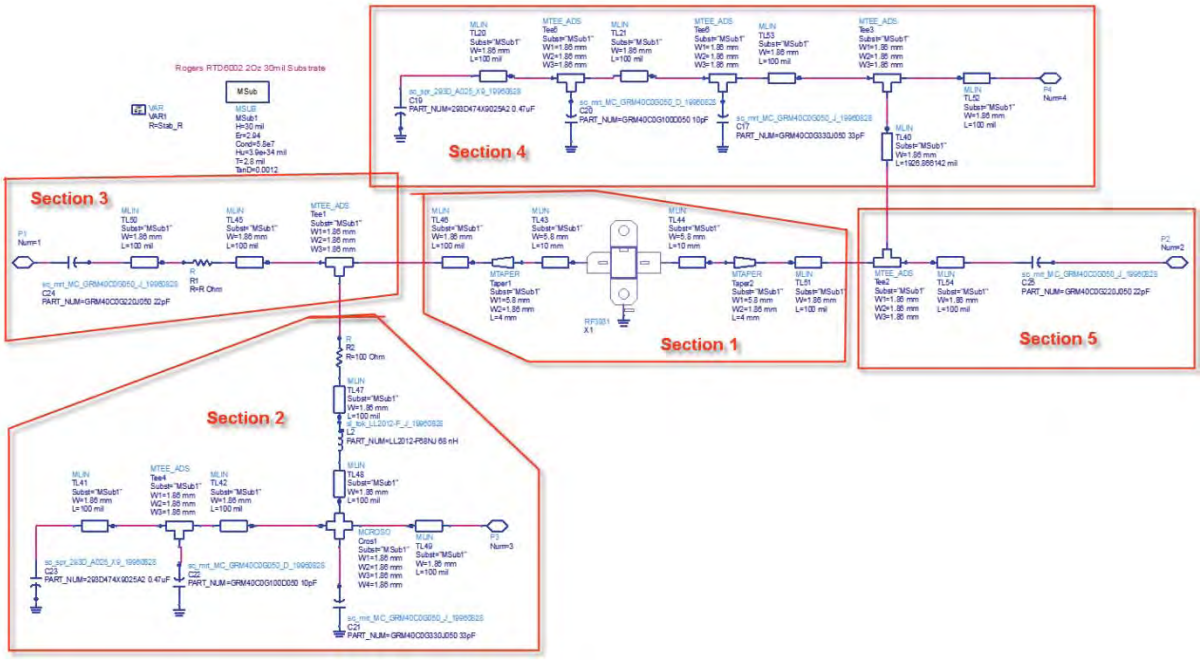
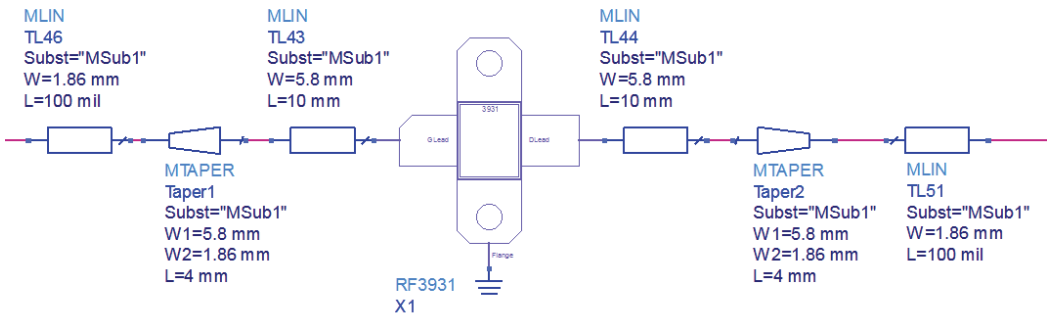


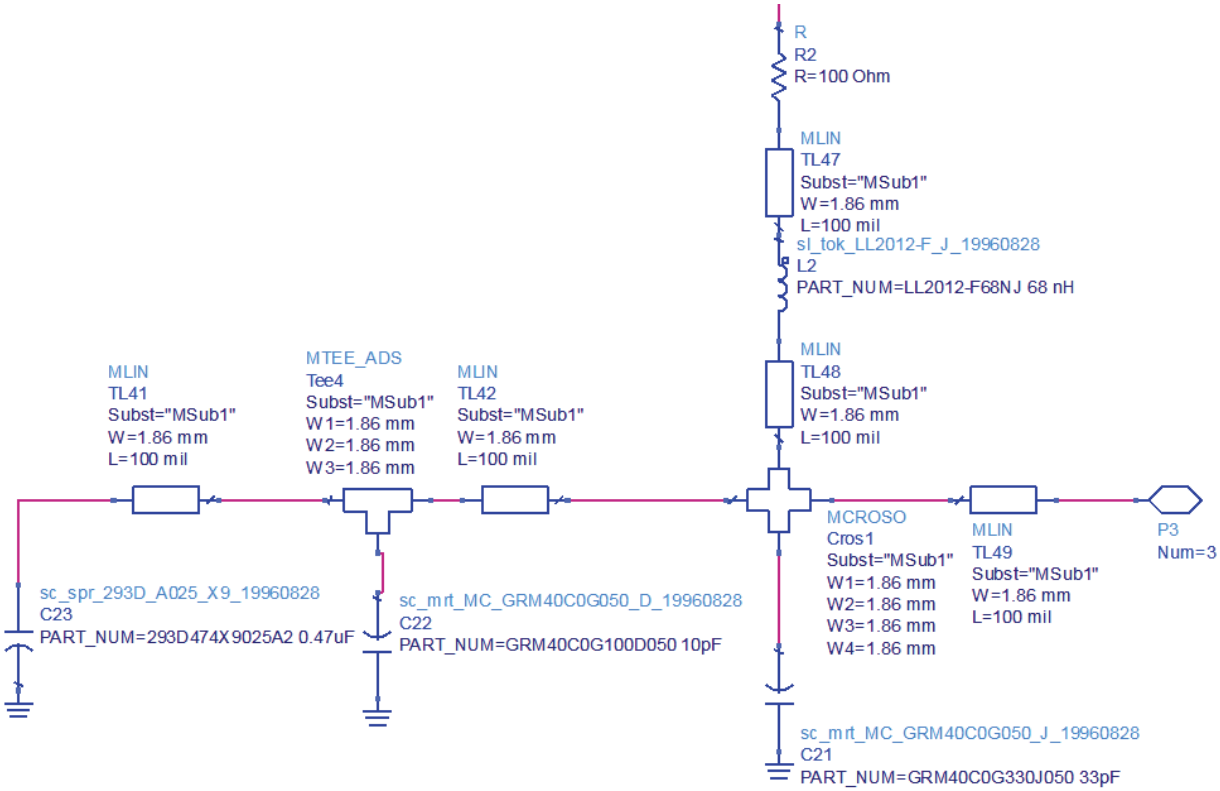
Fig 3: Bias Network for GaN power device

From TLines->Microstrip library place MSUB component as define the parameters as shown below for Rogers RTD6002 substrate. Define a variable as R=Stab_R which shall be used for finding out the required resistor value for device stabilization.

Section 1: Device with Terminal lead mounting lines and taper for providing gradual transition to 50 Ohm impedance line. Microstrip Line dimensions are shown in snapshot below.



Section 2: Gate Bias section with 3 bypass capacitors, DC bias choke (Inductor) and a 100 stability resistor in series with Gate bias.



Bill of Material for Gate Bias Section:

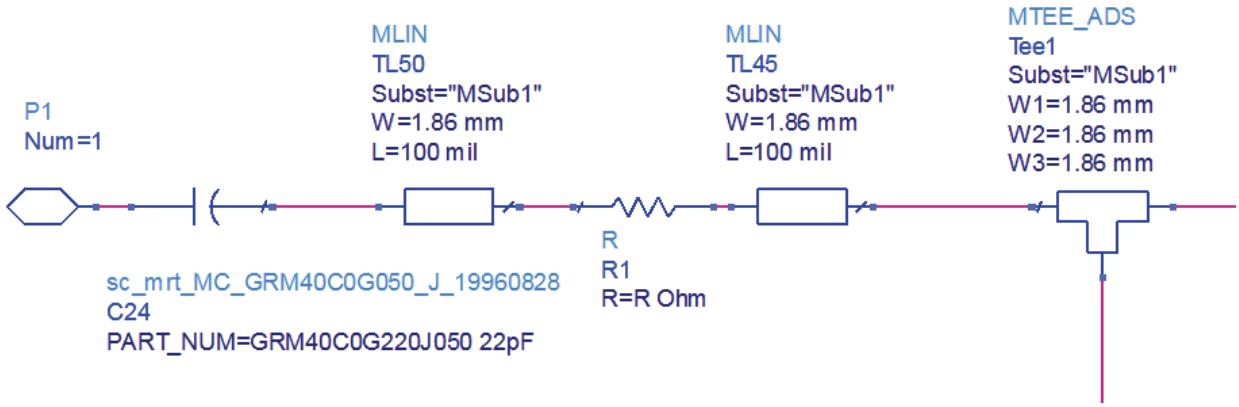
For SMT parts in ADS2011, unzip SMT components library which can be found under and add the lib.defs file from the unzip folder to use components in the design using DesignKits->Manage Libraries option in the ADS main window:

<ADS install dir>\oalibs\componentLib\RF_Passive_SMT_vendor_kit

e.g: C:\Agilent\ADS2011_10\oalibs\componentLib\RF_Passive_SMT_vendor_kit

Component Name & Type	Value	Library
C21 – SMT Capacitor	33pF	Murata: sc_mrt_MC_GRM40C0G050_J_19960828
C22 – SMT Capacitor	10pF	Muratra: sc_mrt_MC_GRM40C0G050_D_19960828
C23 – SMT Capacitor	0.47uF	Sprague: sc_spr_293D_A025_X9_19960828
L2 – SMT Inductor	68nH	Toko: sl_tok_LL2012-F_J_19960828
R2 – SMT Resistor	100Ohm	Lumped Components
Other Microstrip lines	As shown in snapshot	TLines - Microstrip

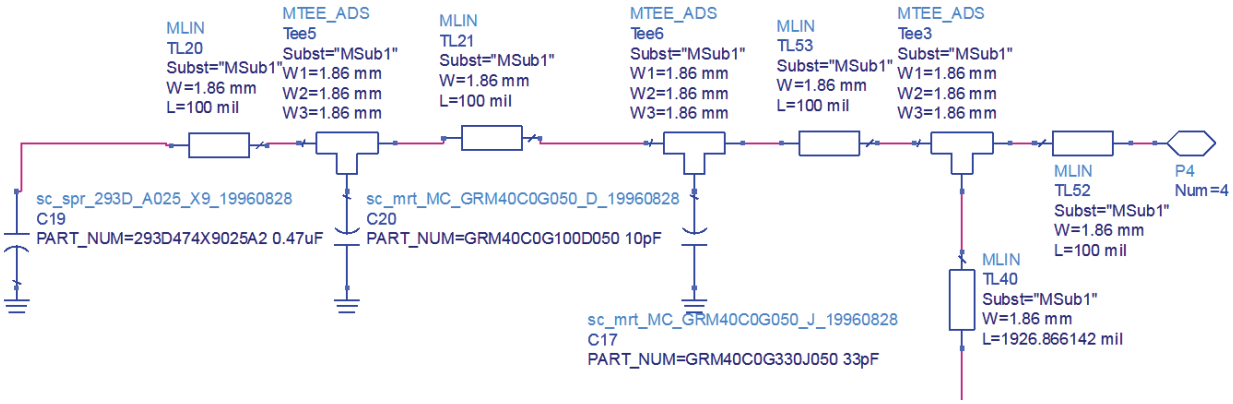
Section 3: Section 3 is for input side of the bias network which includes a resistor R1 for device stability and the value is defined as **R Ohm** which we shall tune to achieve the stability for the power device.



Bill of Material for section 3:

Component Name & Type	Value	Library
C24 – I/P Coupling SMT Capacitor	22pF	Murata: sc_mrt_MC_GRM40C0G050_J_19960828
R1 – SMT Resistor	R Ohm	Lumped Components
Other Microstrip lines	As shown in snapshot	TLines - Microstrip

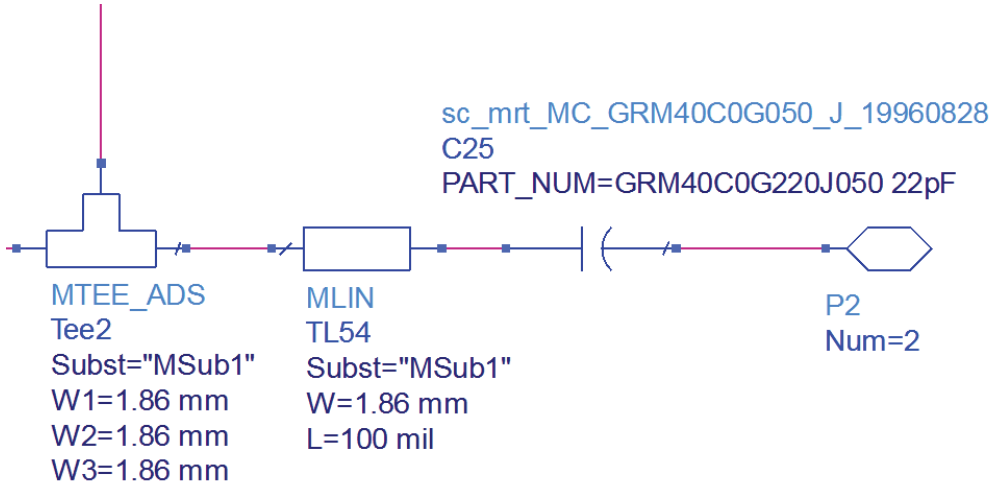
Section 4: This part of the Bias network provides the bias to the drain of the device.



Bill of Material for Drain Bias Section:

Component Name & Type	Value	Library
C17 – SMT Capacitor	33pF	Murata: sc_mrt_MC_GRM40C0G050_J_19960828
C20 – SMT Capacitor	10pF	Muratra: sc_mrt_MC_GRM40C0G050_D_19960828
C23 – SMT Capacitor	0.47uF	Sprague: sc_spr_293D_A025_X9_19960828
Other Microstrip lines	As shown in snapshot	TLines - Microstrip

Section 5: This part is for the output side of the bias network



Bill of Material for section 5:

Component Name & Type	Value	Library
C25 – O/P Coupling SMT Capacitor	22pF	Murata: sc_mrt_MC_GRM40C0G050_J_19960828
Other Microstrip lines	As shown in snapshot	TLines - Microstrip

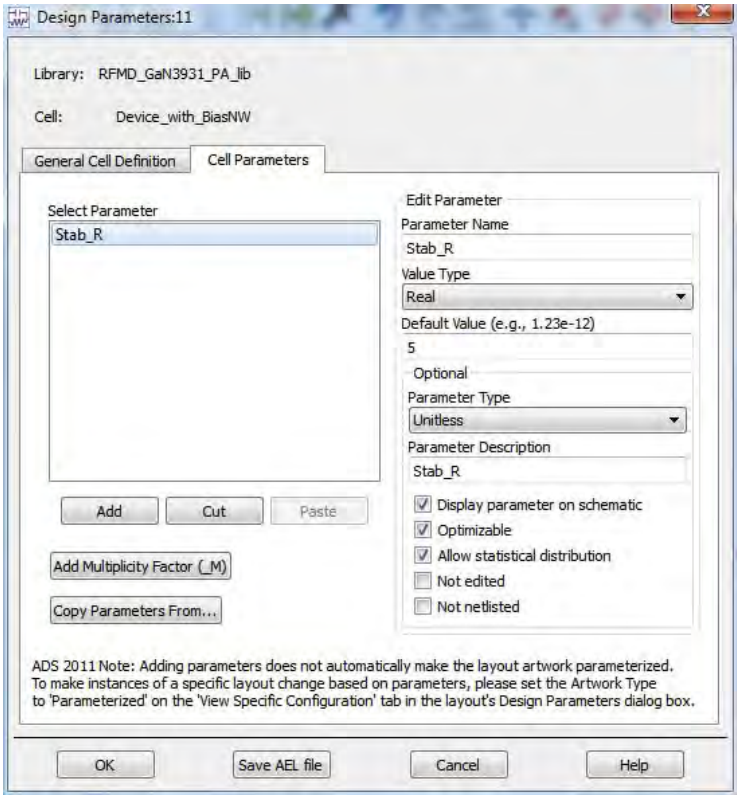
Hierarchal parameter definition for Stability resistor:

We shall define a top level parameter for stability resistor value so that it is easier to set it at top level when we want to tune, optimize or modify it to see the difference in results.
Go to File->Design Parameters->Cell Parameters, enter following:

Parameter Name: Stab_R
Default Value: 5
Parameter Type: Unitless
Parameter Description: Stab_R
Make sure following boxes are checked

a. Display parameter on schematic
b. Optimizable
c. Allow Statistical distribution

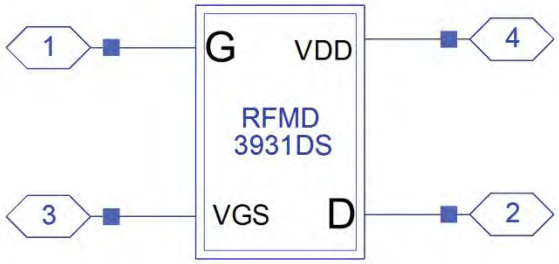
Click on Save AEL file and click OK.



Step 3: Small Signal Stability Analysis

Open a new schematic cell with name “Step2_Small_Signal_Stability” and from main ADS window, drag and drop design cell “Device_with_BiasNW” and you shall see a symbol generation message click “Yes” and click OK on the symbol generator dialog to see a default symbol with 4 pin appear for our use. From the Workspace tree under the cell name, double click on Symbol and this will open the symbol editor for us to create our own symbol for better understanding and use in this workspace.

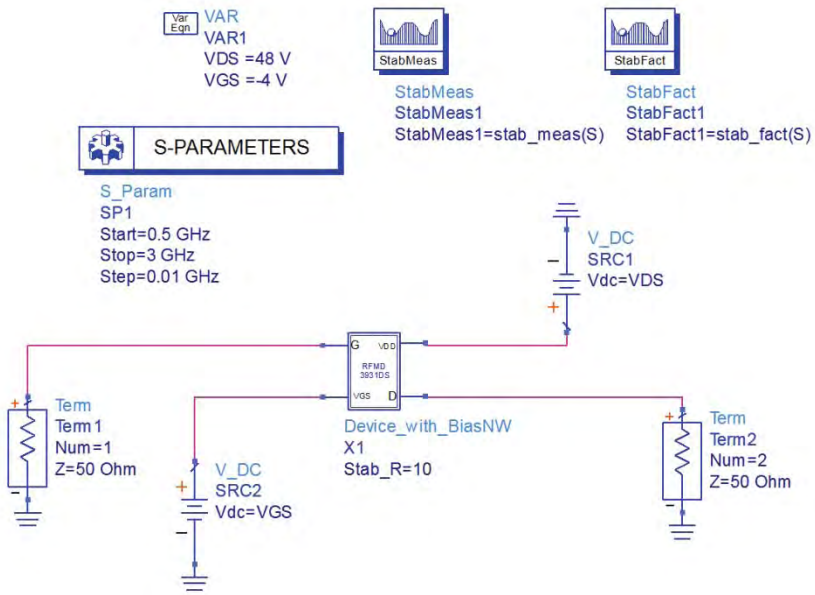
Create following symbol using the symbol editor icons on left hand side of the symbol generator schematic. Provide relevant texts for easier identification of the connection pins and note that Ports 1…4 should be matching the names/place where Ports are kept inside Device_with_BiasNW e.g. Port 1 is connected at the RF input of the Gate terminal of the device as shown in Section 3 snapshot earlier.



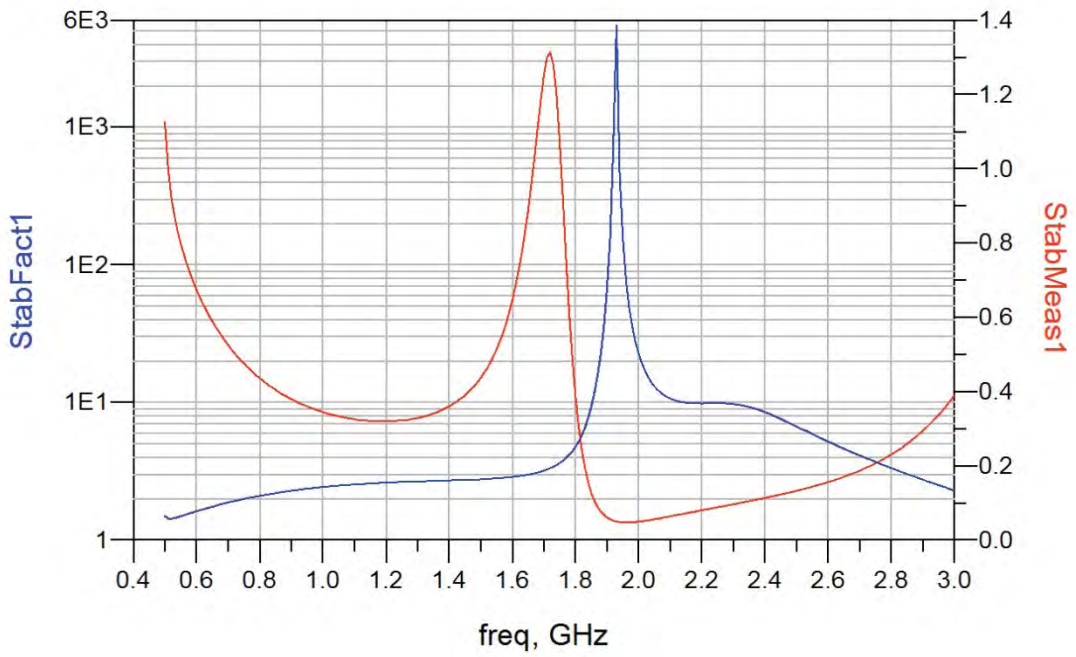
Place the device on schematic and make stability analysis bench as shown below. Place StabFact and StabMes measurement components from Simulation-S_Param library. Define Stab_R=10 so that the stability resistor value inside the subnetwork is set to 10Ohm.

Necessary and sufficient conditions for device to be stable are:

Stability Factor (K) > 1 and Stability Measure > 0



Perform simulation and plot Stability Factor and Stability measure on the rectangular graph as shown.



In the graph shown here, stability factor is plotted on the left-Y axis with log scale and Stability Measure is plotted on the right-Y axis. It can be seen Stability Factor is more than 1 and Stability Measure is greater than 0 over the entire frequency range hence our device is stable with the help of stability resistors inside subnetwork and we can begin our actual PA analysis as outlined in next few sections.

Step 4: Load Pull Analysis

Load Pull is a very commonly used and preferred analysis for PA design applications. Load Pull is the technique during which we keep source impedance and source power is kept constant at certain level and then sweep impedance / reflection coefficient of load over certain section in smith chart to characterize Output Power, PAE, IMD (with 2-tone LoadPull) etc to find out our optimum impedance to be presented to device and then accordingly perform impedance matching network design.

Critical things to determine while performing Load Pull simulation are:

a. Which section of the Smith Chart to use for load impedance?
b. What source impedance to keep while performing load pull simulations?
c. How much should be the source power for load pull simulation?

Now there are no straight answers to these questions but one can follow simple guidelines as given here to work through them in an iterative manner before final Load Pull analysis.

Tip 1: How to select area in Smith Chart for Load Pull?

For finding out which section of smith chart is to be used can be obtained from device datasheet which sometime can provide certain information or one can decide to define a section and then go around various parts in Smith Chart to finalize the optimum location. Usually power devices work at lower impedances so sections near periphery are the best guess to start with and designers can start to divide Smith on four quadrants and work their way to reach right area to zoom in and perform load pull simulations.

Tip 2: What Source Impedance to keep during Load Pull?

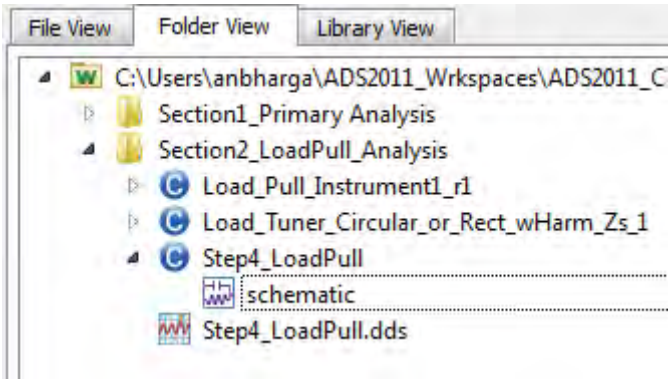
Usually power devices have lower impedances so keeping source impedance as 5 or 10 Ohms offers good starting point for a designer and then this can be tweaked to arrive at good number. After successful load pull simulation ADS provides pretty good estimate of optimum source impedance or designers can perform Source Pull Analysis to find optimum source impedance for maximum gain hence reducing the compression level while extracting required amount of output power from the device. For example, in our case we have used 10Ohm resistor in series with Gate hence we shall keep 15 Ohm as our starting point for Source Impedance during our LoadPull simulations.

Tip 3: How much should be the Source Power for Load Pull Analysis?

Good estimate of the source power to be kept can come from the device datasheet which provides the gain of the device at certain frequency. Good way to calculate required input power required is by formula = **(output power required – gain as mentioned in datasheet) + 3dB** and then it can be reduced or increased in couple of iterations and final value of source power can be decided.

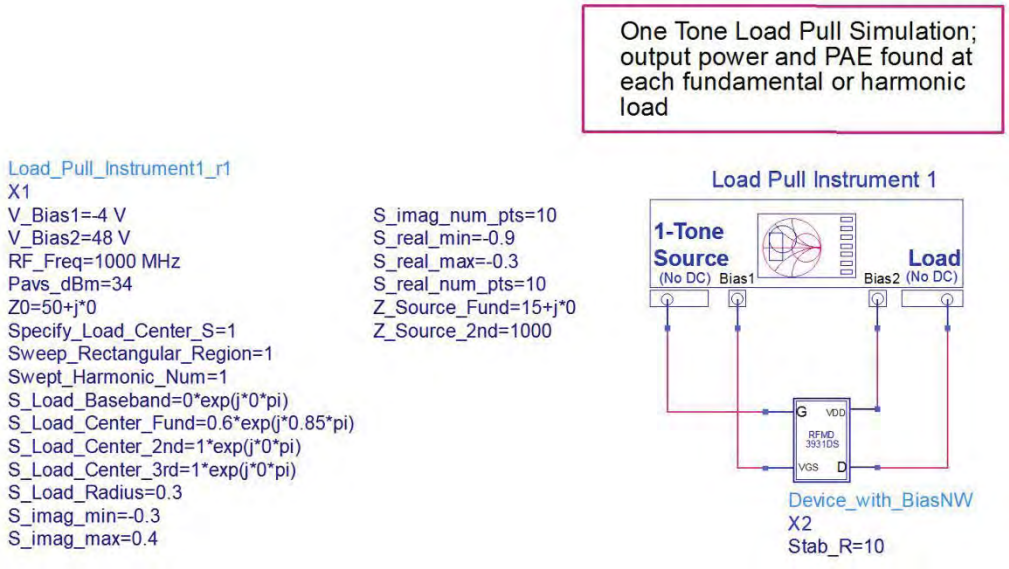
Load Pull Simulation for our Amplifier:

1. Click on **Designguide->LoadPull->One Tone, Constant Available Source Power Load Pull** and this shall copy few schematics and one data display onto the workspace tree….rename HB1Tone_LoadPull to **Step4_LoadPull** and HB1Tone_LoadPull.dds to **Step4_LoadPull.dds** as shown here

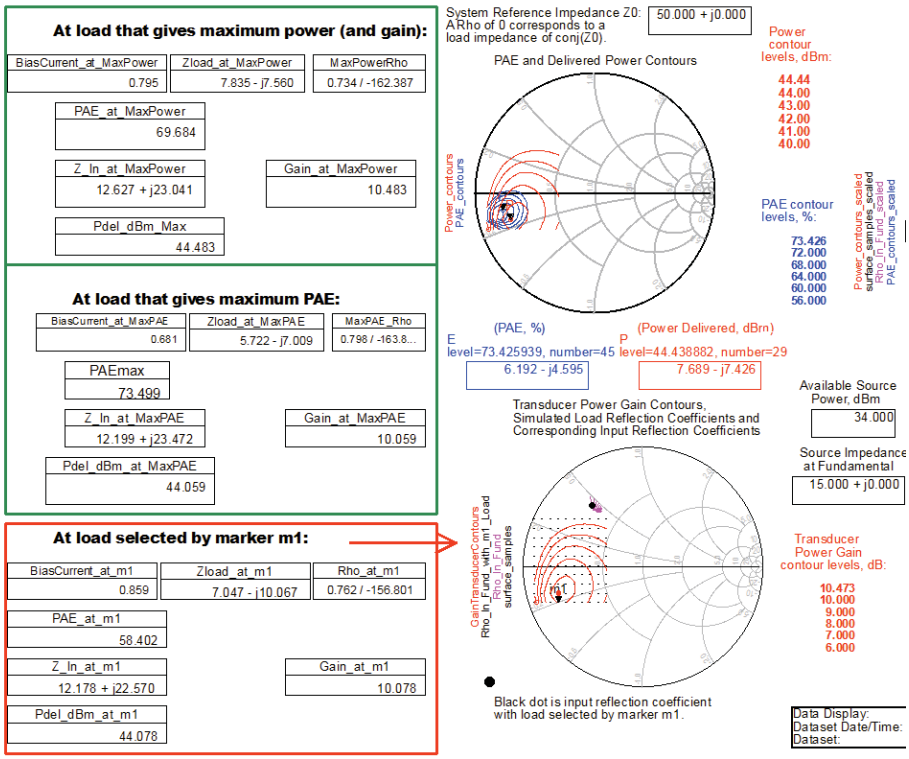


2. Open the schematic of Step4_LoadPull and you shall see a LoadPull instrument with a default device, delete the device and its connections and drag and drop “Device_with_BiasNW” onto this schematic and change **Stab_R = 10** and make connections to the Load Pull Instrument. Make following changes on the parameters by double clicking on the LoadPull Instrument:
    a. V_Bias1 = -4 V
    b. V_Bias2 = 48 V
    c. RF_Freq = 1000 MHz
    d. Pavs_dBm = 34
    e. S_imag_min = -0.3
    f. S_imag_max = 0.4
    g. S_imag_num_pts=10
    h. S_real_min = -0.9
    i. S_real_max = -0.3
    j. S_real_num_pts = 10
    k. Z_Source_Fund = 15+j*0

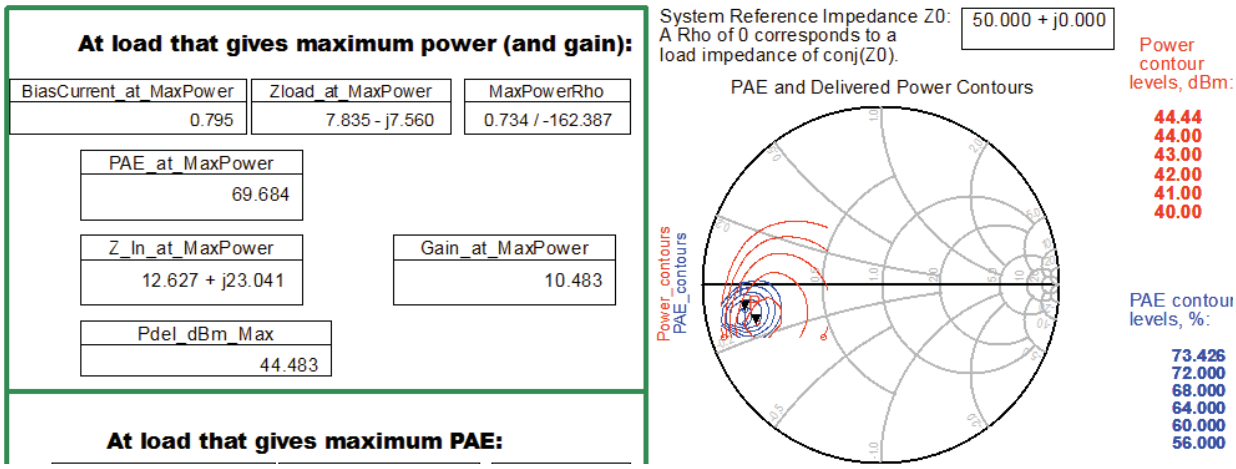
Once finished schematic will look as shown here:



Perform simulation by clicking on Simulate icon or press F7. Observe the data display which provides all the useful information



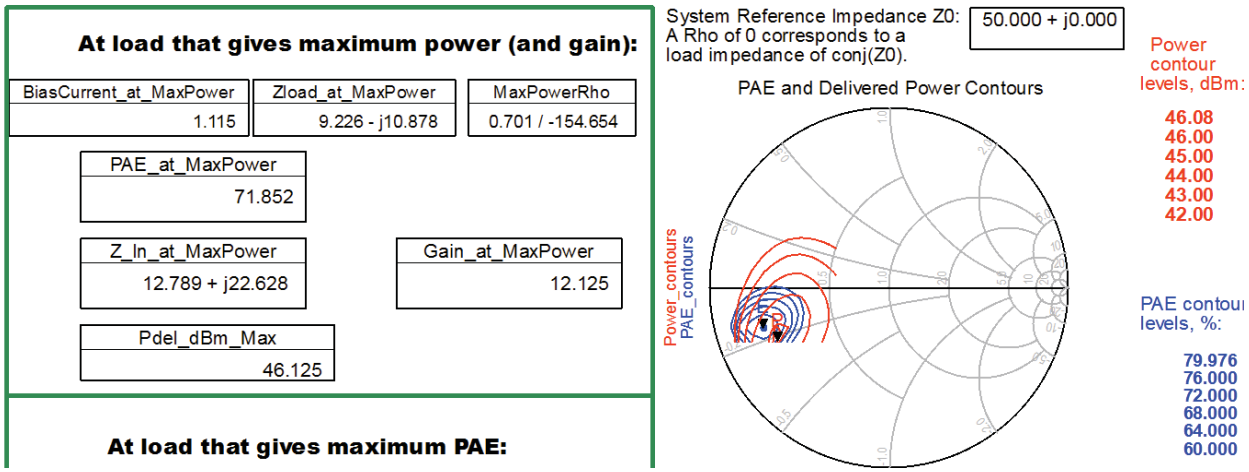
Zoom to the section which shows **"At load that gives maximum power (and gain)"**



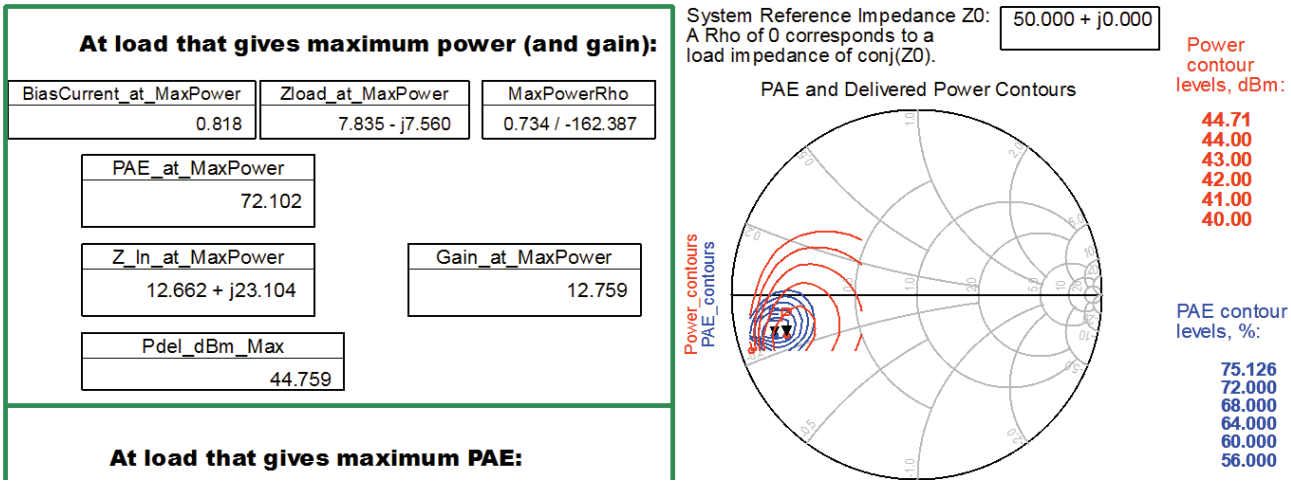
Notice that we are able to achieve the required output power of 44dBm (25Watts) but gain seems to be lower than what is mentioned in the datasheet which should be more than 12 or so and that is because we have not yet terminated source in its optimum impedance for maximizing the gain. We can note the optimum load impedance which is shown as 7.835-j*7.56 Ohm and if we match our device to this load impedance we shall obtain 44dBm of output power.

Go to schematic and modify the Z_Source_Fund = 12.6 –j*23 (complex conjugate) as predicted by Load Pull simulation which is the right termination for the source. For more sophisticated simulation designers can use the Source Pull template provided in Load Pull designguide whereby we shall terminate the load using the impedance of 7.835-j*7.56 and then vary the source impedance to find out the termination which provides the maximum gain from the device. For this exercise we shall use the source impedance as computed by the load pull simulation.

Perform load pull simulation again and observe the Pdel_dBm_Max and Gain_at_MaxPower as shown below



We can observe that the output power has risen to 46dBm and Gain has gone up to 12dB indicating that we can reduce the input power level by 2dB or so to achieve 44 dBm output power. Modify the source power Pavs_dBm to 32 and resimulate the design and observe the data display to note that we obtain output power of 44.75 dBm and Gain of 12.75 with a PAE = 72%



Take away from our Load Pull analysis:

Input Source Power = 32dBm
Input Impedance = 12.6 + j*23 Ohm
Output Impedance = 7.835 –j*7.56 Ohm

Step 5: Impedance Matching Network Design

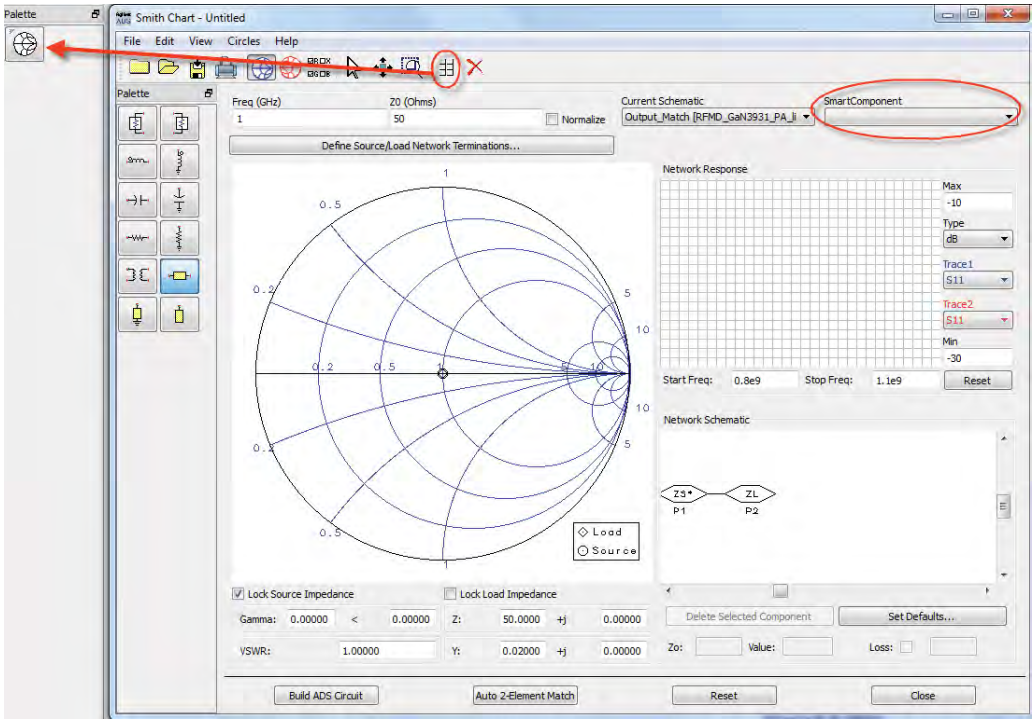
ADS offers variety of choices to perform Impedance Matching network design and designers can choose any of the options as listed below:

a. Tools->Smith Chart: This allows users to perform Lumped Element and transmission line based matching network design using an interactive Smith Chart tool.
b. Tools->Impedance Matching: This is smart component based impedance matching network synthesis which also allows users to perform broadband based matching network using Lowpass, Highpass or Bandpass topologies. Default synthesized network is always lumped components and using the lumped to transmission line transformation one can transform lumped components to equivalent transmission lines.
c. Designguide->Passive Circuit: This designguide can be used to synthesize single stub or double stub transmission line based matching networks.

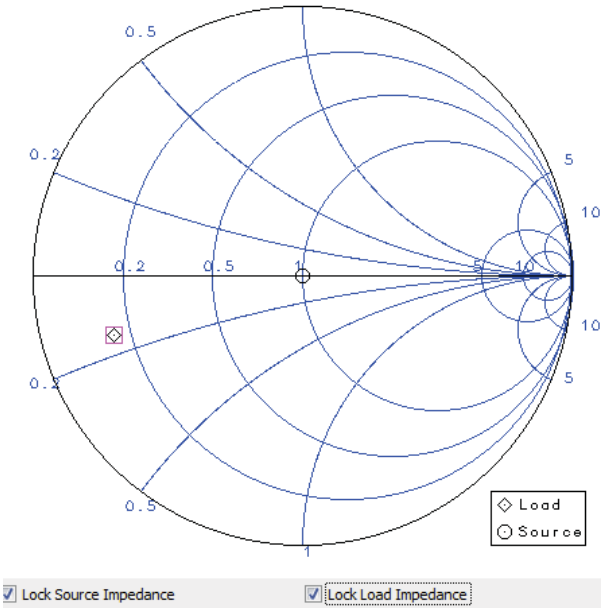
Output Matching Network Design:
For the present case of our Power Amplifier matching network, we shall use Smith Chart tool in ADS which provides greater control on the impedance matching network design.

1. Click on Tools->Smith Chart to see a pop up window of Smith Chart opening up.

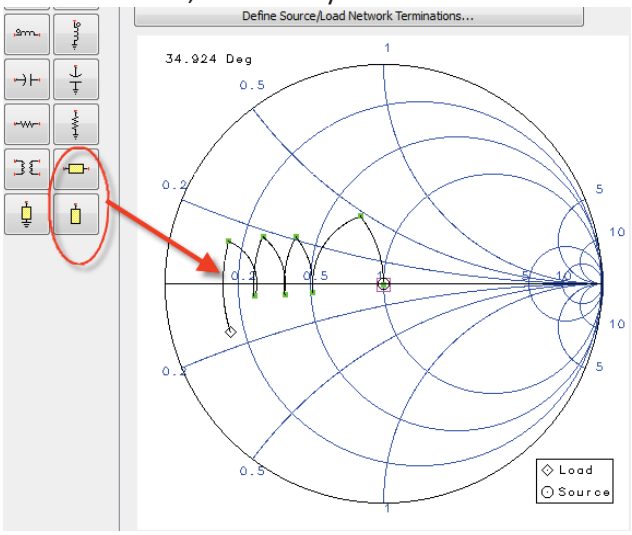
2. Click on Smart Component Palette icon to see Smith Chart component in Schematic palette as shown on next snapshot.
3. Place the Smith Chart component on to the schematic and select this component from the drop down box in the Smith Chart tool. **Uncheck the Normalize option.**



4. Click on ZS* from the Network Schematic and click on Lock Source Impedance. Select ZL and enter Z as 7.835 –j*7.56 as computed by our final Load Pull simulation. Once ZL point shift to the desired impedance point, select Lock Load Impedance so that we don't disturb the impedance point by mistake. Once done it should look similar to the one shown below:



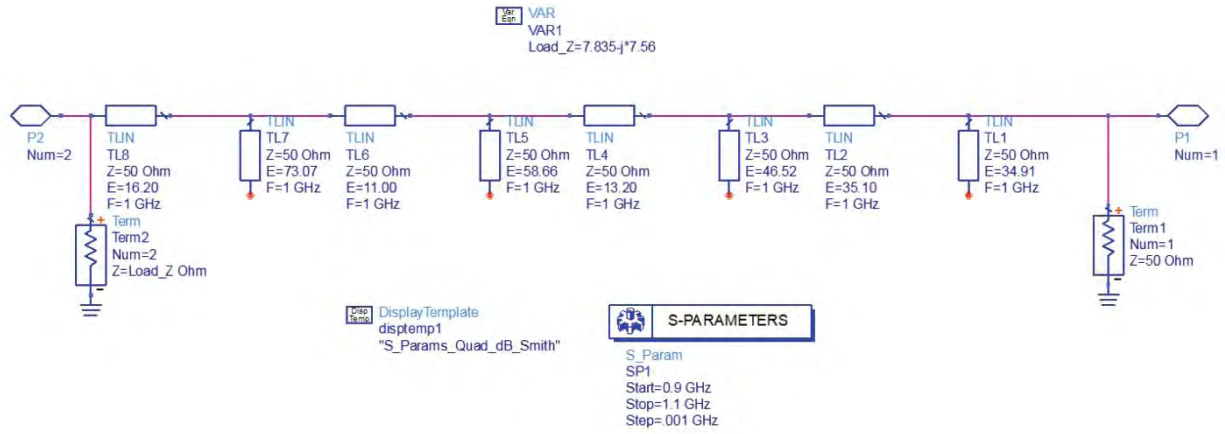
5. Now, we are ready for out impedance matching using either L, C component or using Transmission Lines in the component list….
    a. Click Series Transmission Line and move your mouse over Smith Chart and you shall notice the locus point moving with your mouse in upper direction indicating series inductor action with transmission line electrical length being displayed at upper left corner of the Smith Chart, click once you reach close to 16.1 degrees.



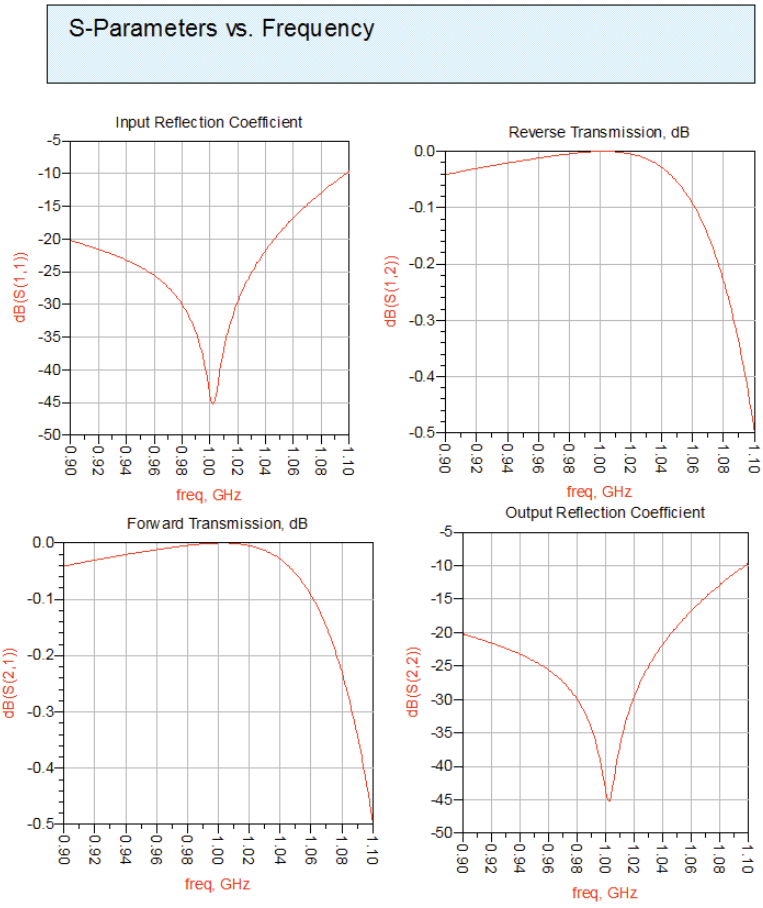
    b. Click Open Circuit stub and now the locus should move downwards indicating this is capacitive action, click mouse left button once you length close to 75 degrees.
    c. Repeat the series line and open stub 3 more times for following length (as close as you can reach)
        i. Series Line 1 = 16.2 degrees
        ii. Shunt Stub 1 = 73 degrees
        iii. Series Line 2 = 11 degrees
        iv. Shunt Stub 2 = 58.6 degrees
        v. Series Line 3 = 13.2 degrees
        vi. Shunt Stub 3 = 46.5 degrees
        vii. Series Line 4 = 35.1 degrees
        viii. Shunt Stub 4 = 35 degrees
    d. Final snapshot will look similar to the one shown above. It is possible for designers to choose how many sections they would like to have in their matching network by taking little longer curves but the problem with this approach would be bandwidth and that the matching network would be more sensitive to the process variation (remember Q-factor fundamentals). Designers can also plot Q-circles for matching network design by going to Circles->Q option of Smith Chart tool.
    e. Larger matching network will consume more area on PCB hence tradeoff between size and number of sections can be taken into account. **Another trick to reduce the size of matching network is to increase the impedance of series lines or to reduce the impedance of shunt stubs to increase inductive and capacitive properties of the transmission lines respectively.**
    f. After this impedance matching network design we have the ideal transmission line properties i.e. Impedance and Electrical Length for the matching network components and we can use LineCalc (Transmission Line Calculator) in ADS to compute physical

width and length of these lines based on the dielectric material which is used for circuit design. Refer to some of the earlier chapters on how to use LineCalc in ADS.

g. **Remember that our Source and Load Impedances used in Smith Chart tool are actually reverse (we kept source as 50 Ohm and load as 7.8-j*7.5) so we need to flip the output matching network when used alongwith the device so that Source impedance can be 7.8-j*7.5 and load impedance is 50Ohm as actually required.**

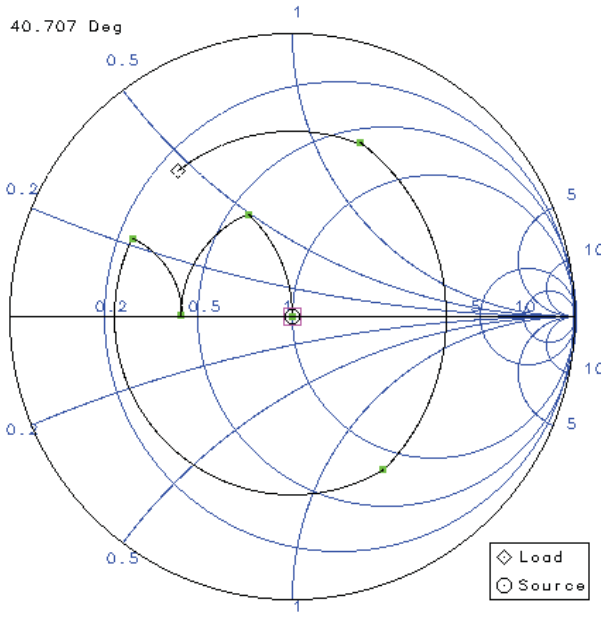


Notice the flipped network with Source impedance is defined as 7.835-j*7.56 and load as 50 Ohm (ignore the variable name which says Load_Z)

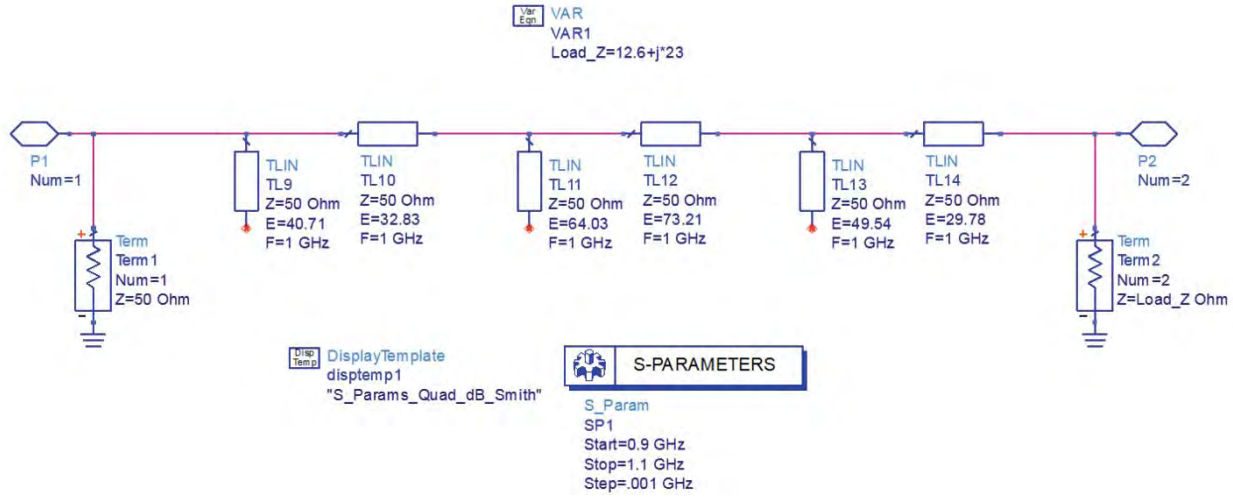


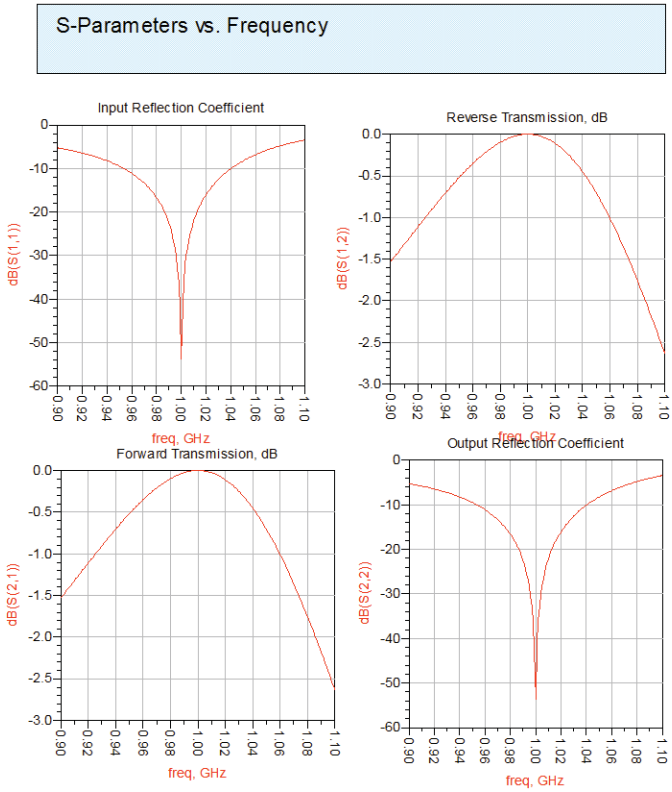
Input Matching Network Design:

Similar to output matching network design, we can design the input matching network with 4 series transmission lines and 4 shunt open circuit stub as Smith Chart display will look similar to the one shown below.



i. Shunt Stub 1 = 40.71 degrees
ii. Series Line 1 = 32.83 degrees
iii. Shunt Stub 2 = 64.03 degrees
iv. Series Line 2 = 73.21 degrees
v. Shunt Stub 3 = 49.54 degrees
vi. Series Line 3 = 29.78 degrees



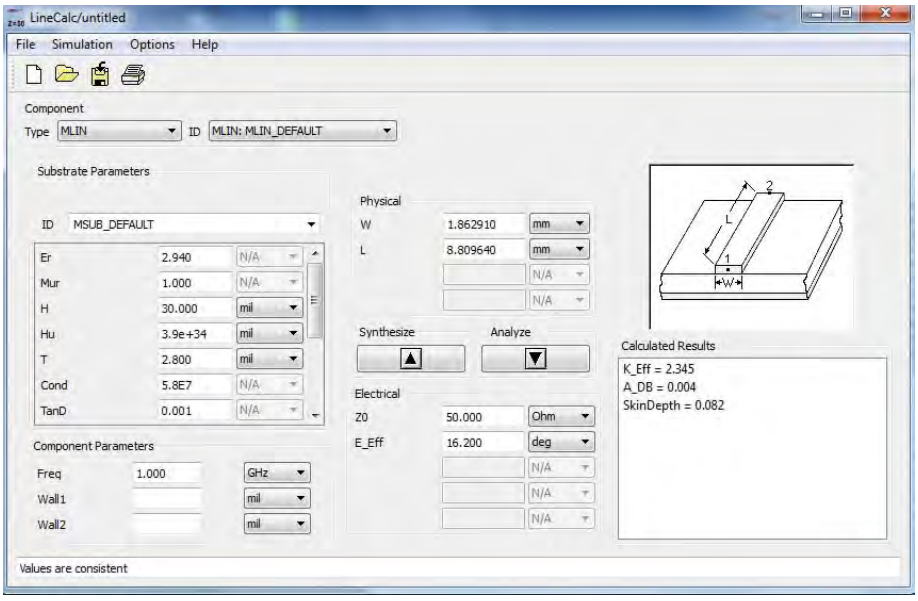


Matching Network after Microstrip Line Transformation using Line Calc:

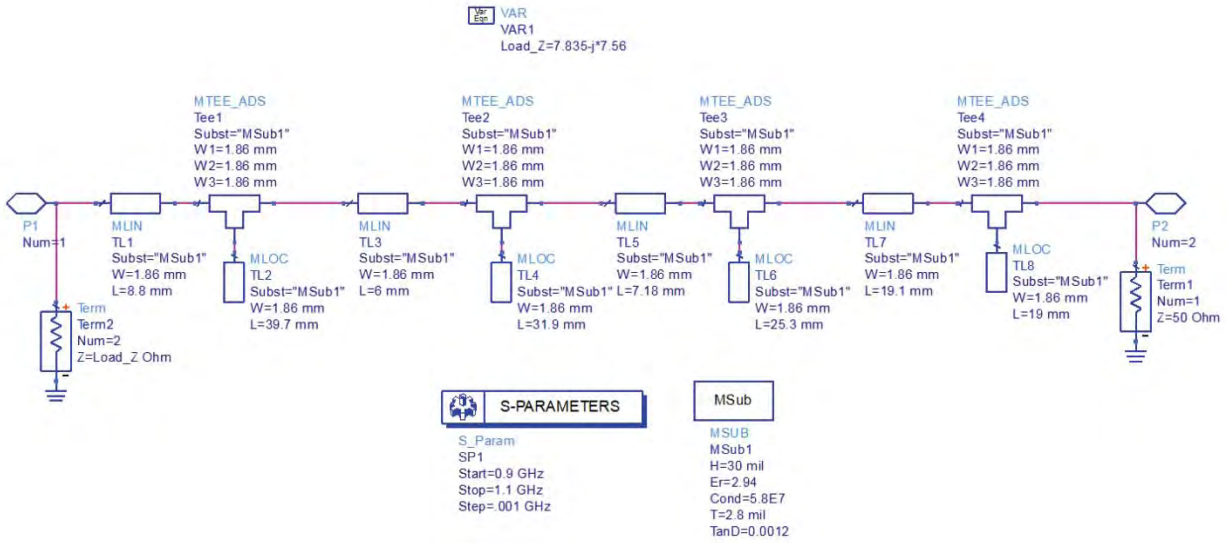
Substrate Definition and physical dimension calculation in Line Calc

MSub

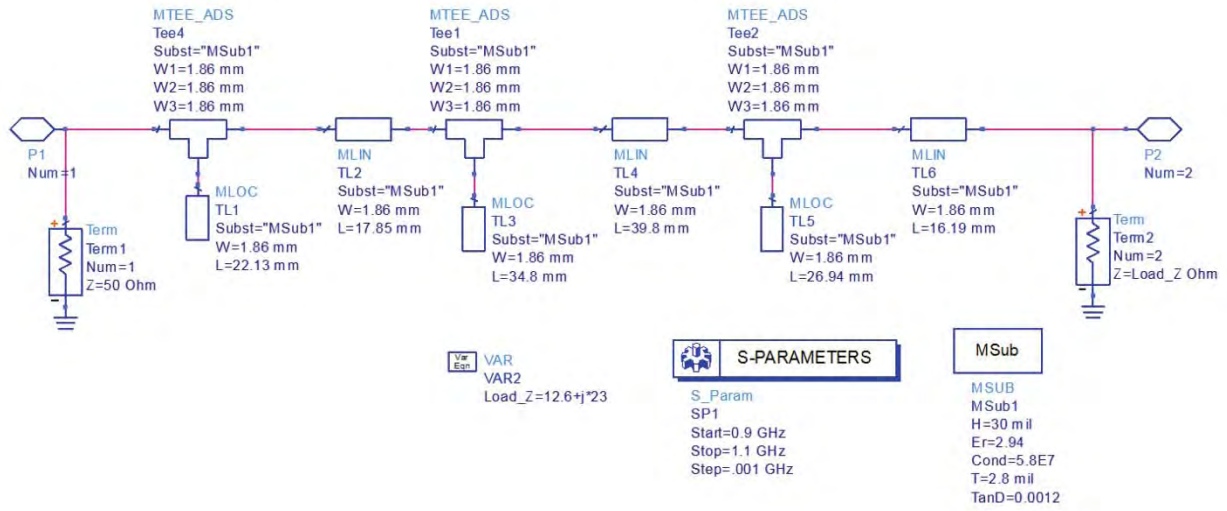
MSUB
MSub1
H=30 mil
Er=2.94
Cond=5.8e7
Hu=3.9e+34 mil
T=2.8 mil
TanD=0.0012



Output Matching Network:

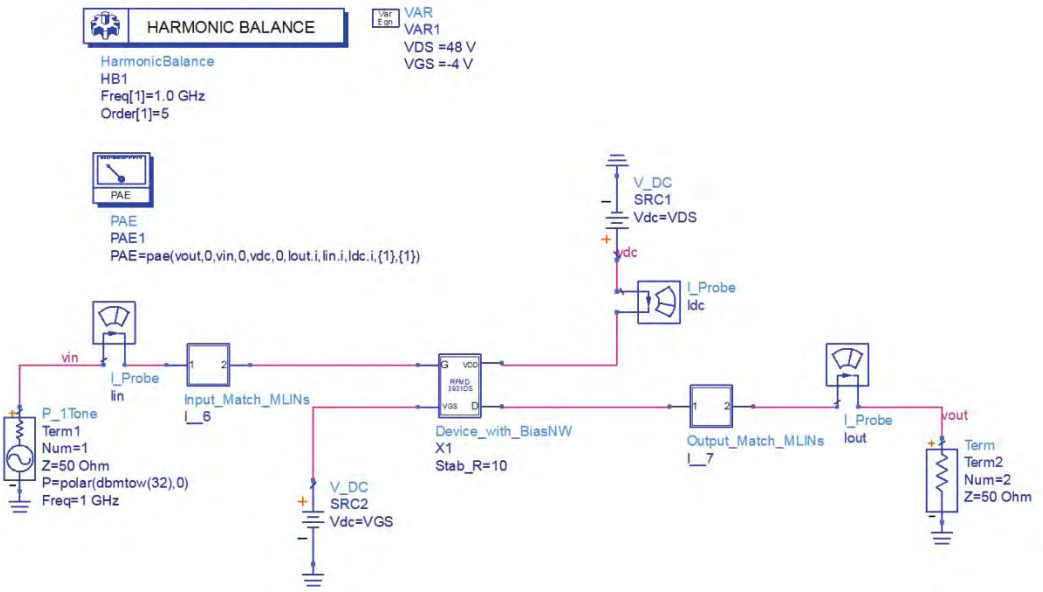


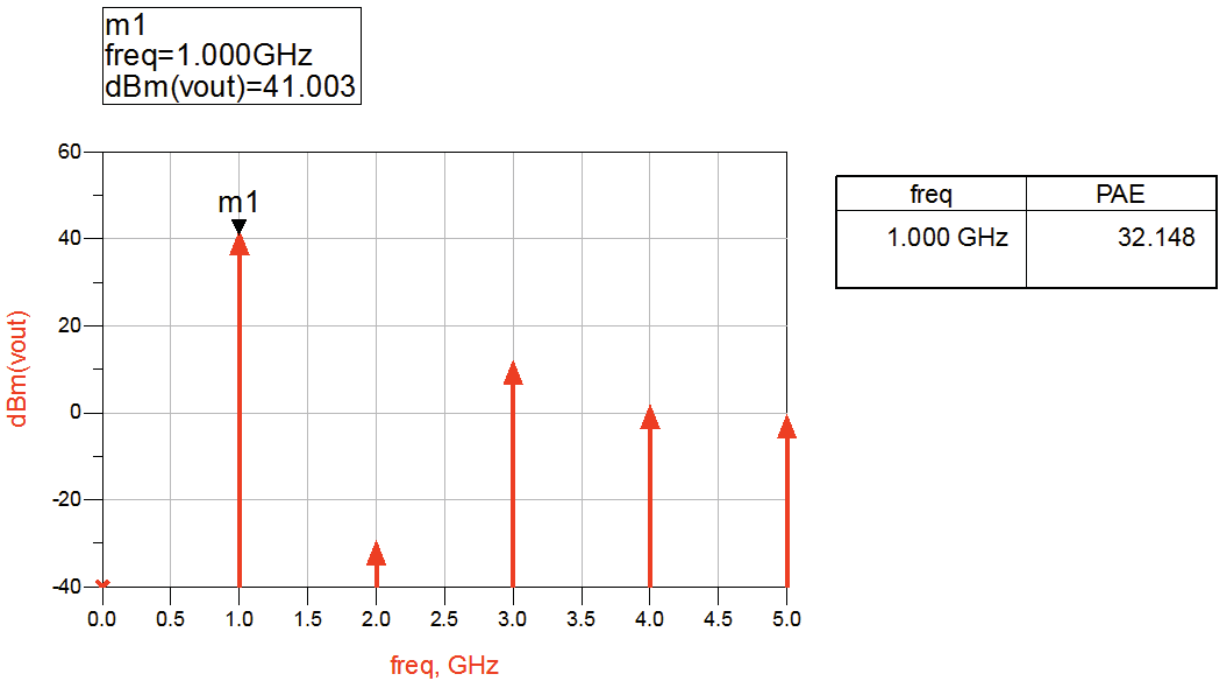
Input Matching Network:



Did we meet all Amplifier Specifications?

Create a new schematic cell with a name “Step5_PA_with_Match” and place “Device_with_BiasNW” (don’t forget to set Stab_R=10) with Input and Output Matching network and setup 1_Tone HB simulation to see if we met all the specifications as shown in next snapshot.
Current Probe component can be found under Probe Components and PAE function can be found under Simulation-HB library. Also note that these probes have been renamed as Iin, Iout and Idc for easier identification and vin, vout and vdc node names (wire labels) have been provided for pae() function.



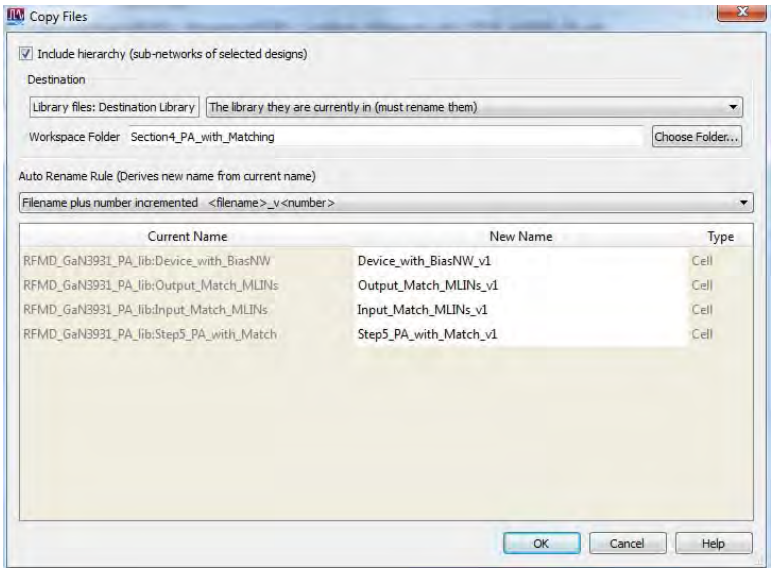


freq	PAE
1.000 GHz	32.148

From the above simulation, we notice that required output power is 3dB lower that what we expected and also Efficiency is much lower than our specification and we will need to optimize the matching networks to meet our required specifications.

Step6: Power Amplifier Performance Optimization

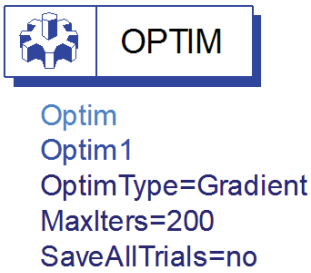
1. Right click on Step5_PA_with_Match and click on Copy Cell and select “Include Hierarchy” so that all subcircuits gets copies alongwith main design. Note “_v1” suffix will be added to all the designs as shown in copy cell window.



2. Click OK and notice new design cells in ADS main window…..right click on Step5_PA_with_Match_v1 and select "Rename", give new name as "Step5_PA_with_OptimizedMatch" and double click its schematic to open the same.

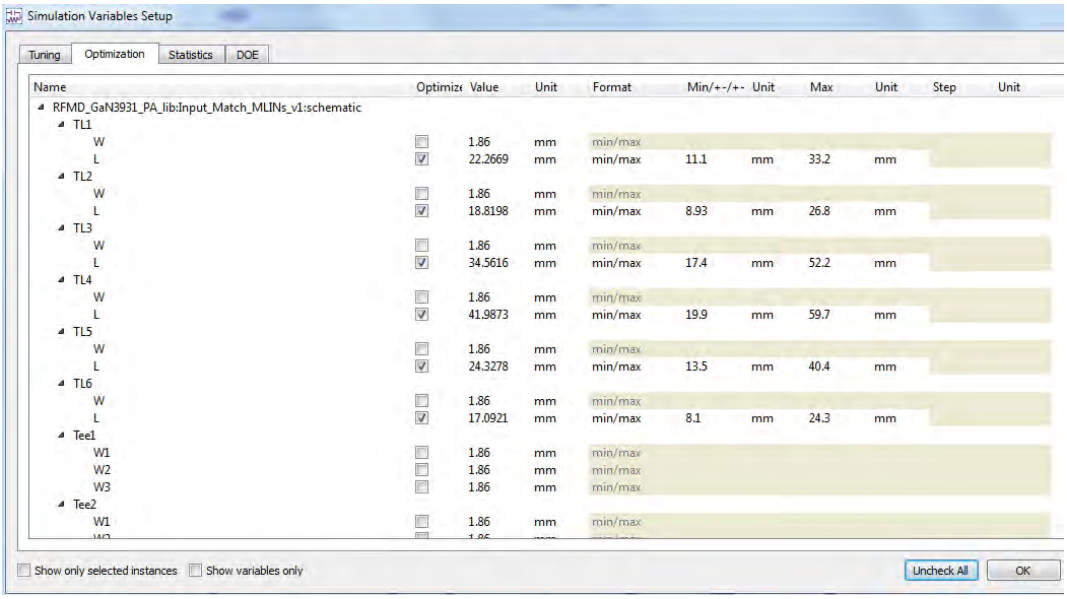
3. From Opt/Stat/DOE library, place 2 Optimization Goals and an Optimization Controller.

a. Goal 1: PAE (or PAE1) > 55 (our requirement is 50% but we keep extra 5% for better confidence)
b. Goal 2: dBm(vout[1]) > 44.5 ([1] indicates fundamental of output power spectrum, our required power is 44dBm but we decide to keep 0.5 dBm as extra margin for little better confidence)
c. Optimization Controller: Optimization Type: Gradient, Iterations: 200



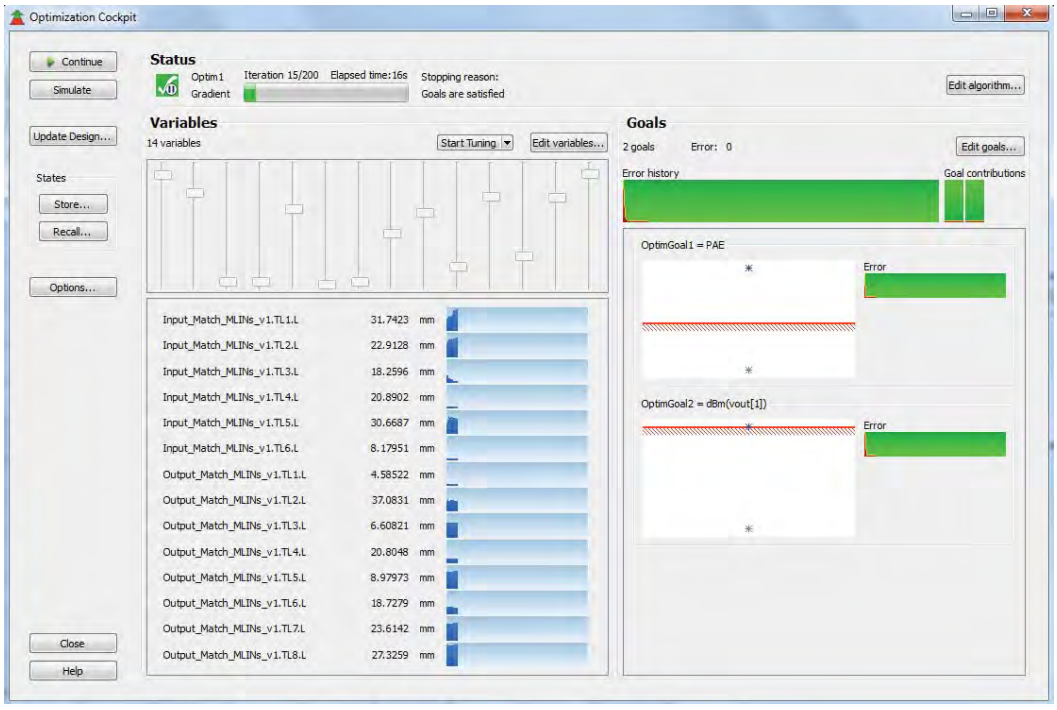
Note by default you may not see LimitMin[1] as shown with above 2 goals, same can be switched on by going to Display tab of goals. Similarly all other unnecessary items are switched off for optimization controller

4. Select **Simulate->Simulation Variables Setup.** The Simulation Variables Setup dialog box is displayed. Select the **Optimization Tab** in the pop up window and from the Input and Output match subcircuit components, click on transmission lengths to make them optimizable. It is possible to optimize the widths as well but in this case we shall just optimize the lengths of transmission lines. By default min and max for lengths will be +/-50% of the nominal value and we just use them as it is as that would be sufficient….



Click OK once all parameters are defined as optimizable.

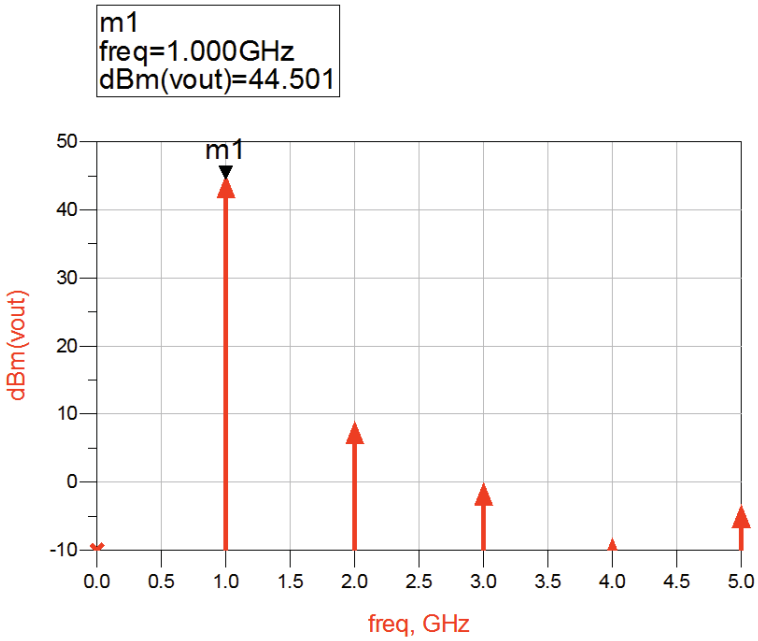
5. Click on Optimization icon in the schematic to begin the optimization process. Once desired goals are achieved, the Error will reach 0 indicating we have achieved our desired specifications.



Click on Close and Select Update the design. Perform simulation by clicking on Simulate icon on schematic tool bar and see the optimized results.

Optimized PA response:

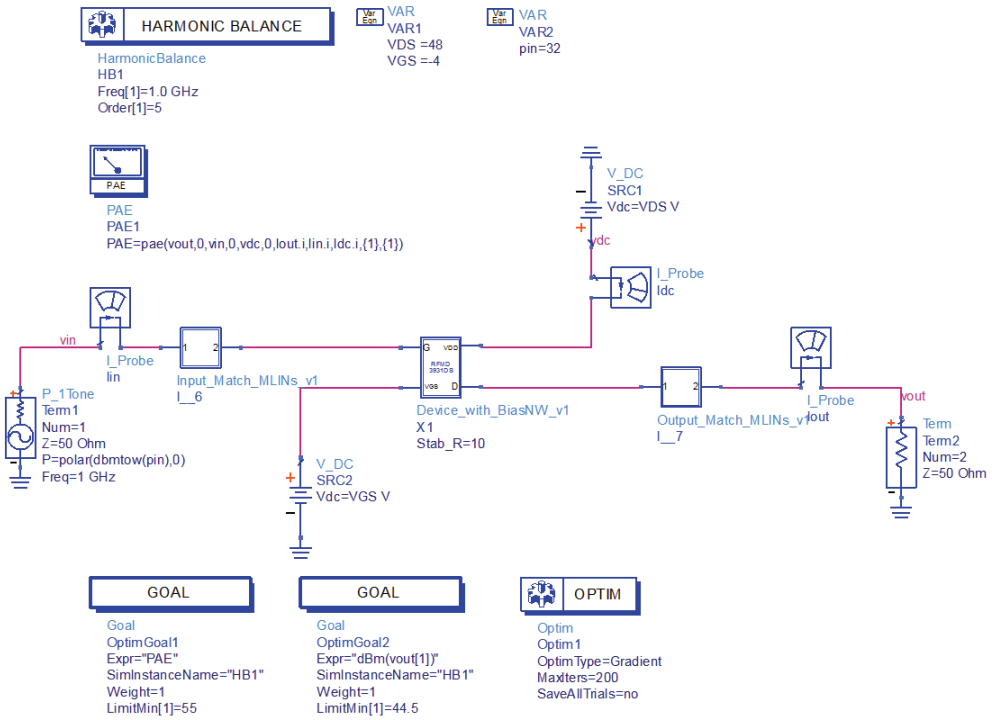
As we can see from the optimized results, we now meet the desired specifications of power and efficiency; we can go ahead and perform some additional simulations on our amplifier for complete characterization as illustrated in next few sections.



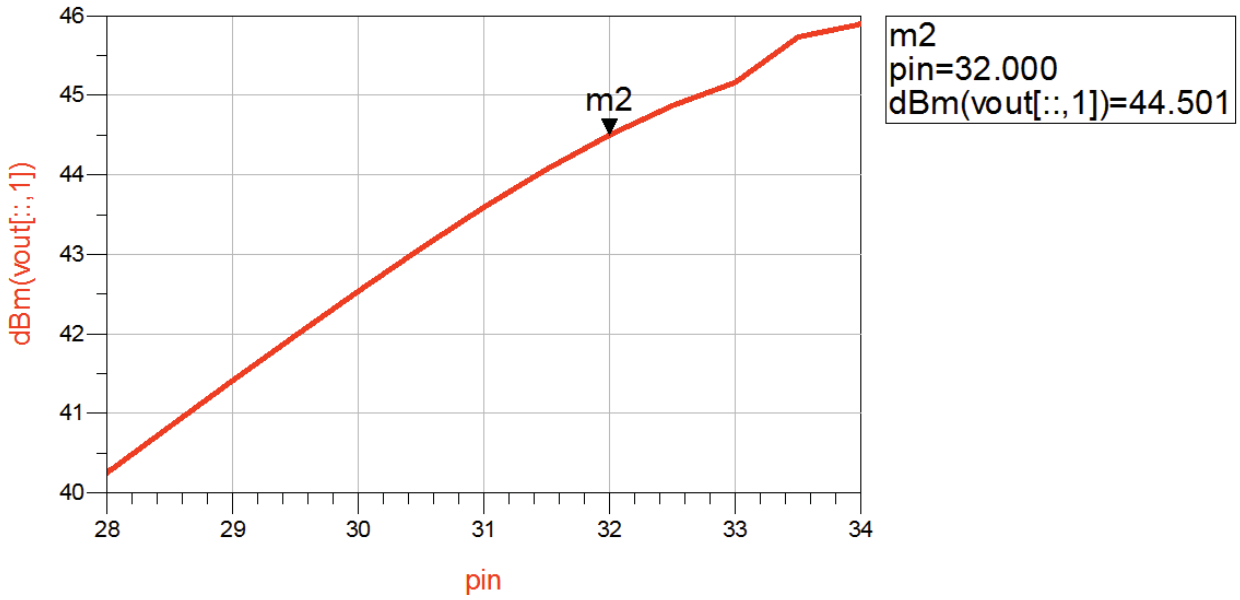
freq	PAE
1.000 GHz	64.650

1-Tone Power Sweep Analysis:

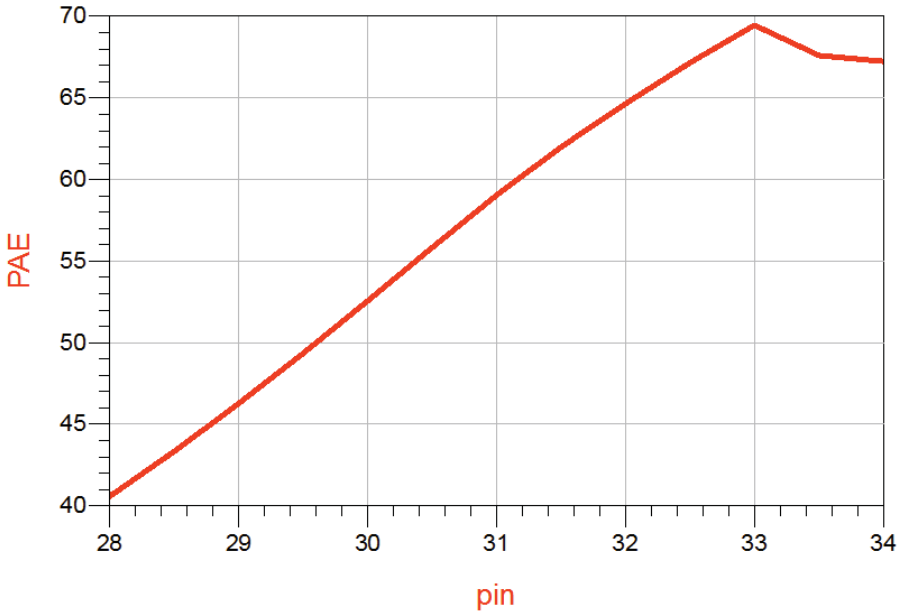
1. Define a new variable e.g. pin=32
2. In the P_1Tone source define “pin” instead of 32 so that input power can change once we sweep the pin variable.
3. Double click on HB controller and go to Sweep tab, define following:
    a. Parameter to Sweep = pin
    b. Start = 28
    c. Stop = 34
    d. Step-size = 0.2
4. Overall setup should look similar to the one shown in next snapshot



5. Click on Simulate icon to simulate the design and you shall see spectral lines with lot of arrows which indicates output power in each frequency component (i.e. harmonics) as input power is being swept. Insert a new rectangular plot and select “vout” to be added….select “Fundamental tone in dBm over all sweep values” to see output power vs. input power curve as shown in following snapshot. Insert a marker at pin of 32 dBm to see the output power matching to our optimization.



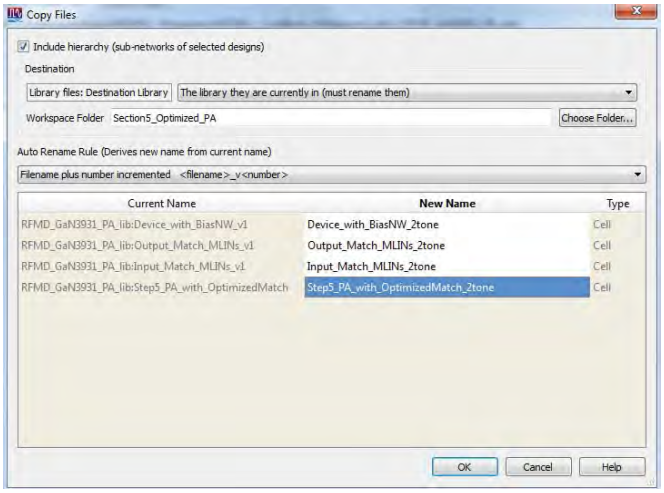
6. Insert a new rectangular plot and insert PAE to be plotted on the same as shown in next snapshot.



Step 7: 2-Tone Simulation of Power Amplifier

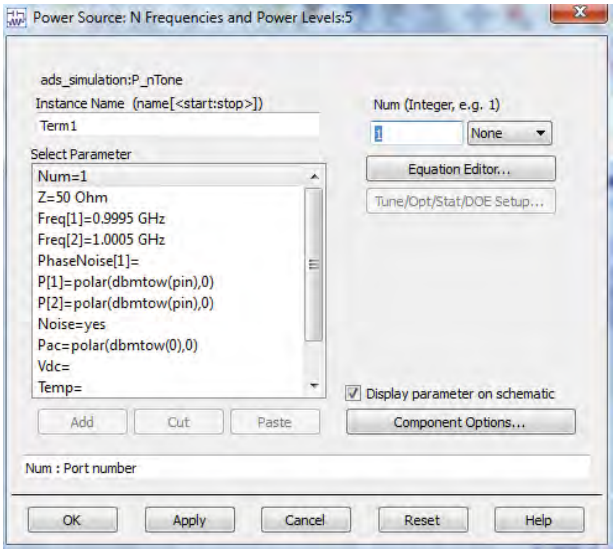
2-Tone simulations of amplifiers is recommended analysis to find out the IMD performance of the designed amplifier which also provides clear indication of ACPR (Adjacent Channel Power Rejection) in case of modulated signals.

1. From the ADS main window, right click on Step5_PA_with_OptimizedMatch and select Copy Cell
2. In the pop window, select Include Hierarchy and change the suffix from _v1 (or _v2) to "2tone" for all the designs as shown here

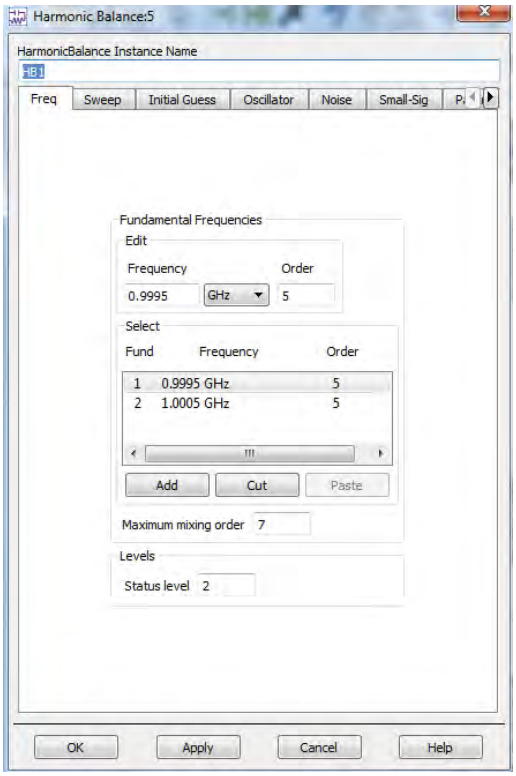


3. Click OK and double click Step5_PA_with_OptimizedMatch_2Tone to open the schematic.

4. Replace P_1Tone source to P_nTone source from Sources-Freq Domain library
5. Define 2 frequencies of **0.9995GHz and 1.0005GHz** and power as **polar(dbmtow(pin),0)**

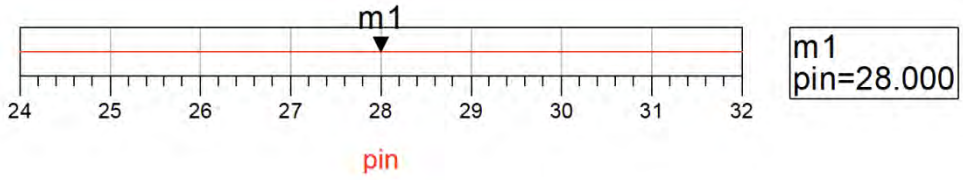


6. Click OK and double click on HB controller & specify following:
    a. Define these 2 frequencies as analysis frequencies.
    b. Change the Maximum mixing Order to see intermodulation products upto 7th order.
    c. Under Sweep tab, modify pin sweep start = 24, stop=32, step-size=1

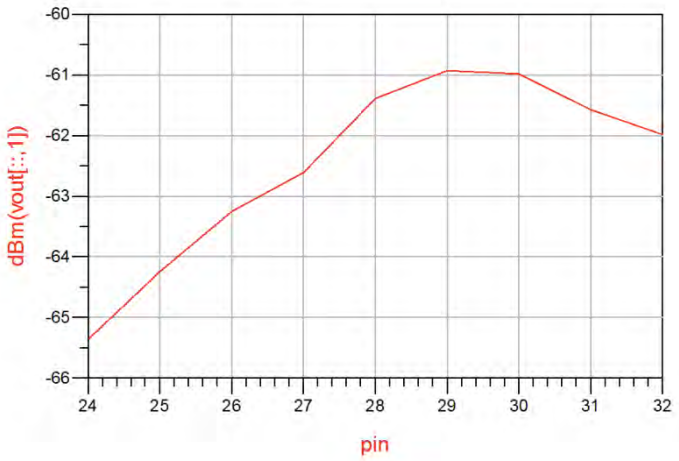


7. Delete the PAE equation as we don't need it during 2-Tone simulations.

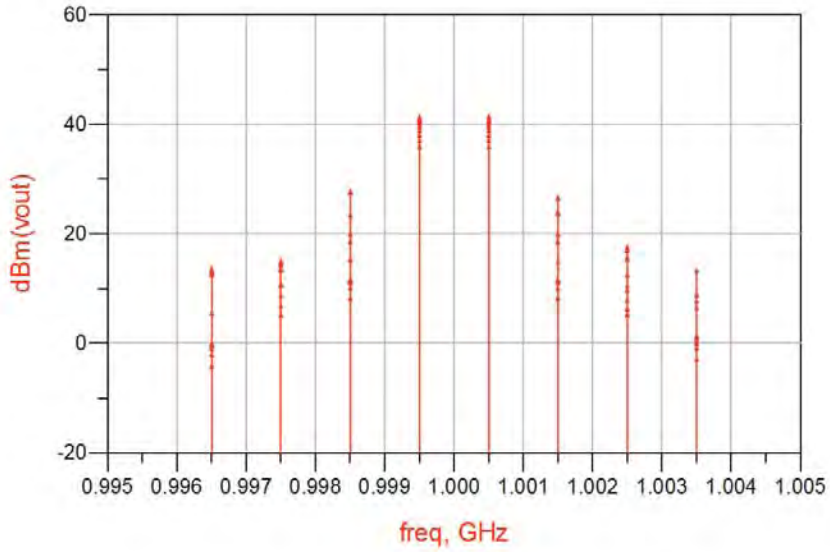
8. Click on Simulate icon to start simulation. On the data display, do following:
   a. Select **Insert->Slider** and click on data display, select **"pin"** and click on **>>Add>>** to see a slider plot as shown below



   b. Insert a new rectangular graph, select **vout** to be plotted….select fundamental tone in dBm over all sweep values from the available plotting options.

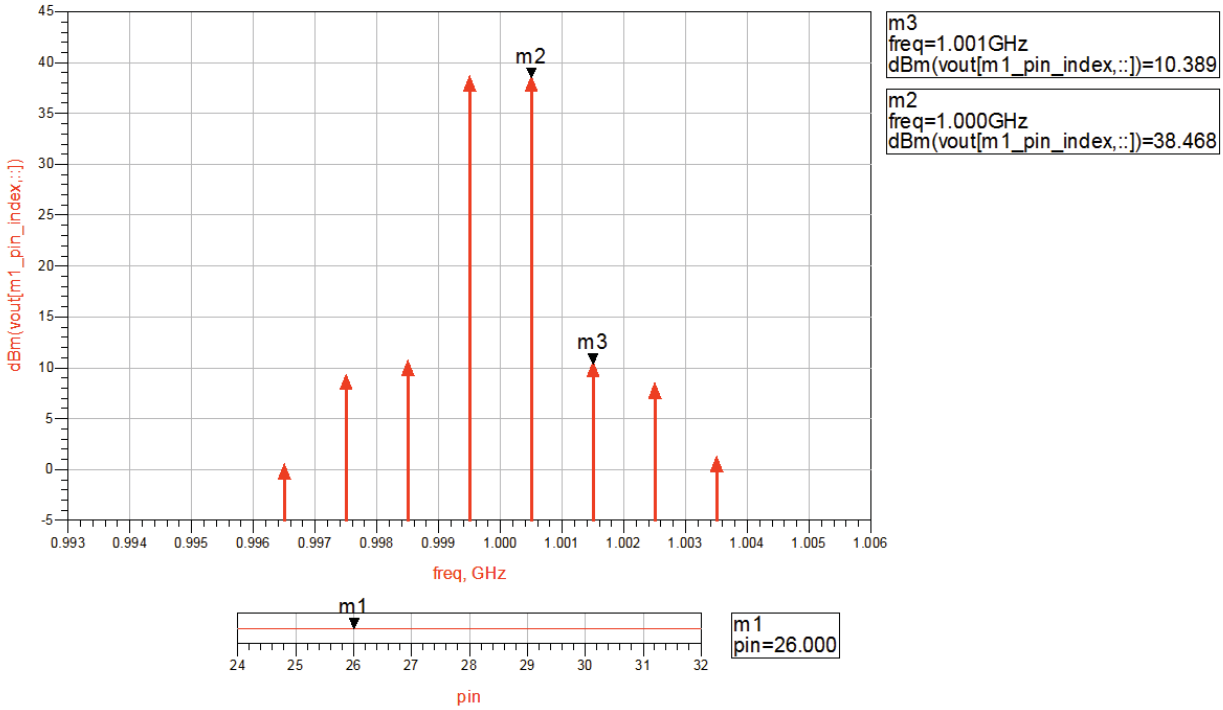


   c. Click on **Y-axis label** (that shows dBm(vout[::,1]) and remove the square brackets and its contents […] so that Y-axis label displays only **dBm(vout).** Zoom in to frequencies closer to 1 GHz using Graph zoom icon 
   d. Resulting graph should be similar to the one shown below

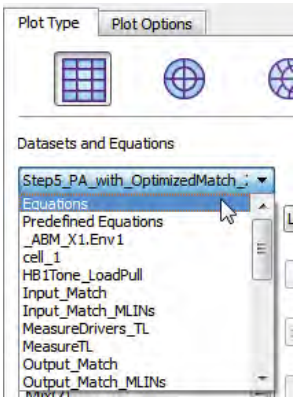


e. Click on Y-axis label and modify **dBm(vout) as dBm(vout[m1_pin_index,::])**….this allows designers to vary the slider and observe 2-tone results vary with the same…**try it…!!!**

f. With the pin value set at 26dBm (6dB below our 1-Tone input power), place 2 markers: One at Main tone on right side and then 1 marker on 3rd order product as shown below.



9. Insert following 2 equations on data display page to calculate PEP (Peak Envelope Power). Insert a table to plot PEP_Watts from Equations dataset as shown below.



Eqn P_Watts=dbmtow(m2)

Eqn PEP_Watts=4*P_Watts

freq	PEP_Watts
1.000 GHz	28.110

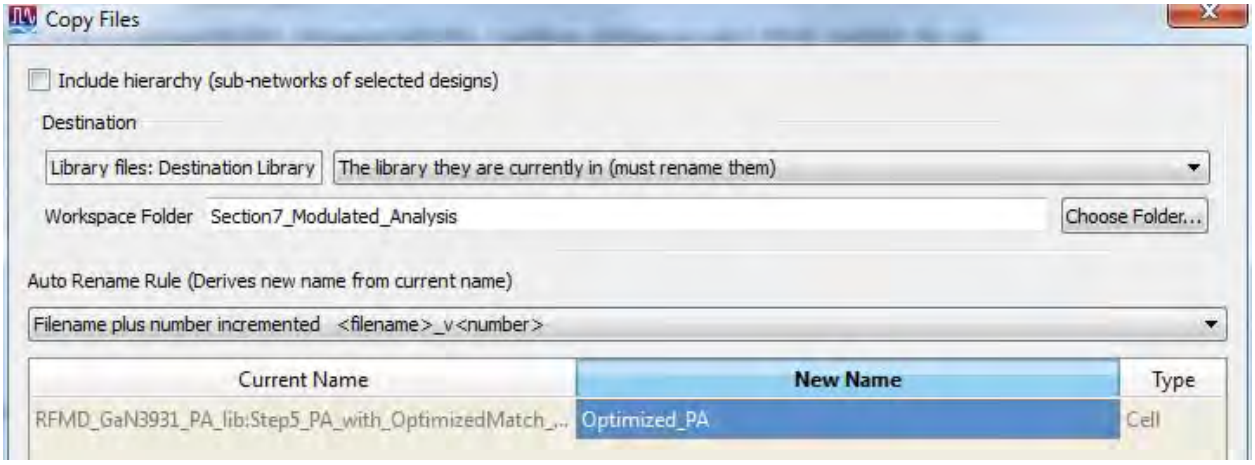
Please note m2 in dbmtow() equation is the marker name on the main frequency content. Change it as per your marker name in the data display.

Step 8: Modulated Signal Analysis of PA (Optional Step)

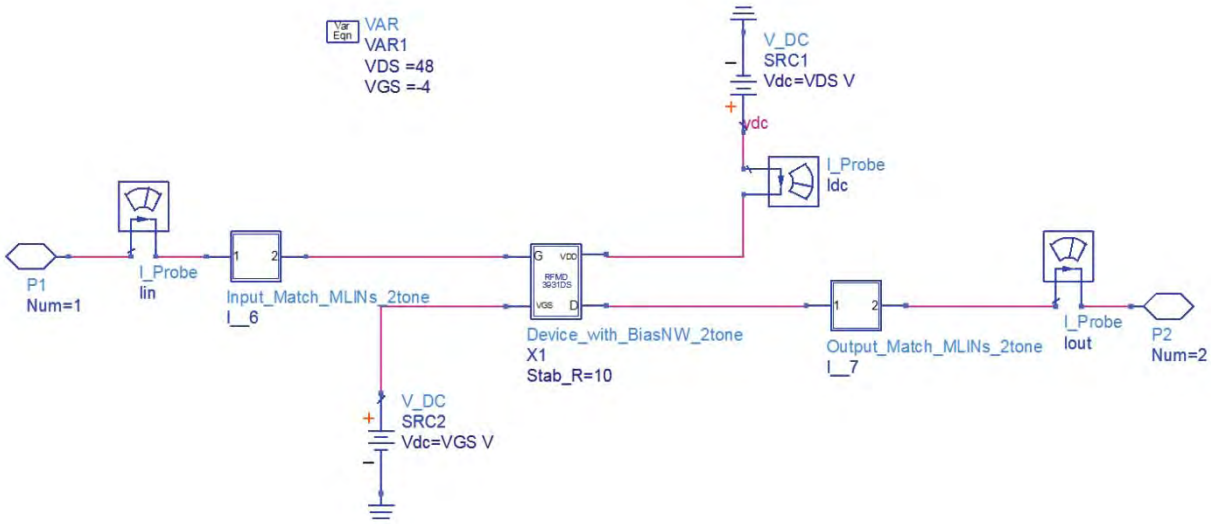
This step requires familiarity with Agilent PTolemy simulator; interested designers can read Chapter 16 and 17 of this book to get familiar with the same.

1. Right click on the Step5_PA_with_OptimizedMatch and click on Copy Cell….provide new name as Optimized_PA and click OK.

ss

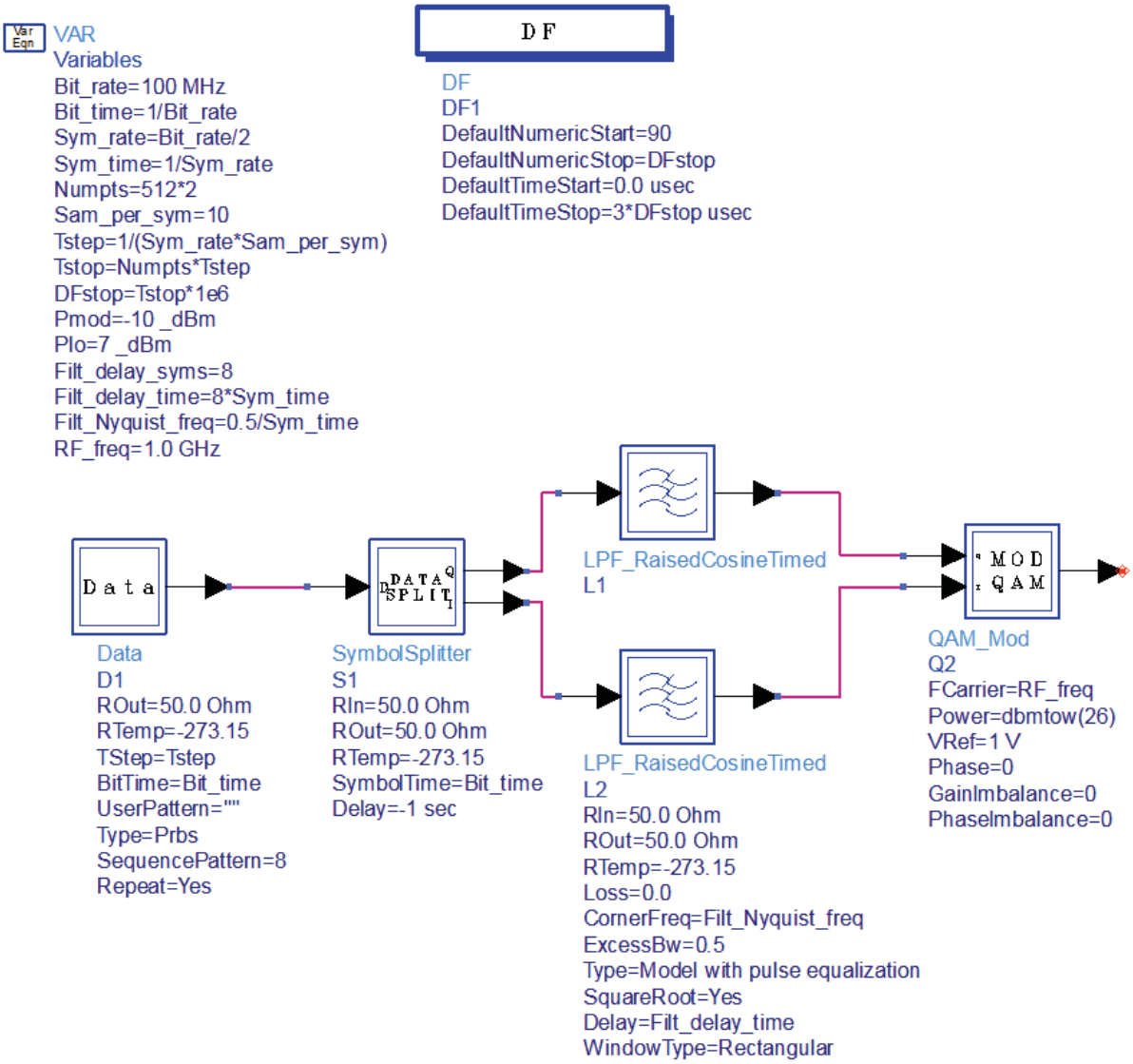


2. Delete simulation controller, source, termination, pin variable etc so that schematic looks as below.

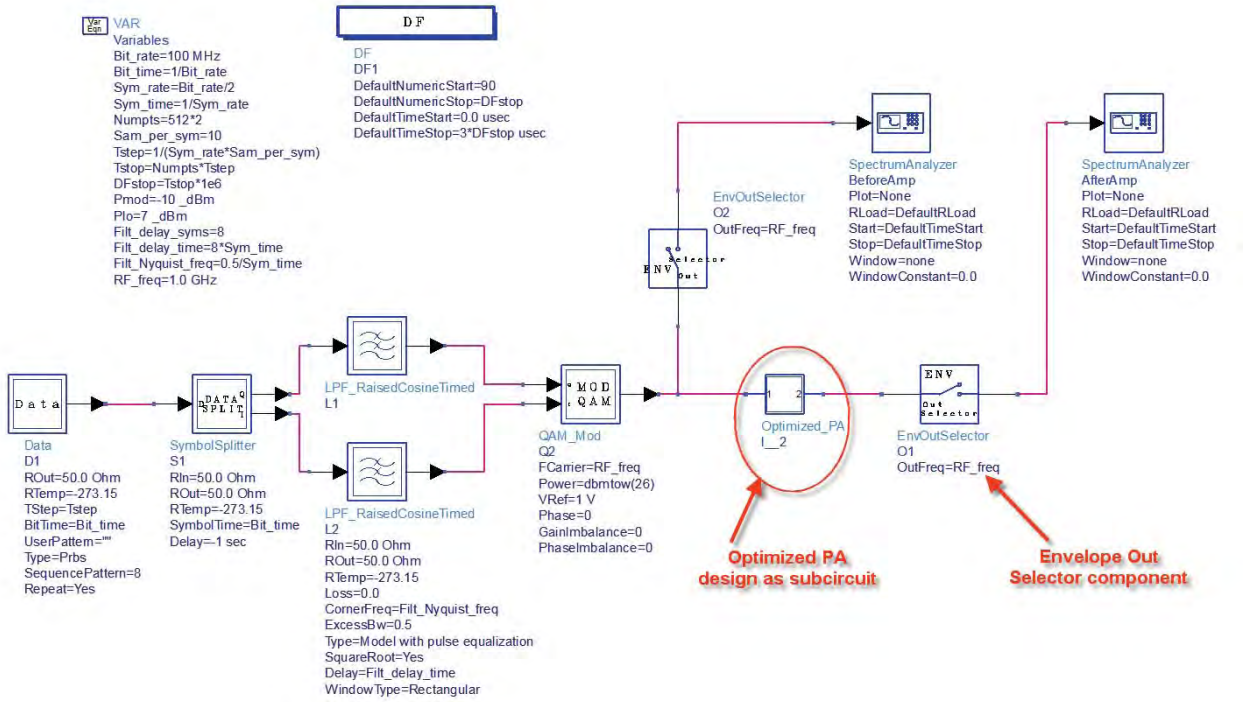


3. Open a new schematic cell with a name "QPSK_Modulator" and create Ptolemy design for a QPSK modulator as per method provided in Chapter 17…Only difference being here we shall use **Bit_rate=100MHz** as opposed to the one used in Chapter 17.

4. QPSK source schematic will look similar to the one shown below

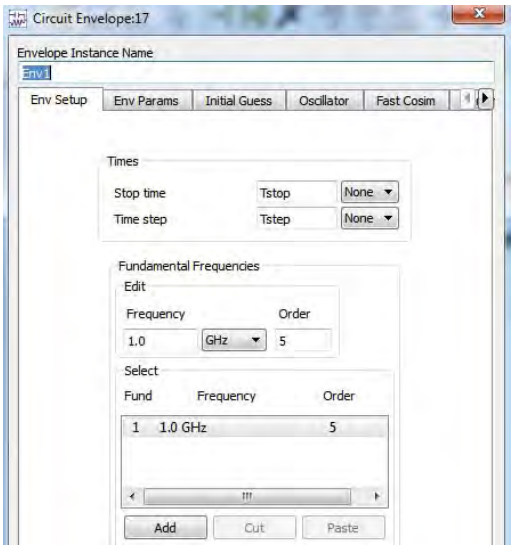


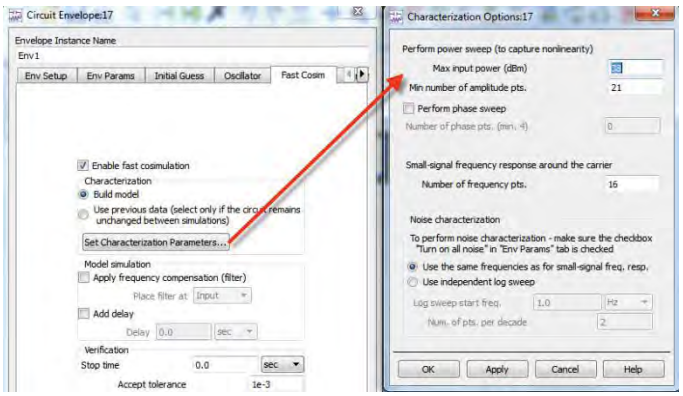
5. Drag and drop "Optimized_PA" design as subcircuit on this QPSK Modulator schematic as shown below. Modulator Power is kept as 26dBm.
6. Please note that Spectrum Analyzer sinks (available in Sinks library) are named as BeforeAmp and AfterAmp so that we can recognize the modulated spectrum in data display properly.
7. Place EnvOutSelector components before and after our PA subcircuit from Circuit Cosimulation library (this is a needed component for DSP & RF cosimulation as explained in Chapter 19 of this book)



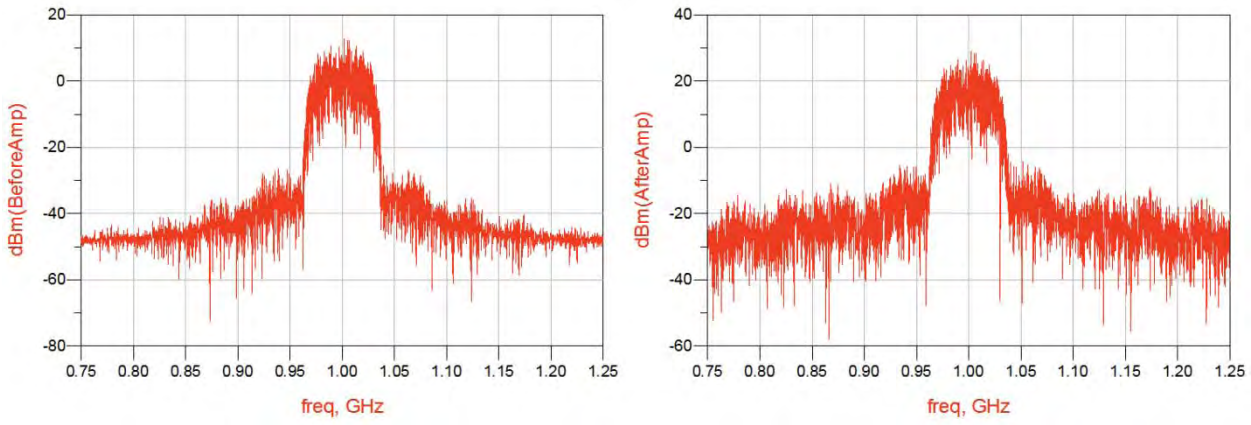
8. Push Inside **Optimized_PA** sub-circuit and place Envelope simulation controller from **Simulation-Envelope** library. Do following settings in Envelope Controller:
    a. Default frequency would be 1GHz matching to our requirement so we can leave as it is. Define Time Step = Tstep and Time Stop=Tstop as these are variables defined in Ptolemy design….make sure syntax is taken care of.
    b. From the **Fast Cosim** tab, select **"Enable Fast Cosim"**
    c. From Set Characterization Parameters, enter Max Input Power (dBm) = 38

Setting (b) and (c) allows a fast cosimulation of circuit level designs alongwith DSP networks.





9. Come back to PTolemy schematic and run simulation and plot 2 rectangular graphs in data display: One for BeforeAmp and one for AfterAmp modulated spectrums.



10. Insert 2 equations on data display page to compute integrated spectrum power:

Eqn PA_IP_Power=spec_power(dBm(BeforeAmp),0.95GHz,1.05GHz)

Eqn PA_OP_Power=spec_power(dBm(AfterAmp),0.95GHz,1.05GHz)

Note: 0.95 GHz and 1.05 GHz are the band edges as per our bandwidth requirements

11. Insert a Table and from Equations dataset select PA_IP_Power and PA_OP_Power as shown below

PA_IP_Power	PA_OP_Power
27.893	43.937

ACPR Calculation:

ACPR is a key metrics for Wireless modulated signals and this gives the power available in adjacent band of the operating PA.

Insert 4 more equations in data display as shown below. 1st two equations compute power is lower and upper adjacent band of the amplifier and next 2 equations compute ACPR in lower and upper sidebands.

Eqn Adj_Ch_Lower=spec_power(dBm(AfterAmp),0.85GHz,0.95GHz)

Eqn Adj_Ch_Upper=spec_power(dBm(AfterAmp),1.05GHz,1.15GHz)

Eqn ACPR_Lower=PA_OP_Power-Adj_Ch_Lower

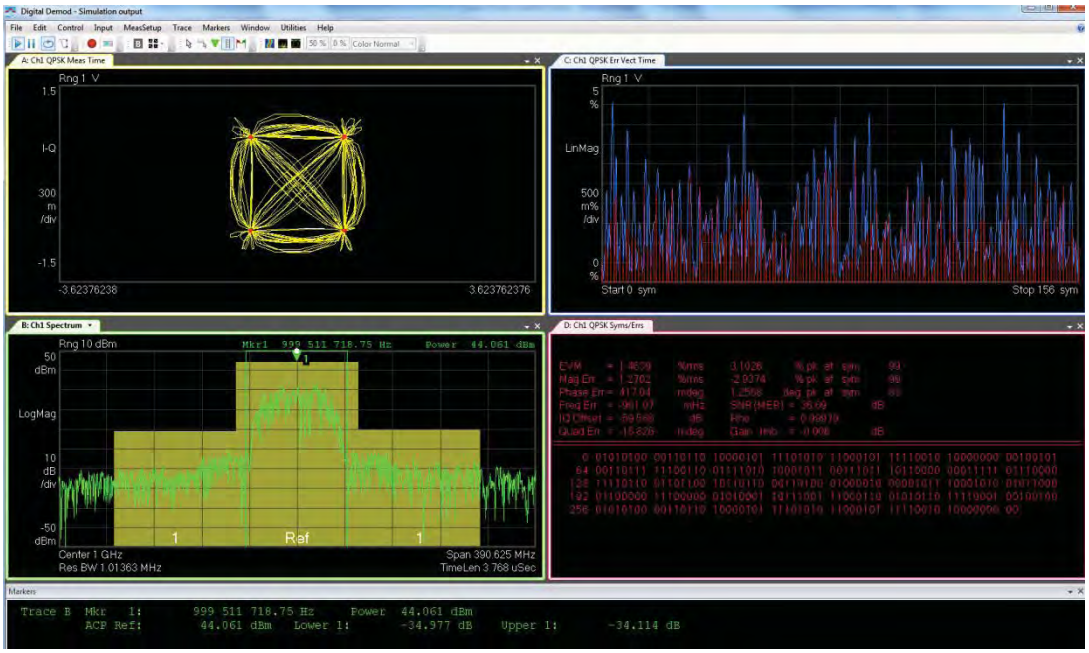
Eqn ACPR_Upper=PA_OP_Power-Adj_Ch_Upper

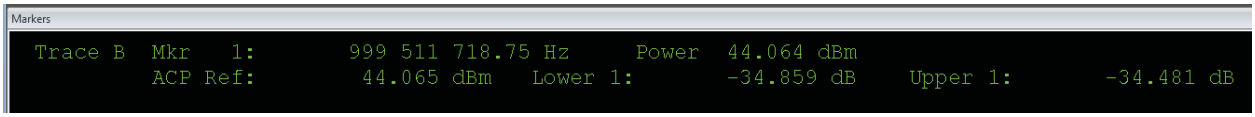
Plot ACPR lower and upper in the table which was inserted earlier and it should look similar to the shown below:

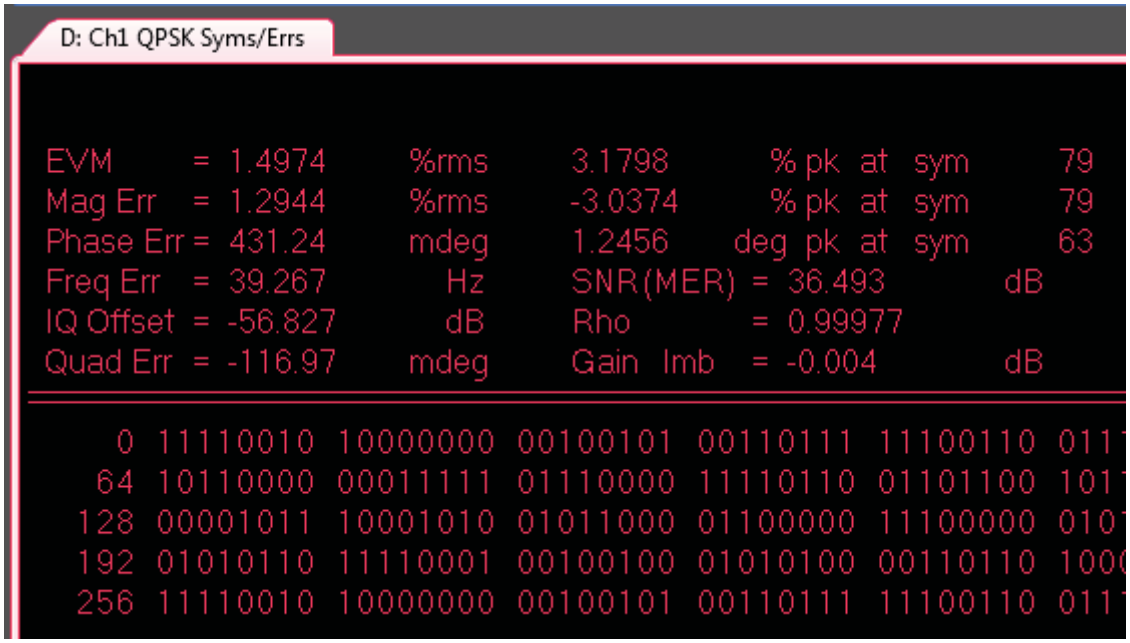
PA_IP_Power	PA_OP_Power	ACPR_Lower	ACPR_Upper
27.893	43.937	33.614	33.516

Using 89600B with ADS: (Optional)

If designers have license of VSA software (89600B) from Agilent then it can be used as interactive sink alongwith ADS PTolemy (run ADS in 32-bit mode), snapshot below shows power amplifier output with QPSK demodulator switched on and we can note that RMS EVM (Error Vector Magnitude) is @1.5% and ACPR is calculated as @34dBc matching to our calculation in ADS data display.







Chapter 16: Design of RF MEMS Switches

Reproduced with permission of Thiagarajar College of Engineering, Madurai, India

ADS Licenses Used:

- **Linear Simulation**
- **Momentum EM Simulator**
- **Layout**

Chapter 16: Design of RF MEMS Switches

Theory:

A RF switch is a two port network that is used for making or breaking a RF circuit. The traditional RF switches based solid state devices like diodes and transistors are limited in performance because of low power handling capability, high resistive losses etc. MEMS switches have recently become more popular because of higher better isolation, low losses and capability to operate at very high frequencies but with limited power handling capability and reducible dc voltage.

RF MEMS switches composed of a thin membrane which can be electro-statically actuated to the RF path using a DC bias voltage. There are two basic switches that are used in RF circuit design: The shunt switch and the series switch. The ideal series switch results in an open circuit in the transmission line when no bias voltage is applied (Up state position) and it results in a short circuit in the transmission line when the bias voltage is applied (Down state position). The shunt switch is placed in shunt between the transmission line and the ground. Depending on the applied bias voltage, it either leaves the transmission line undisturbed or connects it to the ground. Therefore the ideal shunt switch, which results in zero insertion loss when no bias is applied (Up state position) and infinite isolation when bias is applied (Down state position) as shown in figure 1.

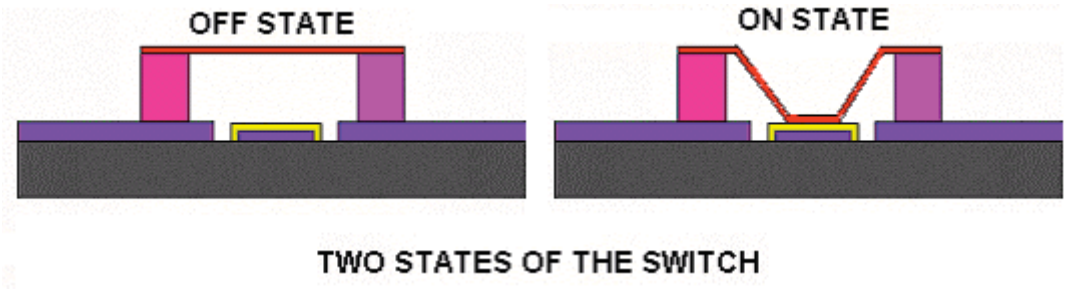


Fig1. Geometry of the RF MEMS Shunt Switch in ON and OFF State

A shunt capacitive MEMS switch consists of a thin metallic membrane bridge suspended over the center conductor of a coplanar wave guide or microstrip line and fixed at both ends to the ground conductors of the CPW line. Thus the tunable capacitor can be associated with the movable electrode suspended on the top of a fixed electrode. The suspended electrode is movable in the vertical direction normal to the substrate. The gap between the movable and the fixed electrodes can be adjusted electro-statically by

applying a tuning voltage resulting in a change in its capacitance. The electrostatic actuation is normally preferred over other actuation mechanisms because of its low power consumptions.

When an electric field is applied to a parallel plate system, the movable plate starts moving towards the fixed plate as the result of the electrostatic force. This force is distributed along the length of the movable plate and, when the threshold bias voltage is reached, the plate snaps down to the bottom plate and the applied voltage no longer controls the beam. The equilibrium between the electrostatic attracting force and the force at the supports holds only for a deflection smaller than one-third of the initial gap between them.

RF MEMS switches are extensively used for high performance switching applications at microwave and millimeter wave frequencies. They are used along with conventional components like filters, antennas etc to bring about frequency tuning. RF MEMS shunt switches are also used for the design of high performance Phase Shifters.

Objective:

To design MEMS shunt switch at 4 GHz and simulate the performance using ADS.

Design of MEMS Shunt Switch

1. Select an appropriate substrate of thickness (h) and dielectric constant (ε_r) for the design of the RF MEMS switch.
2. Synthesize the physical parameters (length & width) for the $\lambda/4$ CPW lines with impedance of Z_0. (Z_0 is the characteristic impedance of CPW line = 50Ω)
3. Determine the material (type of movable membrane, spring constant etc.) and physical parameters of the switch (length & width) of the switch so as to satisfy the given requirements of pull down voltage given by

$$V_p = \sqrt{\frac{8\mathrm{k}}{27\epsilon_o W w} g_o^3} \quad \mathrm{V}.$$

Where,

W is the width of the CPW center conductor

w is the width of the MEMS membrane

k is the spring constant of the MEMS membrane

g_0 is the initial gap between the CPW center conductor and the MEMS membrane

Layout Simulation using ADS:

1. Calculate the physical parameters of the transmission line from the electrical parameters like Z_0, Frequency and electrical length of $\lambda/4$ CPW line. The physical parameters can be synthesized using Linecalc of the ADS as shown in figure 25 for the following parameters.

Frequency	: 4 GHz
Substrate Thickness	: 675 microns
Dielectric Constant	: 11.7
Characteristic Impedance	: 50 Ω
Electrical Length	: 90^0

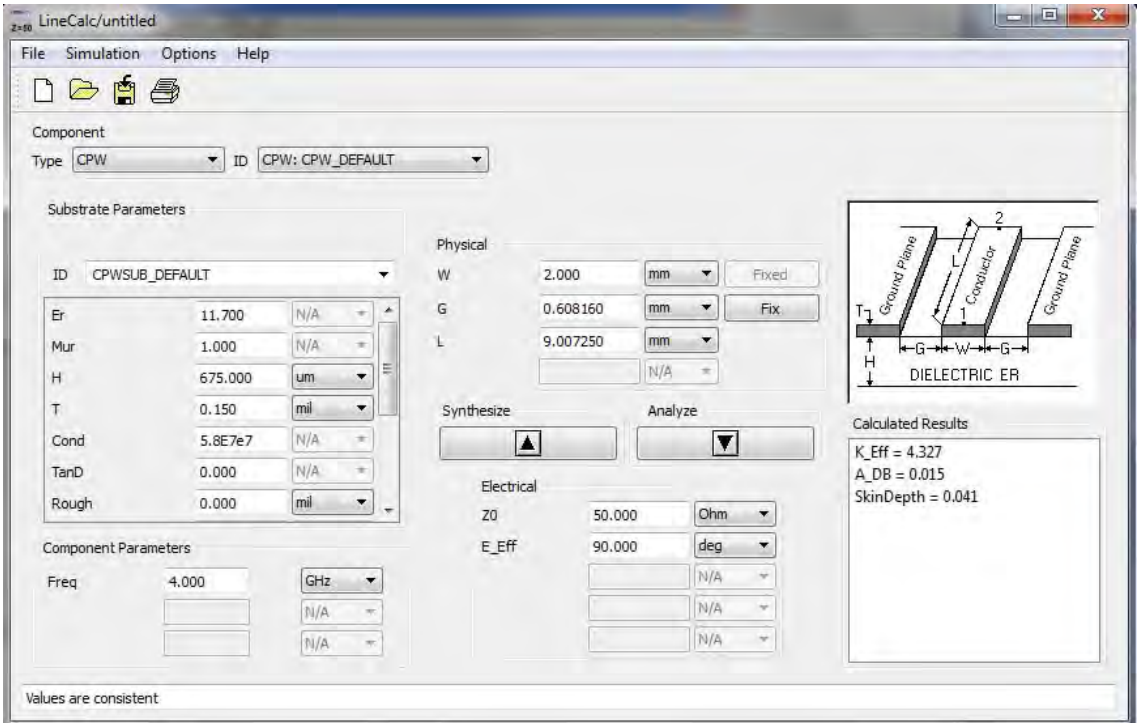


Fig2. Linecalc window of ADS showing the synthesis of physical parameters of the $\lambda/4$ CPW transmission line

2. The Physical parameters of the λ/4 CPW line for the 50Ω (Z_0) line for the frequency of 4 GHz as synthesized from Linecalc is given as follows.

   50Ω Line:

   Width = 2 mm
   Length = 9 mm
   Gap = 0.608mm

3. Calculate the physical parameters of the MEMS switch as given in the design step 3. For example let us chose the physical parameters of the MEMS Switch as follows so as to have a pull down voltage of 10 V.

   Length = 4 mm

   Width = 0.25 mm

   Thickness = 2 microns

   Initial gap = 15 microns

4. Create a model of the λ/4 CPW transmission line in the layout window of ADS. The Model can be created as follows. Click Insert>>rectangle and the cursor appears on the screen with dotted lines. Now click **Insert >> Coordinate Entry** and give the coordinates for the rectangle as shown in figure 3. For Example to create a rectangle of length and width 2 mm and 9 mm we may enter the coordinates as (0, 0) and (2, 9).

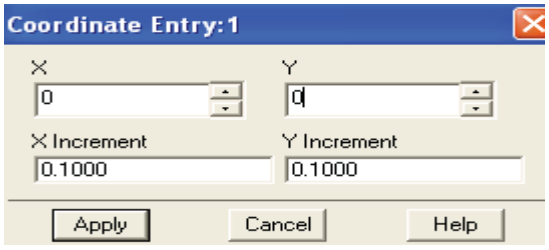


Fig3. Figure showing the coordinate entry dialog box

5. Alternatively we can use 3 coupled line model from **TLines-Multilayer** library and select ML3CTL_V which will allow widths of transmission line to be different. Enter parameters as below

   Length = 9 mm

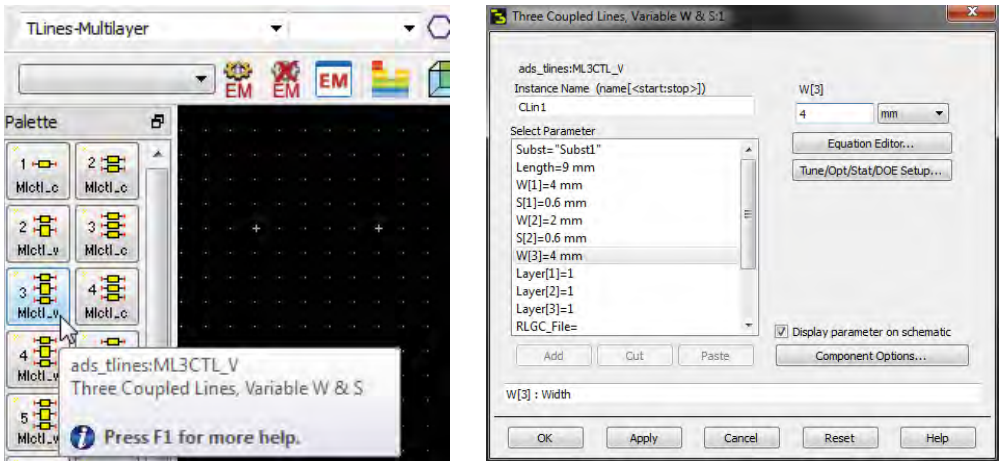
   W[1] = 4 mm (ground width)

   S[1] = 0.6 mm (spacing between conductor and ground)

   W[2] = 2 mm (main line width)

   S[2] = 0.6 mm (spacing between conductor and ground)

   W[3] = 4 mm (ground width)



6. Once done, layout will look as shown below

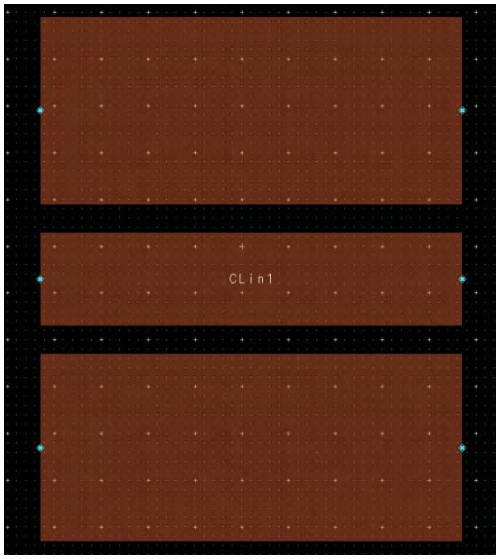


Fig4. Model of the CPW line in the layout window of ADS

7. Assign Pins for the CPW transmission line by clicking the Pin icon  and pasting them in the circuit. The Pins have to be assigned both on the center conductor and the ground plane of the CPW line. For easy remembrance, place Pin 1 and 2 on main line and then P3 & P4 on each side of P1 and P5 & P6 on each side of P2, this shall help us while doing the Port assignment during EM simulation setup.

8. Draw the next layer representing the post of the MEMS switch. To do this select the **hole** as Entry layer from the drawing layer drop down box as shown in the Fig5 below.

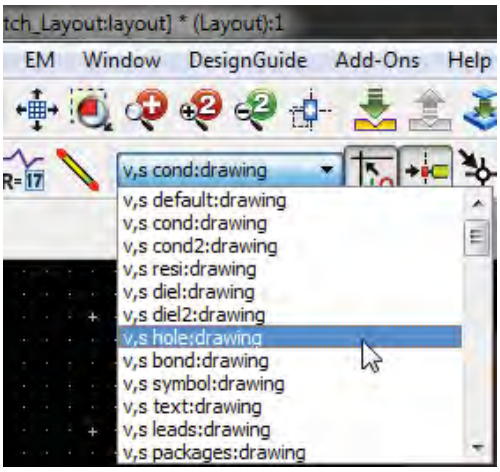


Fig5. Selection of hole layer using the dropdown box

9. Draw the posts for a dimension of width 0.15 and length 0.25 on the ground layers on each side of the center conductor as shown in Fig 6. These posts will provide the support the MEMS membrane in the switch. The posts should be placed in such a way that they lie in the two corners of the MEMS membrane which we shall draw later.

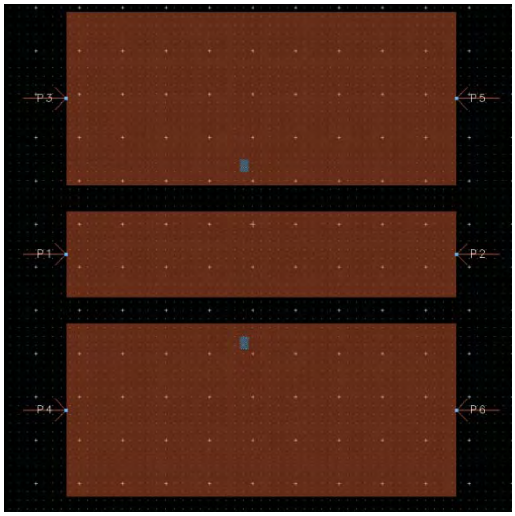


Fig6. Layout of the CPW line with the posts drawn using the resi layer

10. Draw the MEMS membrane layer by selecting the cond2 layer as in earlier step. The membrane is drawn above the post layer as shown in Fig 7 below.

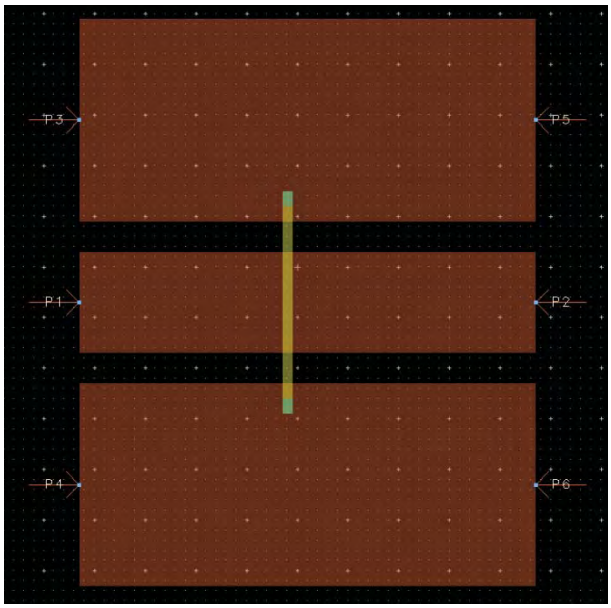
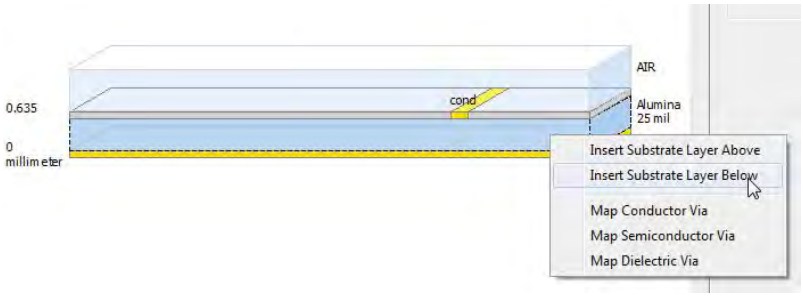
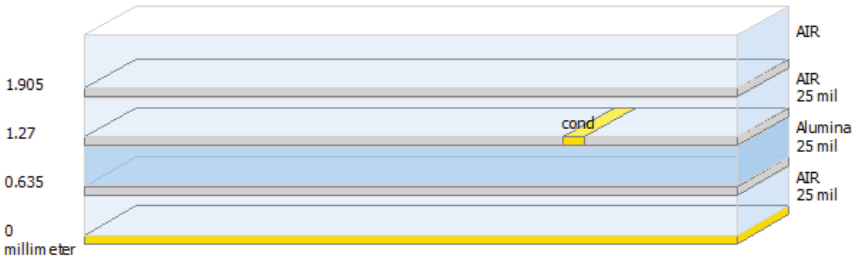


Fig7. Layout of the RF-MEMS Shunt Switch

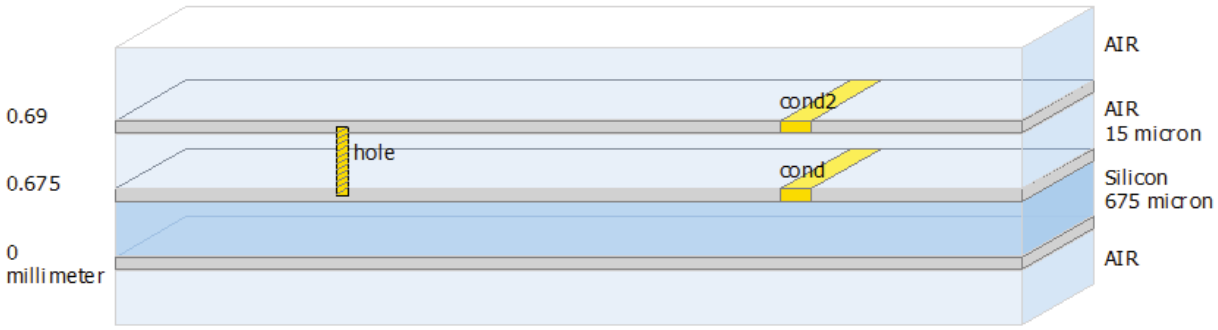
11. Click on Substrate Editor icon and select 25 mil Alumina template  . From the template of default substrate, right click and select Insert Substrate Layer Below and repeat the same action to Insert Substrate Layer Above



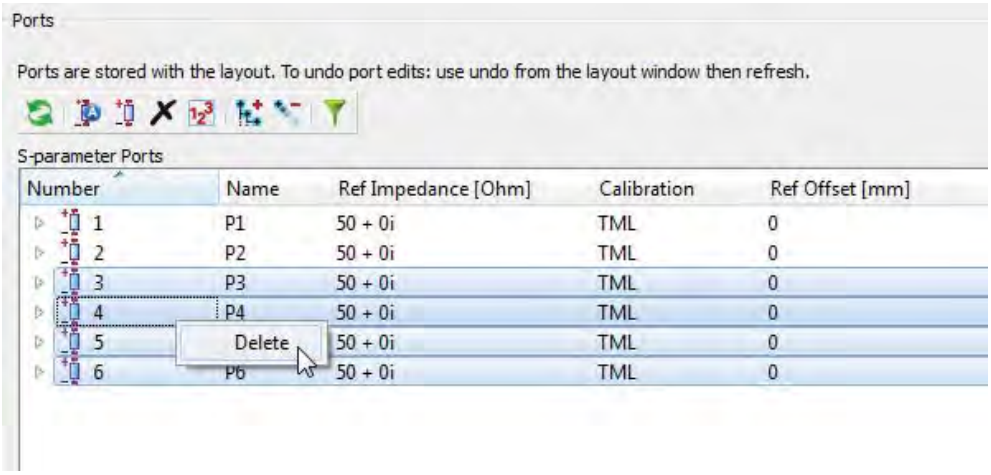
12. Change these 2 new substrate type to AIR (default definition available). Once done we shall have following type of dielectric stackup.



13. From this substrate, do following actions to prepare substrate for MEMS simulation:
    a. Change the AIR layer above cond to have thickness of 15 um to represent Up State of the Switch
    b. Right Click on top of the 15um AIR layer junction and select Map Conductor layer and make sure it is cond2 which is same layer which we have used to draw the Switch membrane in our layout
    c. Add a new Silicon dielectric with Er=11.7 as described in EM simulation chapter and set the height as 675um
    d. Right click on the Silicon substrate and select Map Conductor via and make sure the layer name is hole which is the same as we have used to draw the post in layout
    e. Right click on the bottom most Cover and select Delete Cover so that there is no ground at the bottom.



14. Open the EM Setup window and go to Ports option, select Port 3-6 right click and select delete so that these get removed from the Port list as shown below



15. Expand Port 1 and drag and drop P3 and P4 one by one on –Gnd terminal so that they are used as ground ports for Port1. Do the same thing for P5 and P6 and attach it to –Gnd of Port2. Once done it should be configured as shown below

Ports

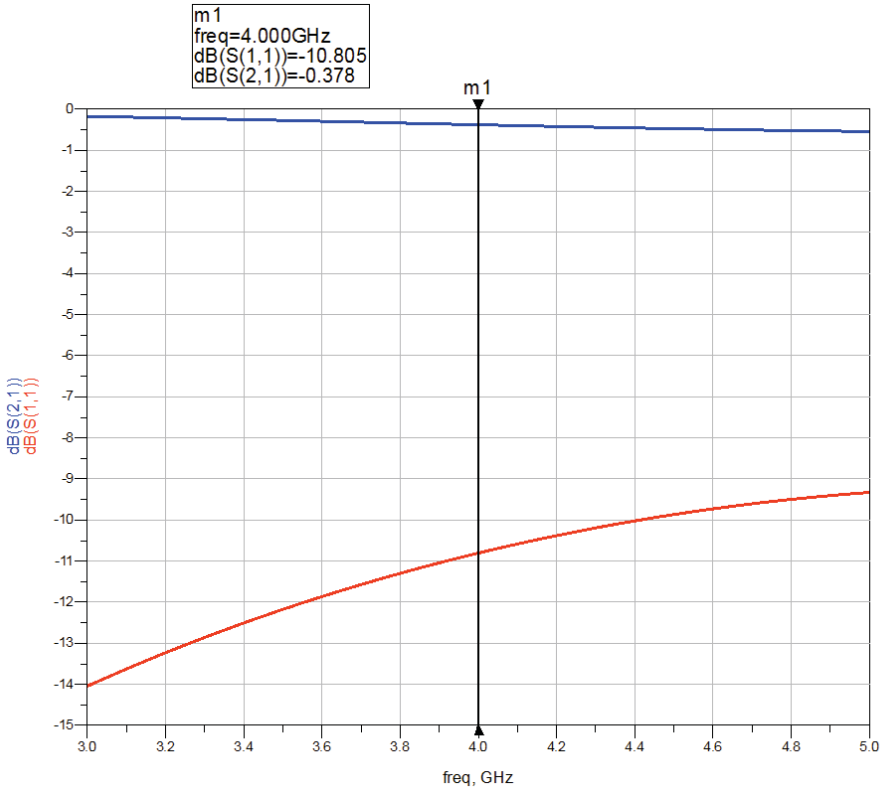
Ports are stored with the layout. To undo port edits: use undo from the layout window then refresh.

S-parameter Ports

Number	Name	Ref Impedance [Ohm]	Calibration	Ref Offset [mm]
1	P1	50 + 0i	TML	0
P1				
P3				
P4				
2	P2	50 + 0i	TML	0
P2				
P5				
P6				

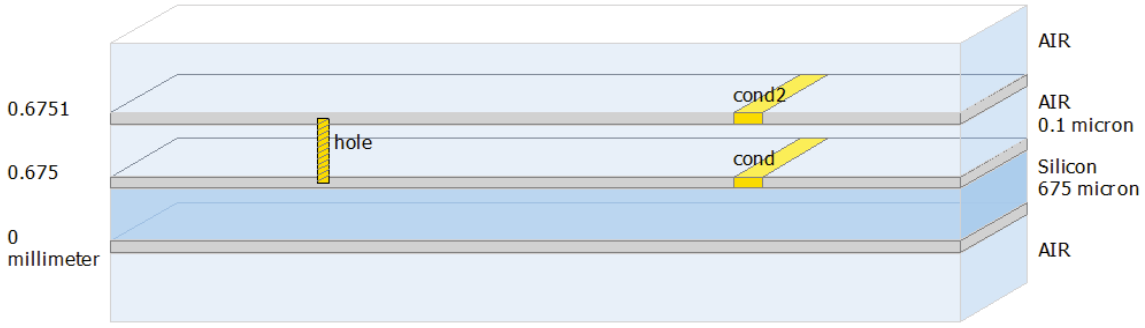
16. Go to Options->Mesh tab and switch on the Edge Mesh and set Cells/Wavelength=50.

17. Change the Simulation Mode to Momentum RF for faster simulation as the structure is smaller. Click on simulate button and plot the required response in data display window to see switch performance in Up State.

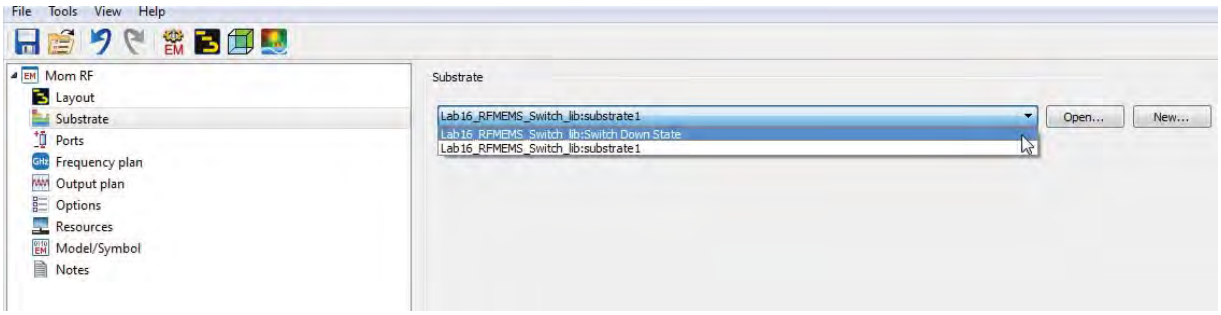


Switch Simulations in Down state:

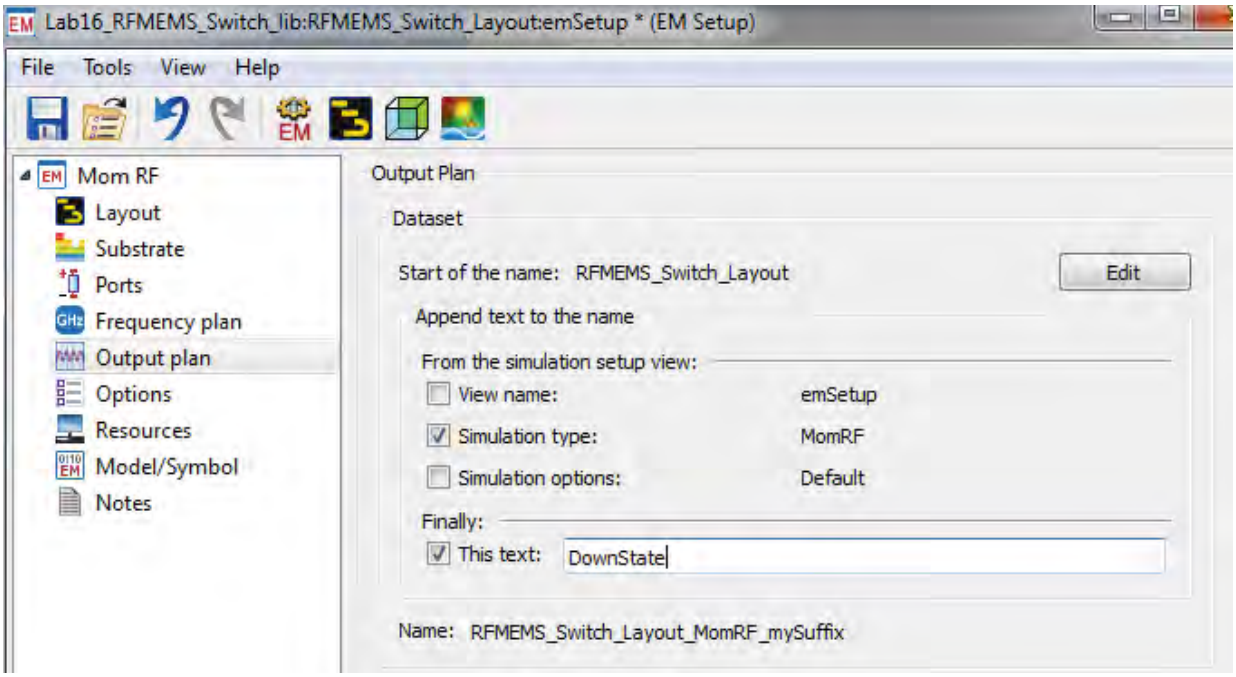
1. To simulate switch performance in down state, we need to change the thickness of AIR layer to something like 0.1um between cond and cond2 layers to represent the membrane movement due to applied voltage.
2. Open the substrate editor and go to File->Save As and save the substrate with new name e.g. Switch Down State as shown below



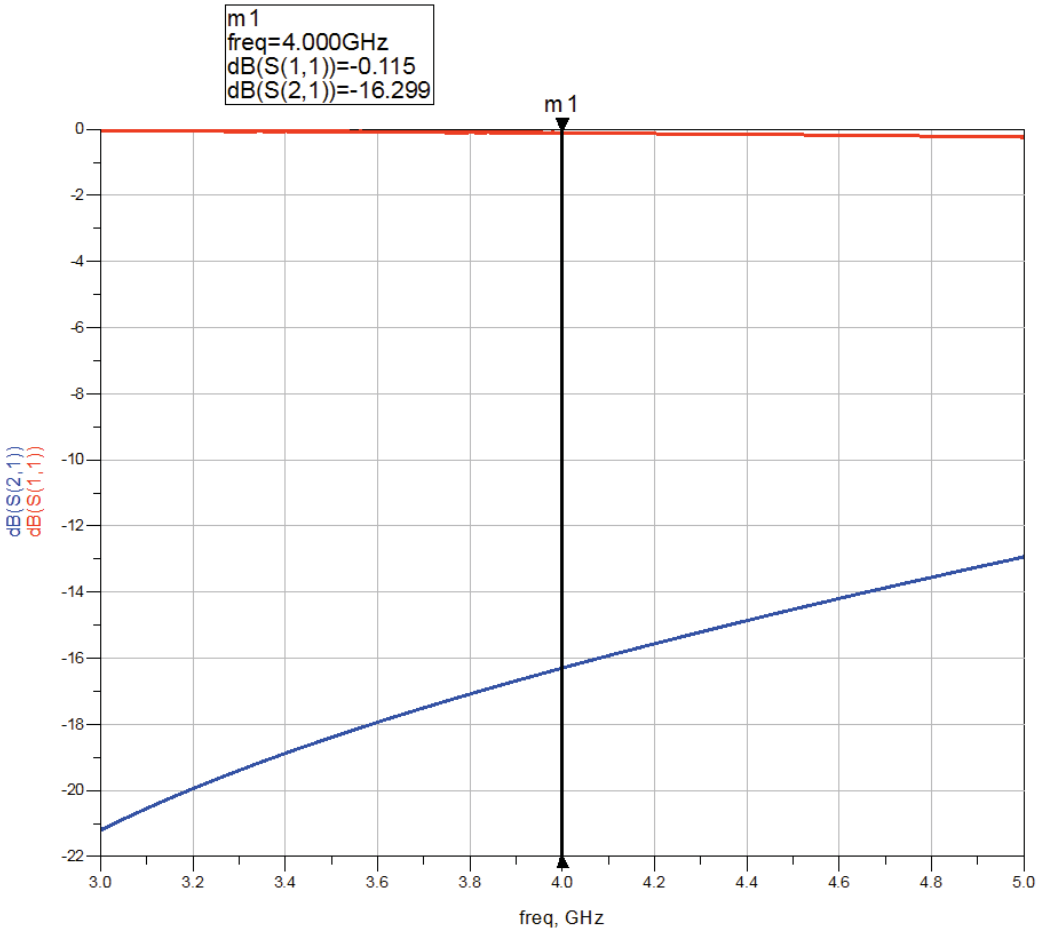
3. Go to the EM setup window and change the substrate to Switch State Down as shown below



4. From Output Plan, select “This text” and enter some name by which we shall recognize this new simulation dataset so that older dataset is not overwritten as shown below



5. Click on Simulate button and plot the required response to see switch's performance in down state as shown below



Results and Discussions:

It is observed from the results that the RF MEMS switch has an insertion loss (S_{21}) of -0.3 dB and return loss (S_{11}) of < -10 dB in the up state and the switch has an insertion loss (S_{21}) of -16 dB and return loss (S_{11}) of about -0.1 dB in the up state thus exhibiting decent switch characteristics, this performance can be further optimized if necessary.

Circuit Model of the MEMS Shunt Switch

Theory

The MEMS switch is modeled by two short sections of transmission lines and a lumped CLR model of the bridge with the capacitance having the up state down state values. The transmission line is of length (w/2) + l where l is the distance from the reference to the edge of the MEMS bridge. Typical values of the inductance are 7 to 8 pH and series resistance are .2 to .3 ohms.

The shunt impedance of the switch is given by

$$Z_s = R_s + j\omega L + 1/j\omega C$$

With $C = C_u$ or C_d depending on the position of the switch.

The LC series resonant frequency is given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

The impedance of the shunt switch can be approximated by

$$Z_s = \begin{cases} 1/j\omega C & \text{for } f << f_0 \\ R_s & \text{for } f = f_0 \\ j\omega L & \text{for } f >> f_0 \end{cases}$$

The CLR model behaves as a capacitor below the LC series resonant frequency and as an inductor above this frequency. At resonance the CLR model reduces to the series resistance of the MEMS bridge. The cutoff frequency is defined as the frequency where the ratio of the off and on impedance degrades to unity and is

$$F_c = 1/2\pi C_u R_s$$

Typical Design:

The Values of Capacitance is given by the formula

$$C = \varepsilon Ww/g$$

Where W is the width of the center Conductor of CPW = 2 mm

w is the width of the switch membrane = 0.25mm

g is the gap between the center conductor and MEMS membrane

Up state:

The Gap g = 15 microns

Thus C_{up} = 0.29 pF

Down State:

The Gap g = 15 microns

Thus C_{down} = 44 pF

Schematic Simulation using ADS

1. Open the Schematic window of ADS
2. From the TLines – Waveguide library select two CPW lines and place them on the schematic window. Double click on the transmission lines and give the physical parameters as follows

   Width = 2 mm

   Length = 4.5 mm

   Gap = 0.608mm

3. From the lumped components library select the appropriate components necessary for the equivalent circuit of the MEMS switch. Click on the necessary components and place them on the schematic window of ADS.

Create the circuit model of the MEMS switch on the schematic window with  appropriate lumped components and complete the circuit with wires.

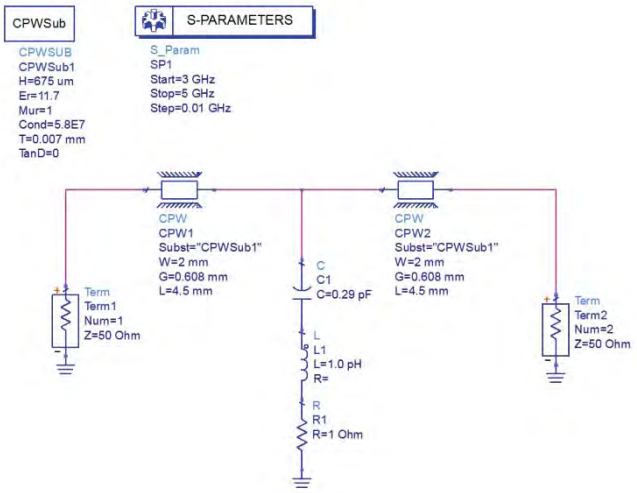
UP State

4. Double click on the lumped components values and enter their values. The values are calculated from the upstate and down state capacitances of the switch as given in design procedure. The values of resistance and inductance are the typical values obtained for a MEMS switch.

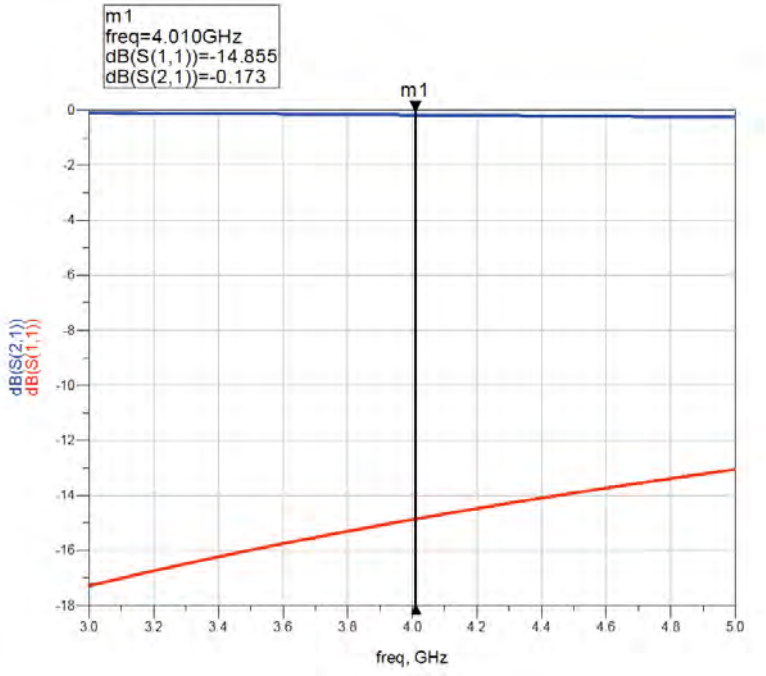
   Capacitance C = 0.29 pF

   Resistance R = 1 Ω

   Inductance L = 1 pH



5. Click on the Simulate icon and plot the required response in data display to observe the Switch characteristics in Up State



Down State

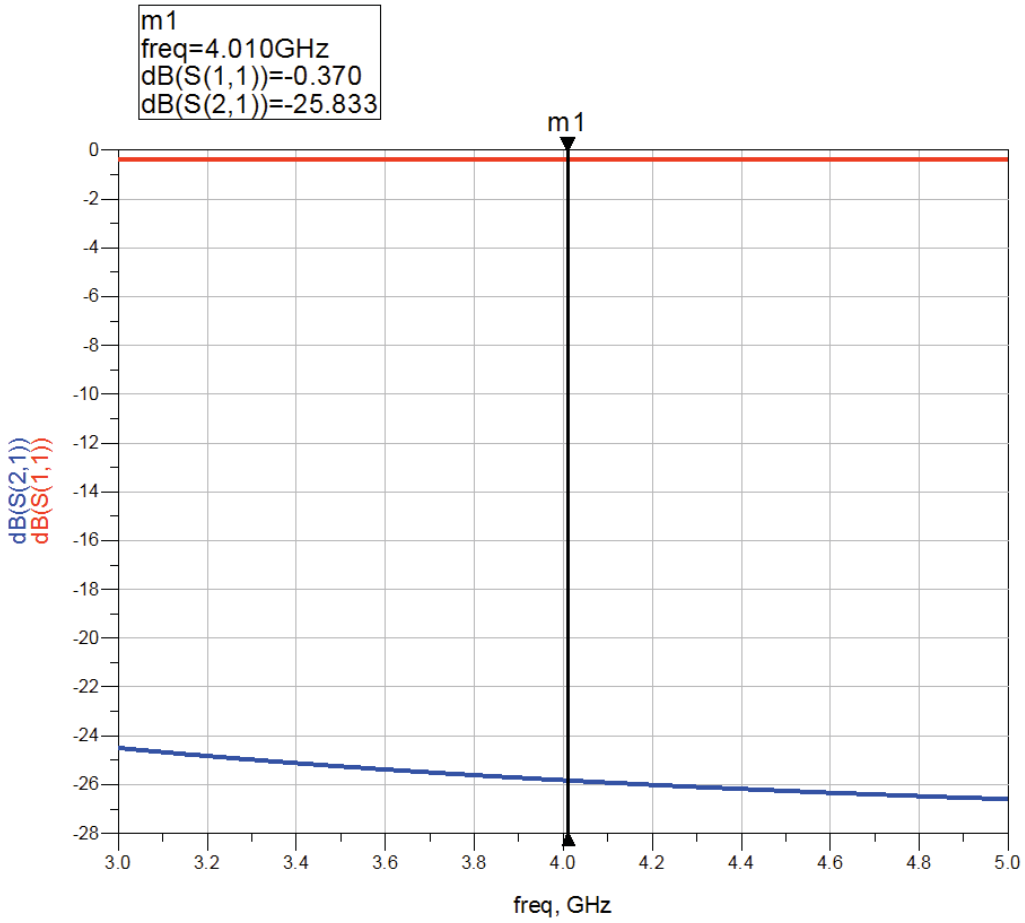
6. Double click on the lumped components values and enter their values.

   Capacitance C = 44 pF

   Resistance R = 1 Ω

   Inductance I = 1 pH

7. Simulate the circuit to view the scattering parameters of the switch in down state. The results of the simulation are shown in next figure.



Results and Discussions:

It is observed from the results that the MEMS switch circuit has an insertion loss (S_{21}) of -0.17 dB and return loss (S_{11}) of about -15 dB in the up state. The switch has an insertion loss (S_{21}) of -25 dB and return loss (S_{11}) of about -0.3 dB in the up state thus exhibiting good switch characteristics

Chapter 17: Getting Started with ADS PTolemy

ADS Licenses Used:

- **ADS PTolemy Simulator**

Chapter 17: Getting Started with ADS Ptolemy

The ADS Ptolemy software provides the simulation tools you need to evaluate and design modern communication systems products. Today's designs call for implementing DSP algorithms in an increasing number of portions in the total communications system path, from baseband processing to adaptive equalizers and phase-locked loops in the RF chain. Cosimulation with ADS RF and analog simulators can be performed from the same schematic.

Using the ADS Ptolemy simulator you can:

- Find the best design topology using state-of-the-art technology with more than 500 behavioral DSP and communication systems models
- Cosimulate with RF and analog simulators
- Integrate intellectual property from previous designs
- Reduce the time-to-market for your products

ADS Ptolemy features:

- Timed synchronous dataflow simulation
- Easy-to-use interface for adding and sharing custom models
- Interface to test instruments
- Data display with post-processing capability

Theory of Operation for ADS Ptolemy Simulation

- ADS Ptolemy provides signal processing simulation for ADS's specialized design environments. Each of these design environments capture a model of computation, called a domain, that has been optimized to simulate a subset of the communication signal path. ADS domains that are part of ADS Ptolemy, or can cosimulate with ADS Ptolemy are:

Domain	Simulation Technology	Controller	Application Area
Synchronous Dataflow (SDF)	Numeric dataflow	Data Flow	Synchronous multirate signal processing simulation
Timed Synchronous Dataflow (TSDF)	Timed dataflow	Data Flow	Baseband and RF functional simulation \ (e.g., antenna and propagation models, timed sources)
Circuit Envelope	Time- and frequency-domain analog	Envelope	Complex RF simulation
Transient	Time-domain analog	Transient	Baseband analog simulation

- In ADS Ptolemy, a complex system is specified as a hierarchical composition (nested tree structure) of simpler circuits. Each subnetwork is modeled by a domain. A subnetwork can internally use a different domain than that of its parent. In mixing domains, the key is to ensure that at the interface, the child subnetwork obeys the semantics of the parent domain.
- Thus, the key concept in ADS Ptolemy is to mix models of computation, implementation languages, and design styles, rather than trying to develop one, all-encompassing technique.

The rationale is that specialized design techniques are more useful to the system-level designer, and more amenable to a high-quality, high-level synthesis of hardware and software.

Synchronous Dataflow

Synchronous dataflow is a special case of the dataflow model of computation, which was developed by Dennis [1]. The specialization of the model of computation is to those dataflow graphs where the flow of control is completely predictable at compile time. It is a good match for synchronous signal processing systems, those with sample rates that are rational multiples of one another.

The SDF domain is suitable for fixed and adaptive digital filtering, in the time or frequency domains. It naturally supports multirate applications, and its rich component library includes polyphase FIR filters.

The ADS examples directories contain application examples that rely on SDF semantics. To view these examples, choose **File** > **Open** > **Example**; select the *DSP/dsp_demos_wrk* directory for one group of SDF examples.

SDF is a data-driven, statically scheduled domain in ADS Ptolemy. It is a direct implementation of the techniques given by Lee [2] [3]. *Data-driven* means that the availability of data at the inputs of a component enables it; components without any inputs are always enabled. *Statically scheduled* means that the firing order of the components is periodic and determined once during the start-up phase. It is a simulation domain, but the model of computation is the same as that used for bit-true simulation of synthesizable hardware.

Timed Synchronous Dataflow

Timed synchronous dataflow is an extension of SDF. TSDF adds a Timed data type (described in Using Data Types). For each token of the Timed type, both a time step and a carrier frequency must be resolved.

ADS examples directories contain numerous application examples that rely on TSDF semantics. To view these examples, choose **File** > **Open** > **Example**, a dialog box appears. Select the *DSP/ModemTimed_wrk* directory for one group of TSDF examples.

Note that the ADS Ptolemy (Pt) simulation time domain signals are different from those used for Circuit Envelope (CE) and Transient (T) simulation.

- For Pt, the simulation time step is not global and the input signals for different components may have a different time step. However, the simulation time step at each node of a design, once set at time=0, remains constant for the duration of the simulation. The time step is initially set by the time domain signal sources or numeric to timed converters. The time step in the data flow graph may be further changed due to upsample (decreases the time step by the upsampling factor) and/or down sample (increases the time step by the downsample factor) components. The time step associated with signals at the inputs of the timed sinks may or may not be the same as the one that was initiated by the timed sources or numeric to timed converters. This is dependent on any up or down sampling that may have occurred in the signal flow graph.
- For CE, the simulation time step is set by the simulation controller and is constant for the duration of the simulation. This is global for all components simulated in the design.
- For T, the simulation maximum time step is set by the simulation controller, but the actual simulation time step may vary for the duration of the simulation. This simulation time step is global for all components simulated in the design.

- For Pt, each timed sink that sends data to Data Display has time values that are specific to the individual sink and may or may not be the same as the time values associated with data from other timed sinks.
- For CE and T, all time domain data sent to Data Display has the same global time value.
- For CE, a time domain signal may have more than one carrier frequency associated with it concurrently. The carrier frequencies in the simulation are harmonically related to the frequencies defined in the CE controller and their translated values that result from nonlinear devices.
- For Pt, a time domain signal has only one characterization frequency associated with it. This characterization frequency is also typically the signal carrier frequency. However, the term *carrier frequency* is more typically used to mean the RF frequency at which signal information content is centered. A signal has one characterization frequency, but the signal represented may have information content centered at one or more carrier frequencies. This would occur when several RF bandpass signals at different carrier frequencies are combined to form one total composite RF signal containing the full information of the multiple carriers.

Example

Two RF signals and their summation:

Arf = Ai*cos(wa*t) - Aq*sin(wa*t) with carrier frequency wa

Brf = Bi*cos(wb*t) - Bq*sin(wb*t) with carrier frequency wb

The summation of these two signal, Crf, can be represented at one characterization frequency, wc, as follows:

Crf = Ci*cos(wc*t) - Cq*sin(wc*t) with carrier frequency wc

where

wc = max(wa, wb)

Ci = Ai + Bi*cos((wa-wb)*t) + Bq*sin((wa-wb)*t) (assuming wa > wb)

Cq = Aq - Bi*sin((wa-wb)*t) + Bq*cos((wa-wb)*t) (assuming wa > wb)

Time Step Resolution

In TSDF, each Timed arc has an associated time step. This time step specifies the time between each sample. Thus the sampling frequency for the envelope of a Timed arc is 1/time step.

The sampling frequency is propagated over the entire graph, including both Timed and numeric arcs. To calculate a time step, the SDF input and output numbers of tokens consumed/produced are used.

For any given SDF or TSDF component, the sampling frequency of the component is defined as the sampling frequency on any input (or output) divided by the consumption (or production) SDF parameter on that port. After a sampling frequency is derived for a given component, it is propagated to every port by multiplying the component's rate with the SDF parameter of the port. A sample rate inconsistency error message is returned if inconsistent sample rates are derived.

Carrier Frequency Resolution

Each Timed arc in a timed dataflow system has an associated carrier frequency (F_c). These F_c values are used when a conversion occurs between Timed and other data types, as well as by the Timed components.

The F_c has either a numerical value, which is greater than or equal to zero ($F_c \geq 0.0$), or is undefined (F_c = UNDEFINED). All Timed ports have an associated $F_c \geq 0.0$. Non-timed ports have an UNDEFINED F_c.

During simulation, all F_c values associated with all Timed ports are resolved by the simulator. The resolution algorithm begins by propagating the F_c specified by the user in the Timed sources parameter *Fcarrier* until all ports have their associated F_c. At times, the user may have specified incompatible carrier frequencies, and ADS Ptolemy will return an error message.
In the feedforward designs, the algorithm will converge quickly to a unique solution. In the designs with feedback, the algorithm takes additional steps to resolve the carrier frequency at all pins.
For feedback paths, a default F_c is assigned by the simulator. This default F_c is then propagated until the F_c converges on the feedback path. This F_c is occasionally non-unique. To specify a unique value, use the SetFc Timed component.

Input/Output Resistance

Resistors can be used with timed components. Resistors provide a means to support analog/RF component signal processing. They provide definition of analog/RF input and output resistance, additive resistive Gaussian thermal (Johnson) noise, and power-level definition for time-domain signals.
Though resistors are circuit components, they are used in the data flow graph by defining their inputs from the outputs of connected TSDF components and their outputs at connected TSDF component inputs.

Representation of Data Types

ADS Ptolemy schematics contain component stems with different colors and thicknesses. Each component input and output pin has an associated data type, and each type is represented in the component symbol by use of a color code and a thickness of stem. And, each component stem may have single or multiple arrowheads. The following table lists the data types.

Component Stem Color and Thickness

Data Type	Stem Color	Stem Thickness
Scalar Fixed Point	Magenta	Thin
Scalar Floating Point (Real)	Blue	Thin
Scalar Integer	Orange	Thin
Scalar Complex	Green	Thin
Matrix Fixed Point	Magenta	Thick
Matrix Floating Point (Real)	Blue	Thick
Matrix Integer	Orange	Thick
Matrix Complex	Green	Thick
Timed	Black	Thin
Any Type	Red	Thin

How to set Tstep in a TSDF simulation

Tstep is the single most important factor in a TSDF simulation. The Tstep setting will determine the effective analysis BW of the simulation. All signals present within the analysis BW will determine the result in a simulation, including aliased waveforms.

For band pass signal types, the analysis BW will be equal to 1/Tstep For Base band signal types the analysis BW will be equal to 1/(2*Tstep). If you think about this from a Nyquist point of view, the Tstep must be set, at a maximum, to ½ of the shortest period signal in the simulation. Since Ptolemy only treats the complex envelope of a signal, the Tstep is always set relative to the BW of the complex envelope and not the carrier frequency. So, thinking in terms of the signal being analyzed, Tstep=1/(EnvBW) for band pass signals and Tstep=2/(BBBW) for base band signals, where EnvBW is the BW of the complex envelope of the modulated signal being analyzed and BBBW is the BW of the base band signal being analyzed. As a rule of thumb, many simulations are over sampled beyond to simple Nyquist rate.

In both modulated and base band cases, we are sampling the base band portion or complex envelope of the waveform and not the carrier. In the modulated case the base band BW contains real and imaginary signal information, or I and Q, while the non-modulated case typically we are sampling only a real valued signal.

For a more thorough treatment of the TSDF simulation domain and it's signal types please refer to the online manual set for ADS. The appropriate information can be found in chapter 9 of the Agilent Ptolemy Simulation manual as well as the Introduction section of the Timed Non-Linear, Timed Linear, and Timed Filter sections of Signal Processing Components manual.

Signal Conversions: How to go from SDF to TSDF and vice-versa

The interface between SDF and TSDF is analogous to the interface formed by DACs and ADCs in a real system. Everything between the DAC and ADC in a transceiver (with the DAC being in the TX path while the ADC is in the RX path) is analog/RF while everything before the DAC and everything after the ADC is typically digital, representing discrete signal processing. So, considering a typical simulation of a complete transceiver in Ptolemy, the purely digital and algorithmic portions of the design will be treated in SDF while the analog/RF portions will be in TSDF.

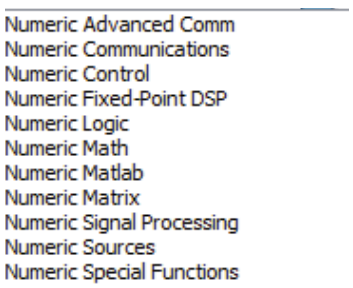
There are many ways to convert Timed waveforms into SDF (or numeric) waveforms and vice versa. In the case of band pass (or modulated) signals, conversion has to take place in such a way as to keep the complex nature of the signal intact. The following components depict typical waveform conversions for going from Timed to Numeric and then Numeric to Timed:

ADS PTolemy Component Libraries:

Key component libraries of ADS Ptolemy are

1. Numeric

Numeric libraries provides all the necessary blocks for performing SDF simulations i.e. that is classic DSP mode of operation in ADS. There are various categories as shown in the snapshot here which are mostly self explanatory.



2. Timed

Timed library blocks enable designers to perform simulations based on TSDF i.e. RF or RF envelope simulations for Mixed Signal System simulations

Timed Filters
Timed Linear
Timed Modem
Timed Nonlinear
Timed RF Subsystems
Timed Sources

3. Signal Converters

Signal Converter libraries provides the necessary blocks to perform Data type convertors e.g. Float to Timed, Rect to Complex etc..

4. Sinks

Sinks library provides variety of data collection sinks such as Timed, Spectrum Analyzer, EVM, BER etc

5. Interactive Controls and Displays

ADS provide real time interactive controls and display options which can be used by designers to plot data on-the-go. These displays are based on TCL (Terminal Control Language) scripting.

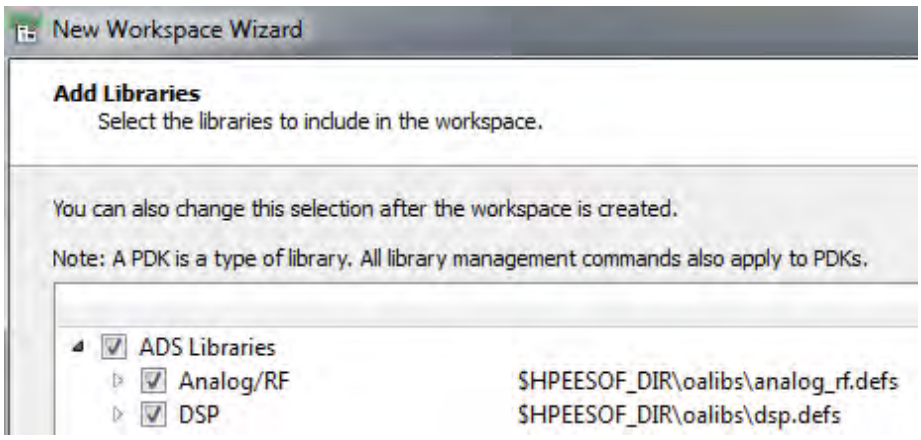
6. Instruments

Instruments library provide source and sink components for various Agilent instruments such as Vector Signal Generators, Logic Analyzers, Scopes, VSA etc. Using these links we can transfer the data from ADS to Instruments & vice-versa through ADS Connection Manager Server software.

Lab 1: Getting Started with Numeric (DSP / SDF) simulations

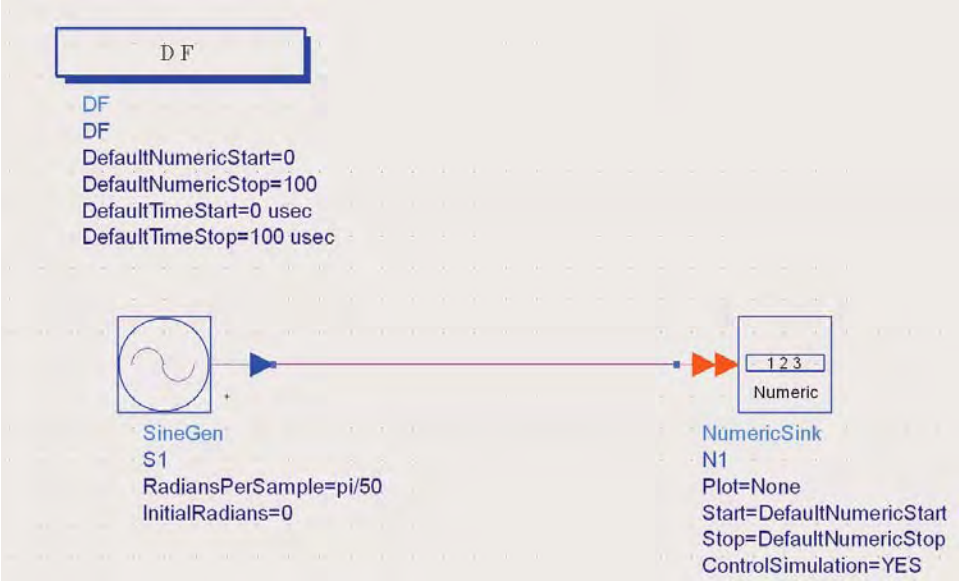
Objective of this first lab to understandg some of the basic use model of ADS PTolemy and understand the concept to using Sink, Interactive Control and Displays etc.

1. Create a new workspace from File->New->Workspace and make sure DSP library is selected in the library selection window as shown below

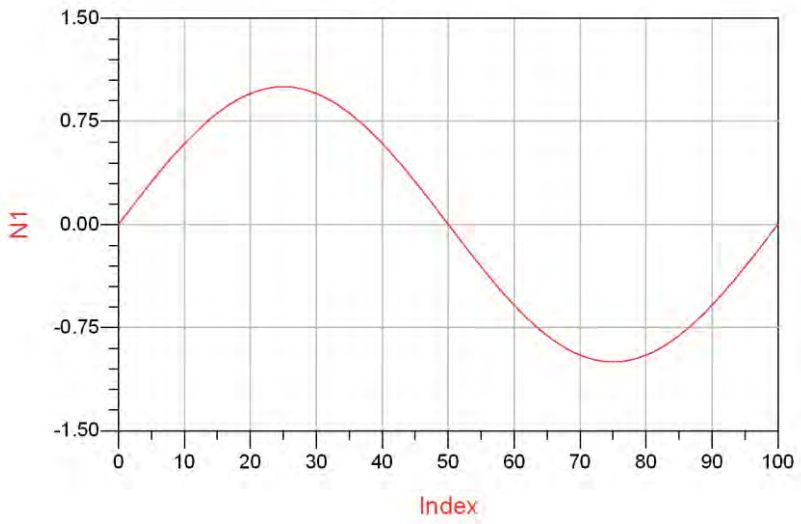


2. Open a new schematic cell and place following components from library

a. SineGen source from Numeric Sources library (note the blue colour stem which indicates that the output from SineGen would be of Float data type)
b. Numeric Sink from Sinks library
c. DF (Data Flow / PTolemy) controller from Common Components library. Note that DF controller has Numeric Start, Stop & Time Start, Stop which shall be used as per the blocks in the design. Currently there are no Timed block in our design hence Time start & stop will be ignored.

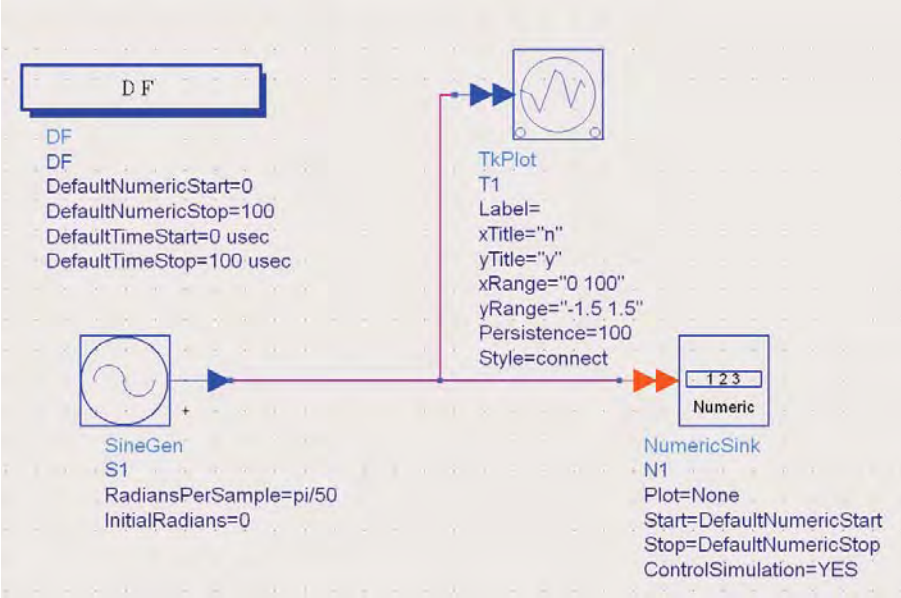


3. Simulate the design by pressing F7 or Simulate icon
4. Insert a rectangular graph in the data display window and select N1 (name of the numeric sink, designers can rename the sink as they need) data to plot to observe the data as shown below. Please note that Y-axis limits can be changed to +1.5 to -1.5 as shown below.

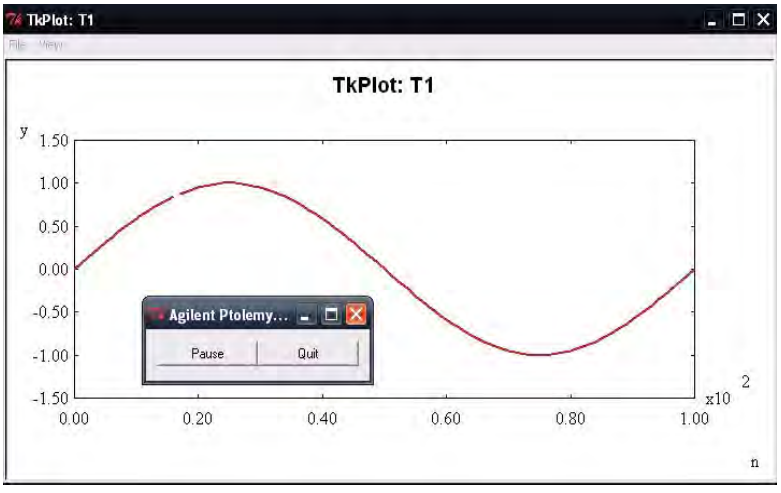


Notice the X-axis on the graph which mentioned Index (which is data sample index as per the RadiansPerSample setting in SineGen source)

5. Insert a TkPlot from Interactive Control and Displays library and connect it to the SineGen source as shown below. TkPlot is used to see the data on real time basis which is very useful before running a long simulation to make sure design is providing the expected results. Change the yRange on TkPlot to -1.5 1.5 to scale the Y-axis of the display window.



6. Click in Simulate icon and observe the TkPlot which will run in continuous mode till we click on Quit button as shown below. Once we click on Quit, normal data display with N1 result will appear.



Please note TkPlots are qualitative plots and not quantitative hence we can't place markers etc for readout.

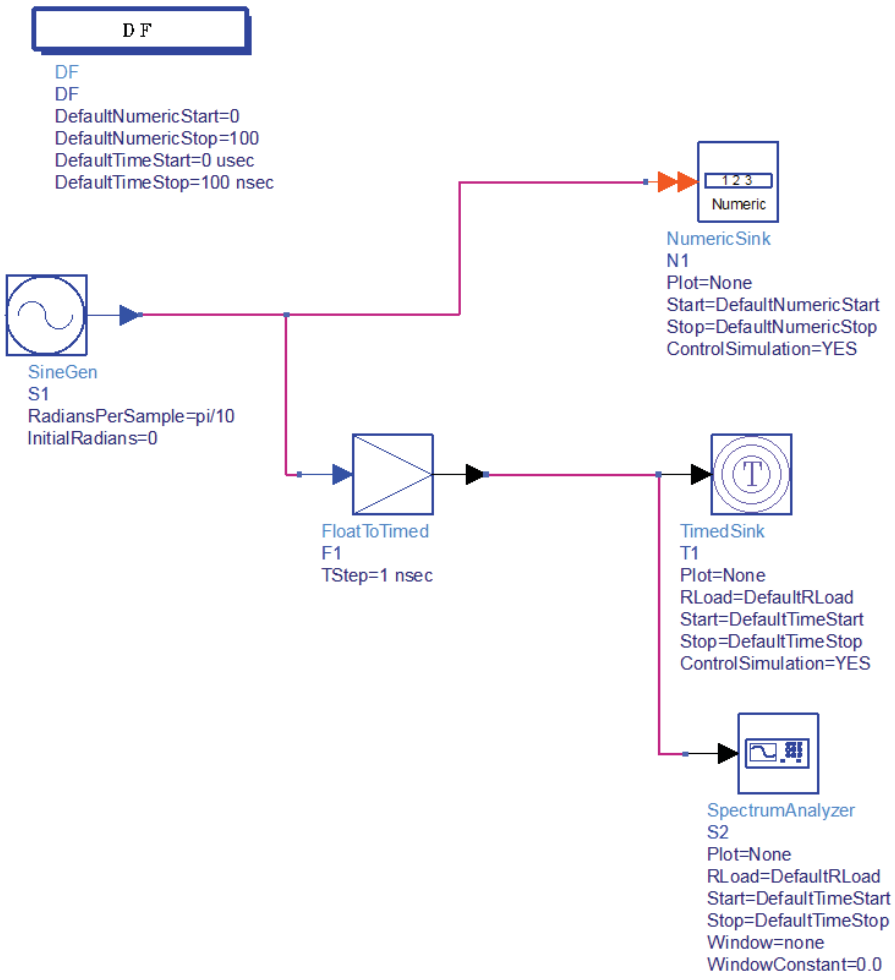
7. Now let us understand how signal / domain conversion can be performed to form a very basic mixed mode simulation. Place following components in the design:

    a. Insert Timed sink and Spectrum Analyzer sink from Sinks library
    b. Insert Float to Timed converter from Signal converter library.

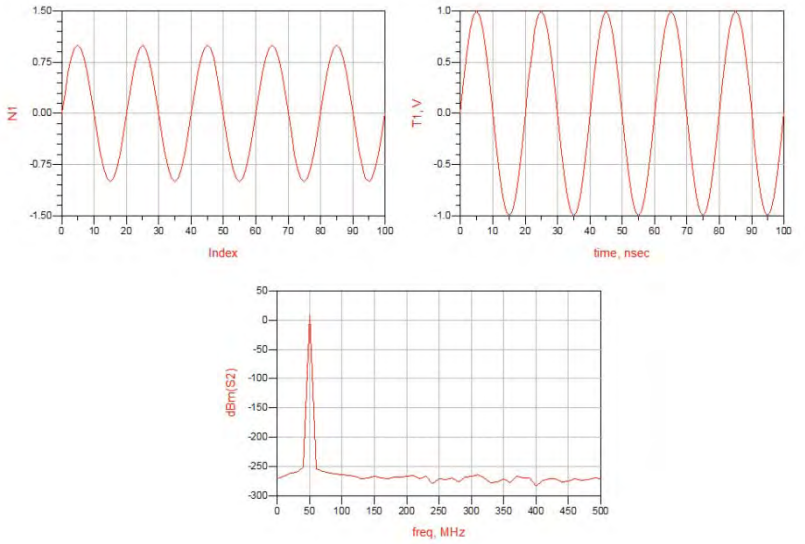
Modify following in the design:

a. Delete or Deactivate Tk Plot
b. Define TStep=1nsec in Float to Timed converter
c. Change the DefaultTimeStop=100nsec in the DF controller

Once completed, schematic should look as below:

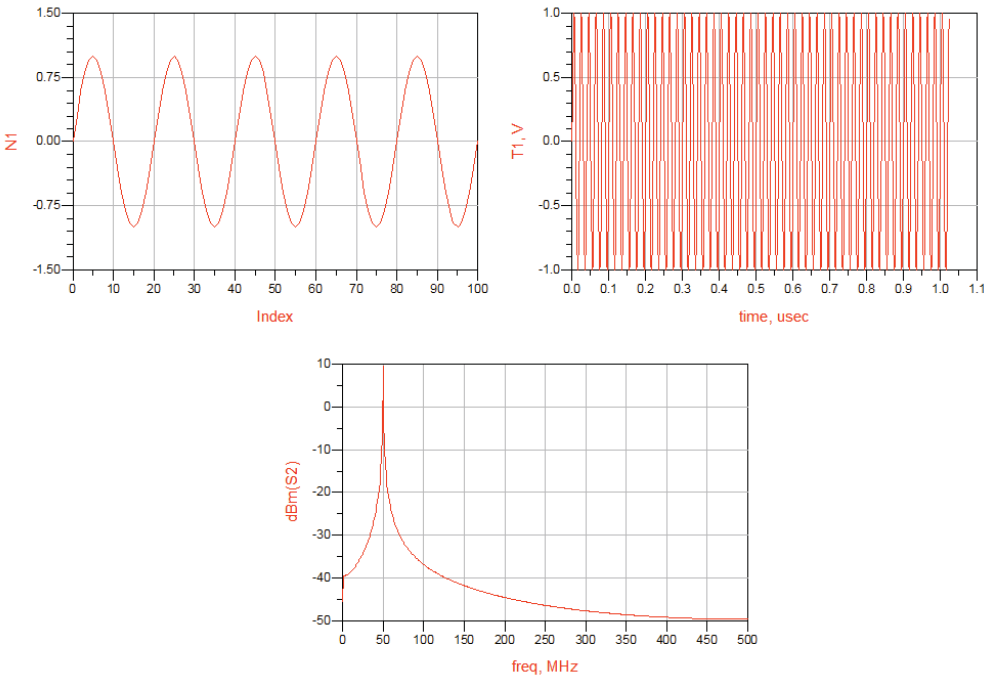


8. Simulate and add a new rectangular plot alongwith previously plotted N1 (Numeric sink) and select T1 (Timed Sink) and notice the time domain waveform with X-axis is denoted as time.
   Add a new rectangular graph and plot S2 (Spectrum Analyzer) in dBm to see the 1-tone spectrum waveform



Notice that resolution of spectrum plot is not good and that is because we only have 100 sample point resolution i.e. 100nsec (Stop Time) /1nsec (Sampling Time) = 100.

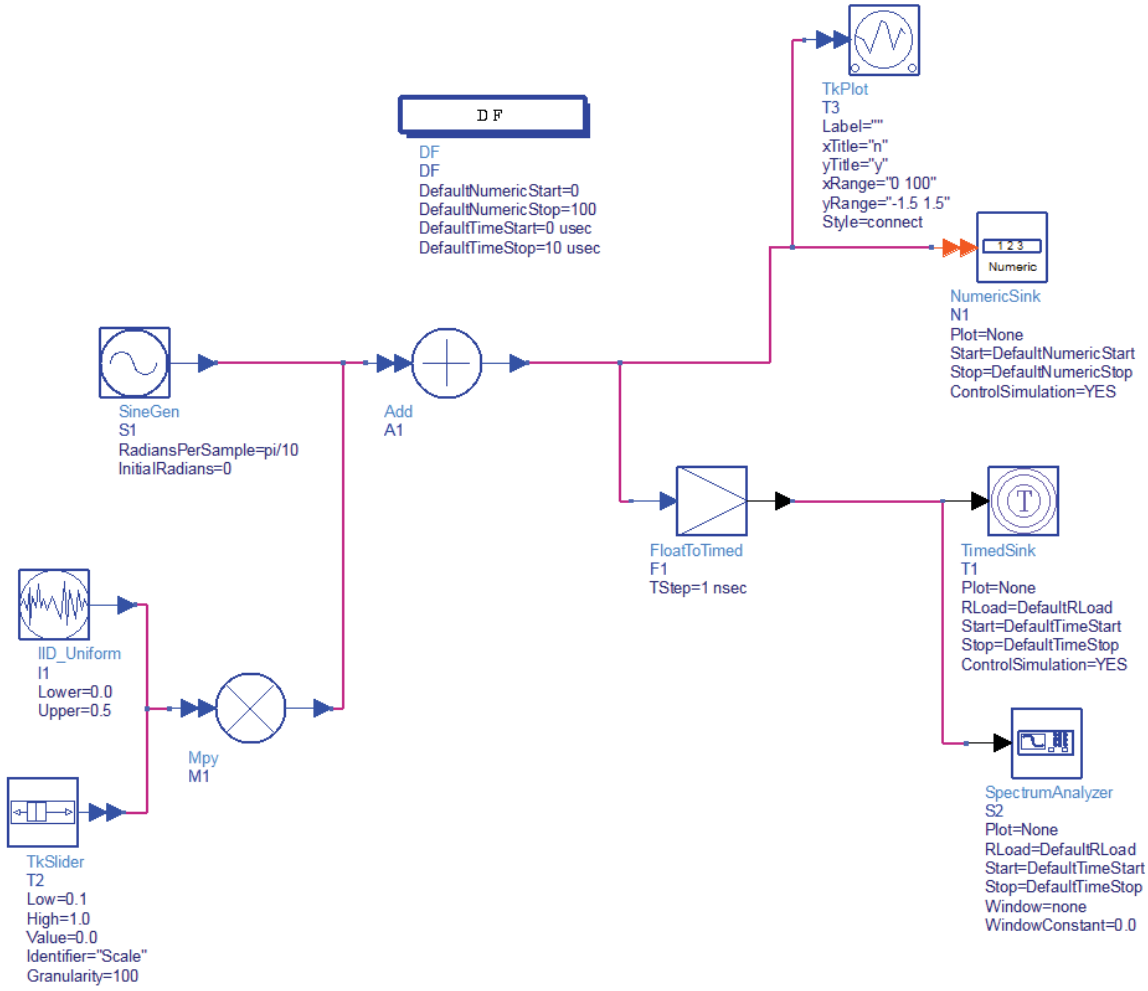
Increase the DefaultTimeStop = 1024 nsec and observe the data display again and now Spectrum plot should be much nicer. ***More samples you have better will be the spectrum resolution***



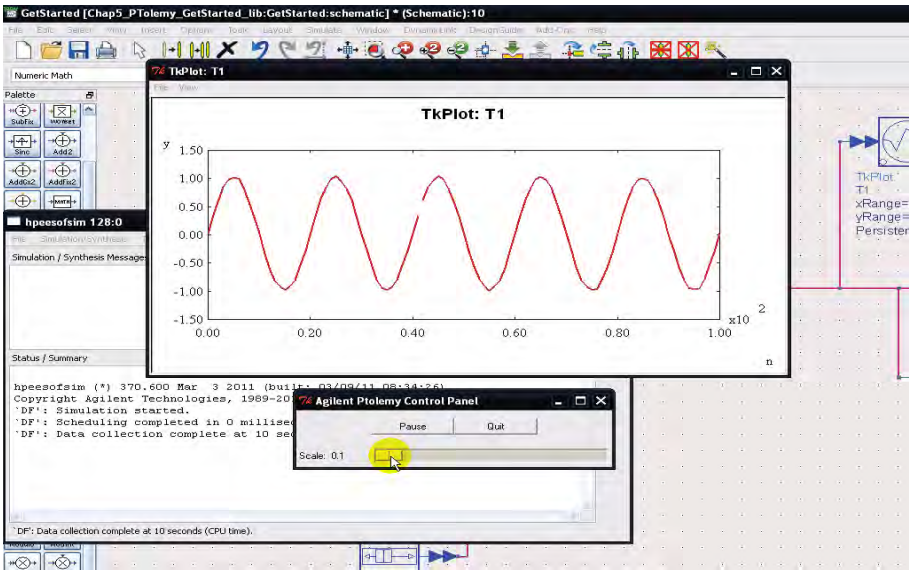
Lab2: Interactive Control

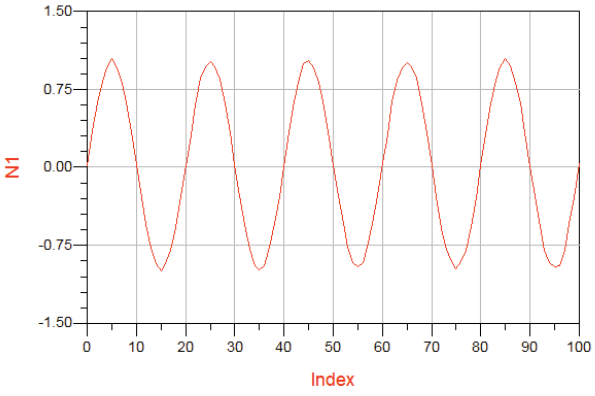
Let's extend Lab1 to understand how can we add few dynamically changing effects on to our system design by using TkSlider component from Interactive Controls and Displays library.

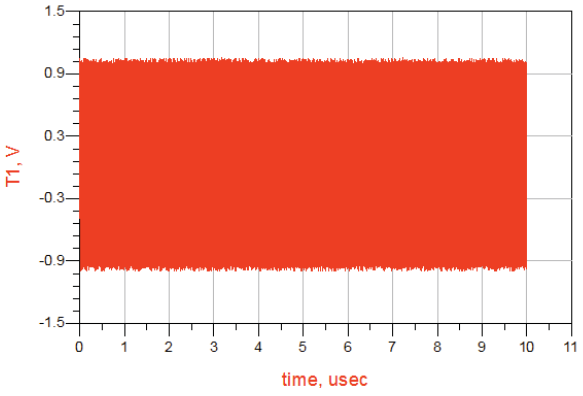
1. Do following:
   a. Insert TkPlot again (if deleted in earlier lab) or reactivate it (if deactivated earlier)
   b. Insert IID_Uniform noise source from Numeric Sources library
   c. Insert Multiply (Mpy) and Adder (Add) from Numeric Math library
   d. Insert TkSlider from Interactive Controls and Displays library
   e. Modify the DefaultTimeStop = 10 usec for good resolution in the spectrum plot with noise
   f. Connect them as shown below, essentially we are multiplying the IID_Uniform noise amplitude with the TkSlider ranging values of 0.1 (min) to 1 (max) and same shall be mixed with our clean SineGen source to introduce Signal + Noise effect for our analysis.

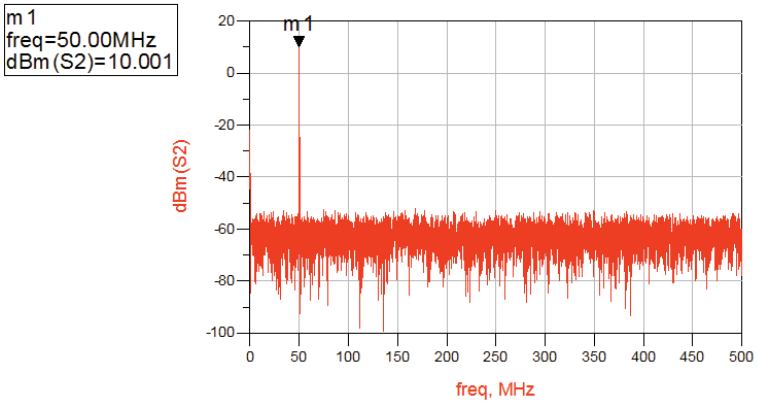


2. Simulate the design and notice a slider bar with Identifier shown as Scale (which is same as in TkSlider component) and when we change the slider the TkPlot changes in real time….Click Quit once done and observe the data display plot.









References

1. J. B. Dennis, *First Version Data Flow Procedure Language*, Technical Memo MAC TM61, May 1975, MIT Laboratory for Computer Science.
2. E.A. Lee and D. G. Messerschmitt, "Static Scheduling of Synchronous Data Flow Programs for Digital Signal Processing," *IEEE Trans. on Computers*, vol. 36, no. 1, pp. 24-35, January 1987.
3. E.A. Lee and D. G. Messerschmitt, "Synchronous Data Flow," Proc. of the IEEE, vol. 75, no. 9, pp. 1235-1245, September 1987.
4. R.M. Karp and R. E. Miller, "Properties of a Model for Parallel Computations: Determinancy, Termination, Queueing," SIAM Journal, vol. 14, pp. 1390-1411, November 1966.

Chapter 18: QPSK System Design using ADS PTolemy

ADS Licenses Used:

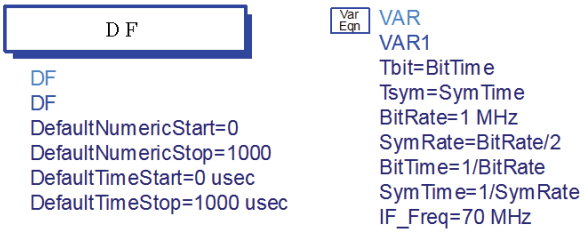
- **ADS PTolemy Simulator**

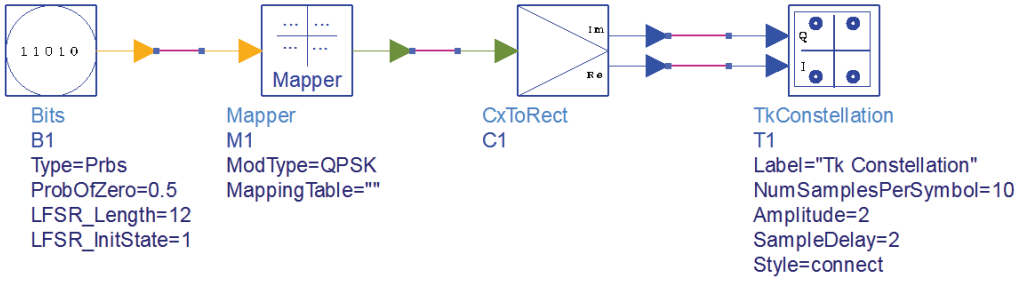
Chapter 18: QPSK System Design using ADS Ptolemy

Objective: With the basic understanding of ADS Ptolemy as described in the chapter Getting Started with ADS Ptolemy, we can now implement the QPSK system to perform end to end system simulation and BER analysis to gain more understanding.

Step1: QPSK Modulator Design

1. We shall start our system design by building a QPSK modulator network. Create a new workspace with a name **Lab18_QPSK_SystemDesign** and create a new Schematic cell with name **QPSK_Mod.**
2. With the understanding gained from previous chapter, place following components on a new schematic:
   a. **Bits** source and **change the Type to PRBS** (Notice the stem colour is Orange indicating this will be an Logic/Integer data type)
   b. **Mapper** and make sure ModType=QPSK (this shall map the bits to symbol in QPSK format, notice the input stem is Orange indicating Integer/Logic and output is green indicating complex number for I and Q symbols)
   c. **Complex to Rect** converter (CxtoRect) so that we can separate out I and Q symbols.
   d. **TkConstellation** from **Interactive Controls and Displays library** to plot constellation. Style in the TkConstellation sink can be kept as **connect** or **dot** depending upon is we just want to see constellation points or trajectory as well.



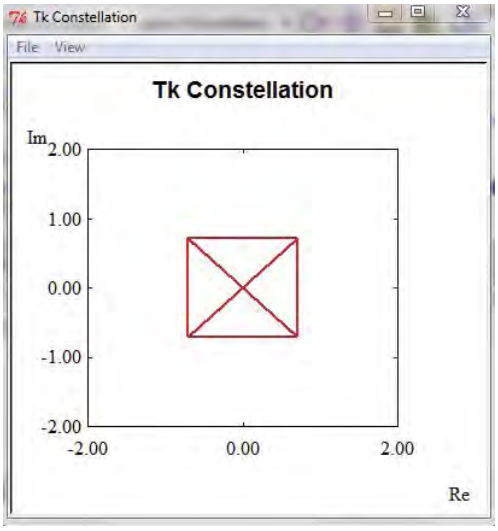


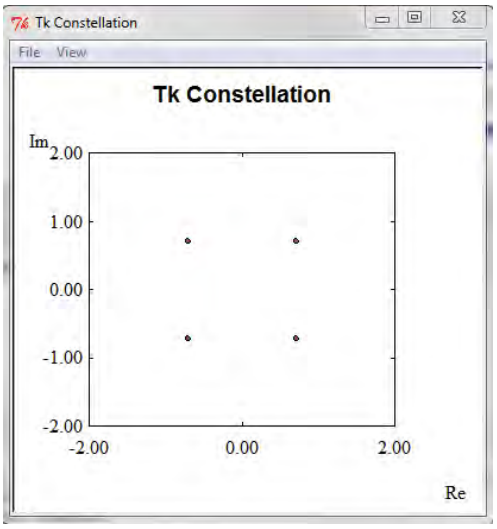
e. DF controller from Common Components library and change the NumericStop=1000 and TimeStop=100 usec

f. VAR block by clicking on the VAR icon 

and declare the variables as shown in the graphics

g. Simulate the design and notice the interactive plot as shown below (graphs for both connect and dot options are shown below). These graphs indicate that we are infact mapping the bits to QPSK format symbols.

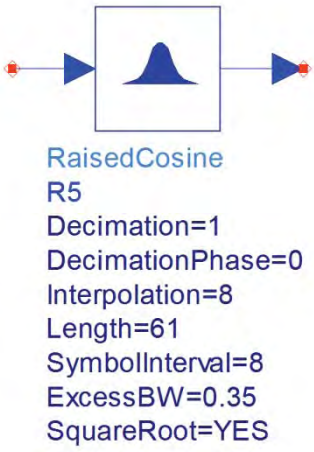




h. Click on Quit to finish the simulation. We have nothing to plot in data display.

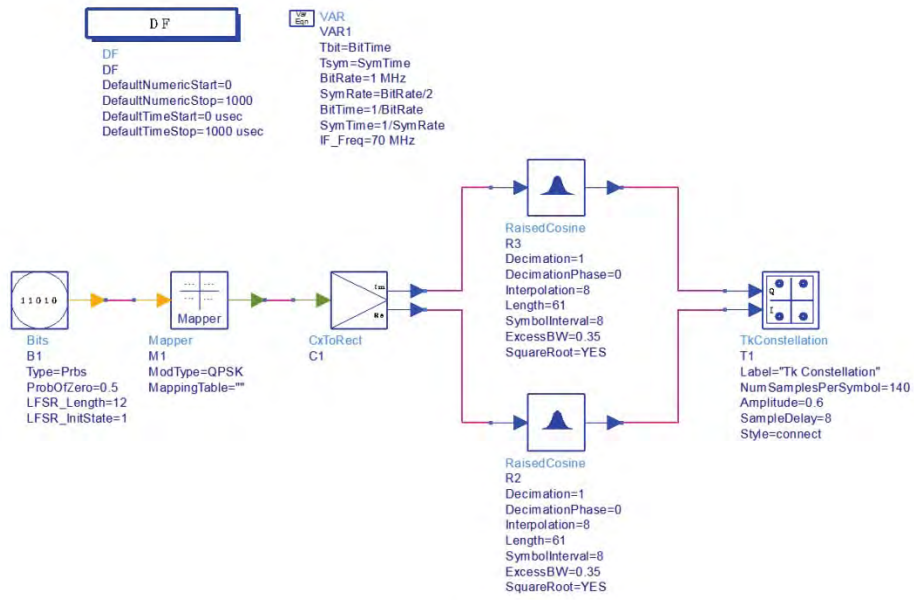
3. Spectrum Shaping (or Band limiting) Filters:

Communication systems often employ band limiting or spectrum shaping filters for I and Q channels/signals. Place Raised Cosine filters from Numeric Filters library and define the parameters as shown below in I and Q branches:

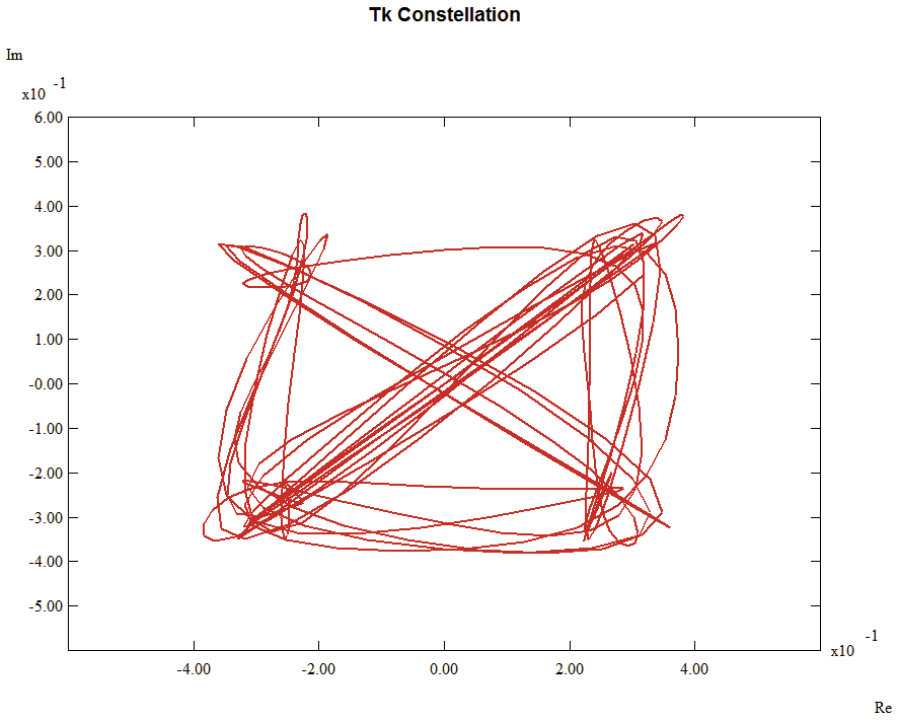


- Interpolation = 8
- Length = 61
- Symbol Interval = 8 (should be same as Interpolation)
- ExcessBW = 0.35 (i.e. 35% excess bandwidth)
- SquareRoot=YES (this makes it as a Root Raised Cosine Filter)

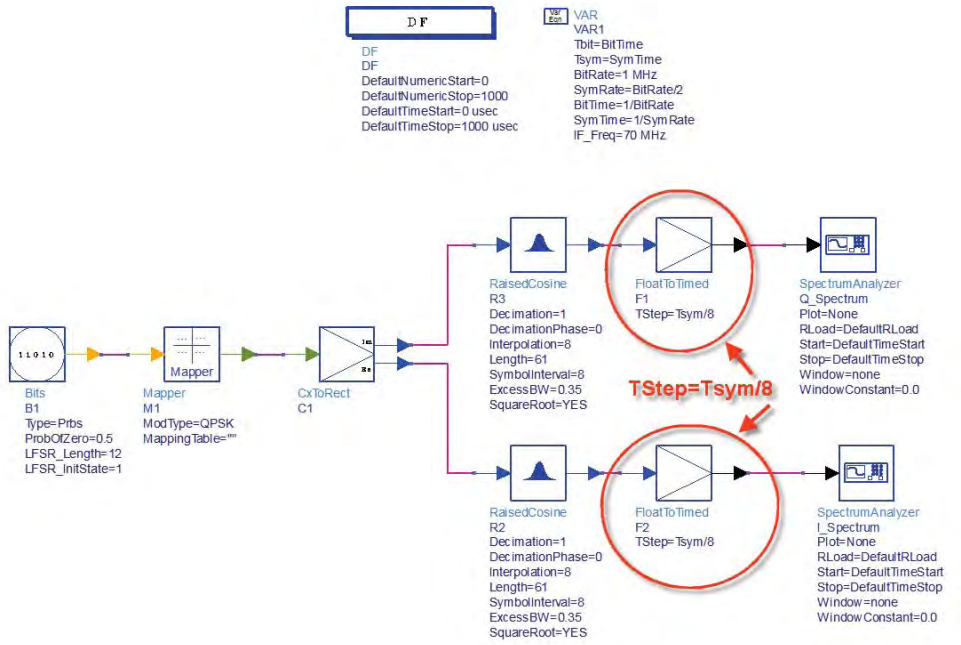
4. Once finished schematic should appear as below (note that we have shifted the TkConstellation sink after the RRC (Root Raised Cosine) filters to see the effect of filter on constellation.

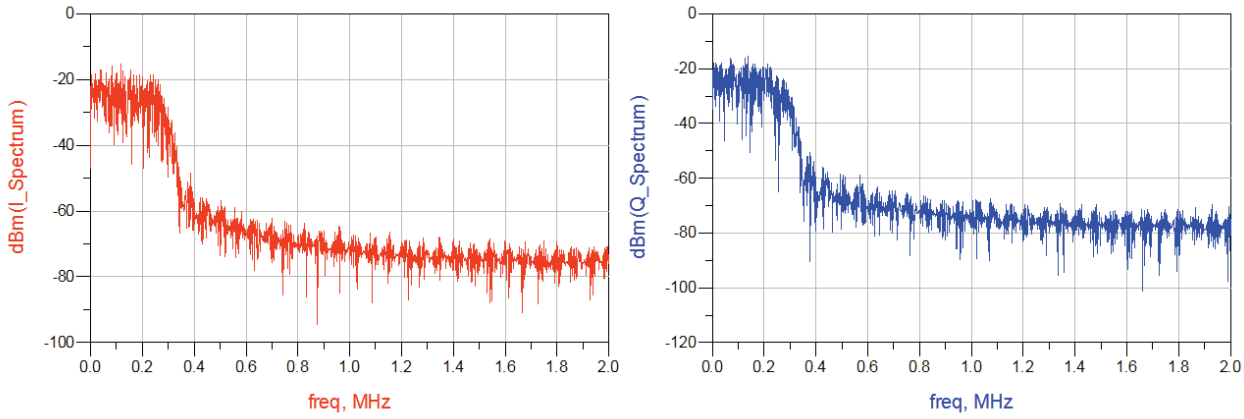


5. Simulate and observe the constellation after RRC Filters.

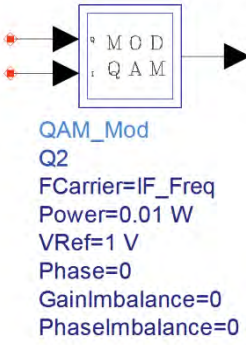


6. Now once we have the band limited I & Q signals we can perform the IQ modulation on the same but before that we can see the I & Q spectrum to make sure things are as we desire them to be.
    a. Insert **FloatToTimed** converter and I & Q channels and define **TStep=Tsym/8** and that is because we have interpolated (upsampled) I & Q signal by factor of 8 hence sampling rate by rise by that amount.
    b. Insert Spectrum Analyzer sink in I & Q channel and rename it as I_Spectrum and Q_Spectrum so that we can identify the same while plotting the data graphs.

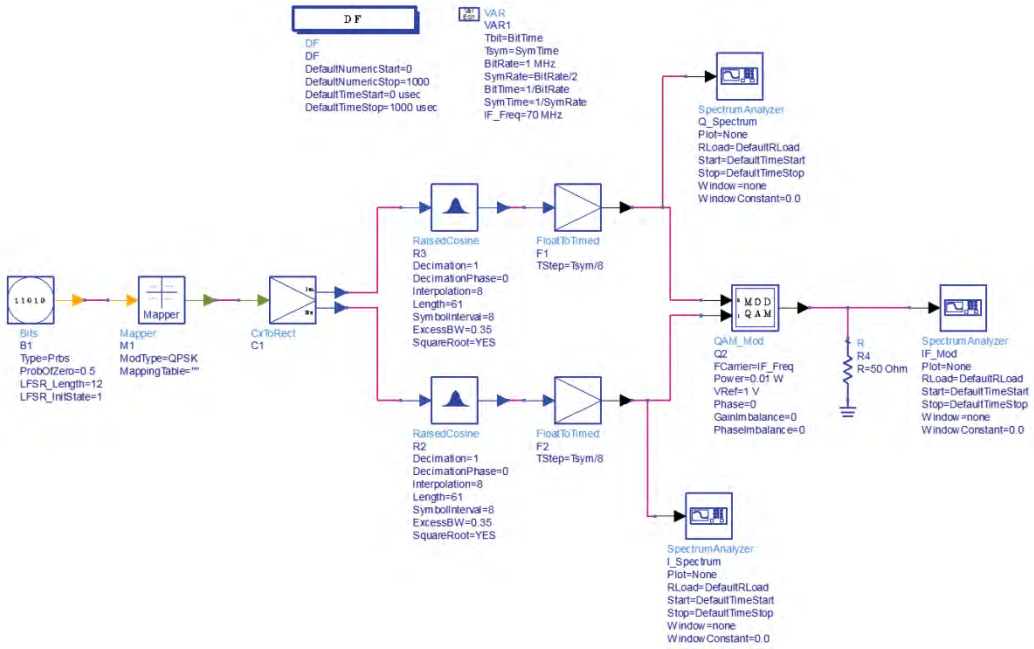


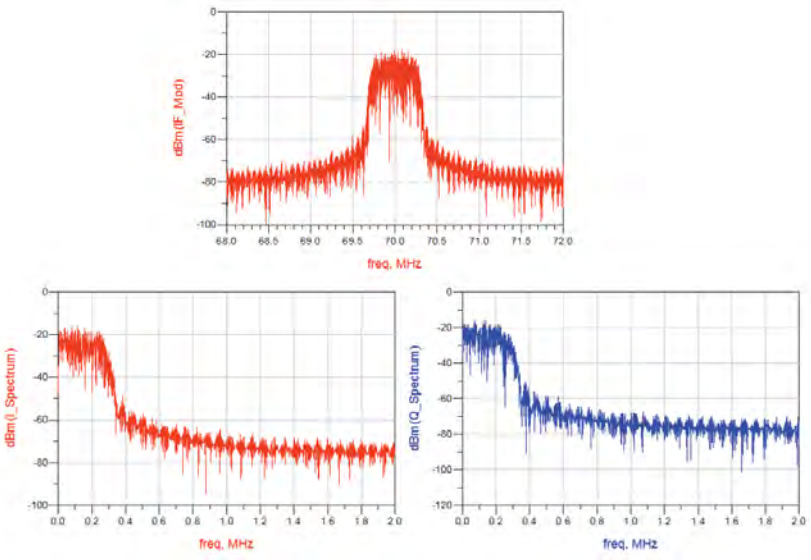


As we can from the previous graphics that I & Q spectrum looks to be fine, now we can place a QAM modulator from the Timed Modem library and define the parameters as shown here.



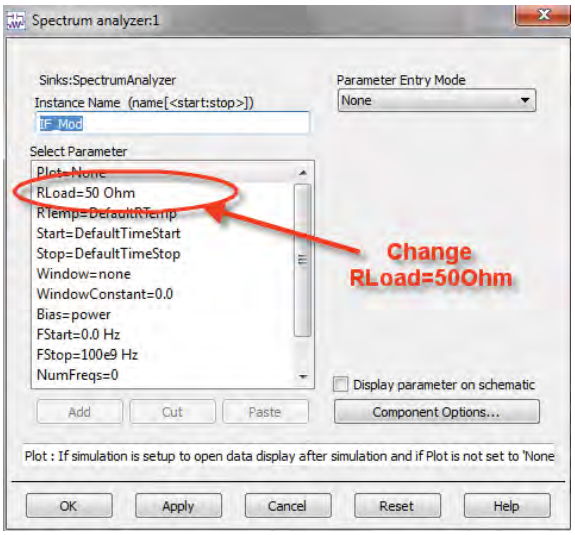
7. Connect the I and Q signals to the respective terminals and place a Spectrum Analyzer sink (**name it as IF_Mod**) to the output of QAM modulator with 50Ohm resistor in shunt to make sure we do the power calculations with respect to 50Ohm reference impedance.
8. Once done complete schematic design will look as shown below.
9. Run Simulation and plot the spectrum of IF_Mod as shown below



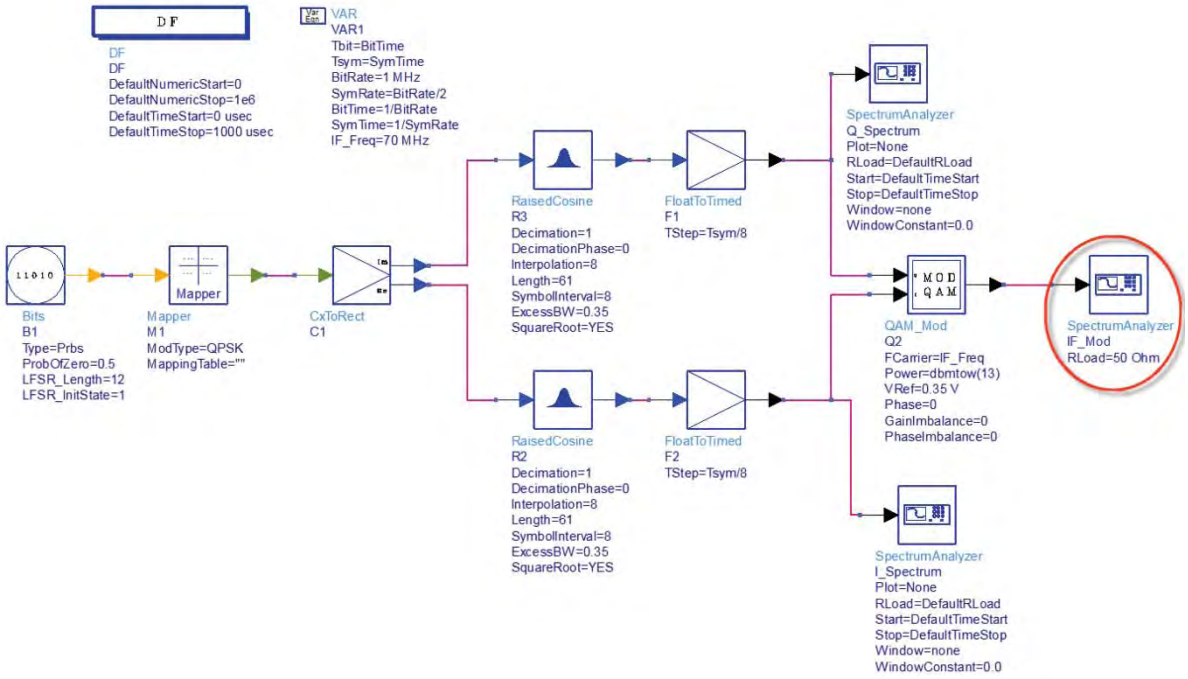


Step2: Modulated Output Power Calculations

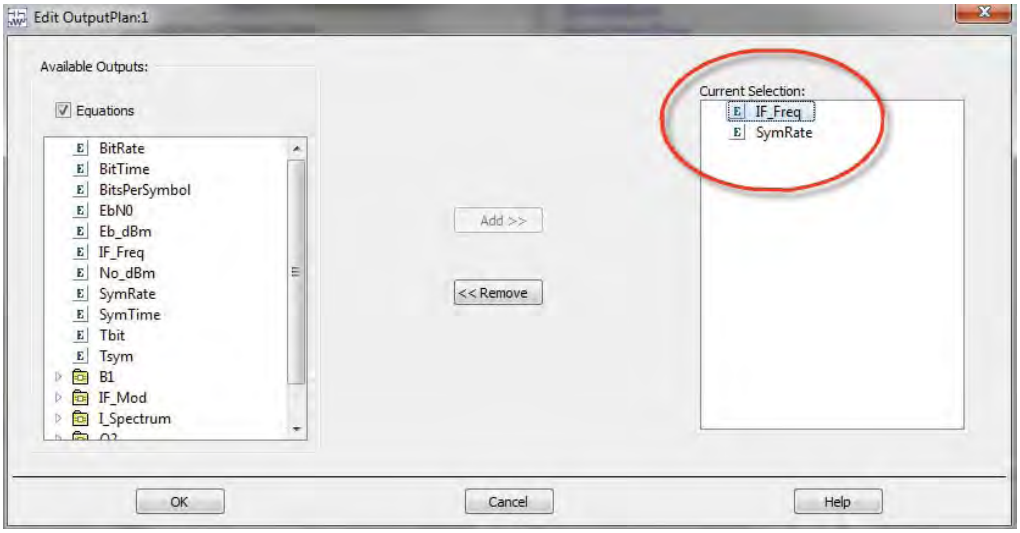
For correct power or voltage calculations, designers need to ensure that correct load impedance is used in the sinks. By default these sinks use DefaultLoadR which can be set from the DF Simulation controller's Resistor tab (this will make global change) or in individual sinks as may be needed as shown below. Another alternate technique is to connect 50Ohm resistor in parallel to the sinks where voltage or power calculations needs to be performed.



Change the RLoad to 50 Ohm and change Vref=0.35 and Power to 13 dBm in the modulator as shown below



Double click on the DF controller, go to Output tab and select IF_Freq, SymRate and click on Add. This allows us to access these variables in the data display to compute power.

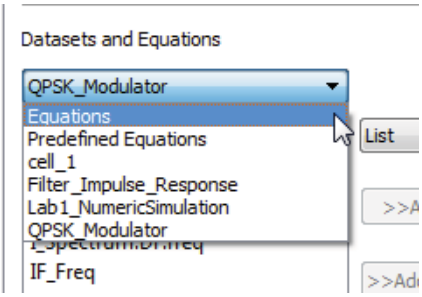


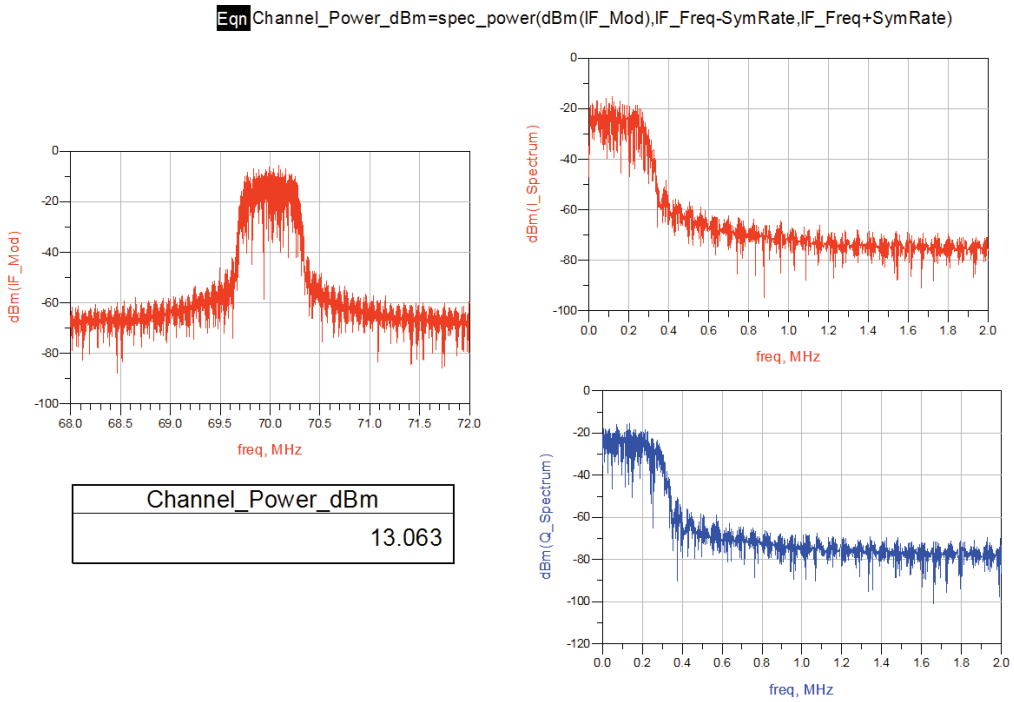
Run Simulation and use the **Eqn** button on data display to write an equation to compute Main Channel Power at the Modulator output:

Channel_Power_dBm=spec_power(dBm(IF_Mod),IF_Freq-SymRate,IF_Freq+SymRate)

Please note: *spec_power() is the function provided in ADS for Spectral Power calculations and IF_Mod is the name given to the Spectrum Analyzer sink connected at the modulator output. You can use whatever name you might have provided.*

1. Insert a Table plot and drag it to the desired size and select the Equations under Datasets and Equations as shown here.
2. Select the equation name from the list and click on Add>> to add this measurement on the Table.
3. The Channel Power should be @13dBm as shown on the snapshot on next page.



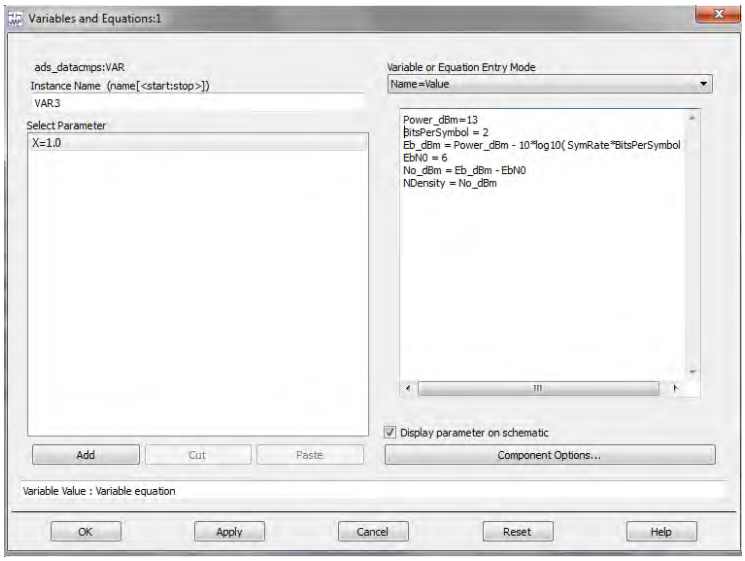


Step3: QPSK Demodulator and AWGN Channel

After we create QSPSK modulator design remaining sections in our QPSK system is Demodulator and AWGN (Additive White Gaussian Noise) channel.

1. Copy the earlier created QPSK_Mod cell by name QPSK_System *(Hint: From the main ADS window right click on the QPSK_Mod cell and select Copy Cell….type new name in the pop up window)*

2. Insert a new VAR block and change the Type to Name=Value and enter equations as shown in the snapshot below



Equations to be used:

Power_dBm= 13 ***(Comment: This is the Modulator output power measured previously)***

BitsPerSymbol = 2 ***(Comment: QPSK has 2 bits per symbol)***

Eb_dBm = Power_dBm - 10*log10(SymRate*BitsPerSymbol)
(Comment: This is to compute the energy per bit)

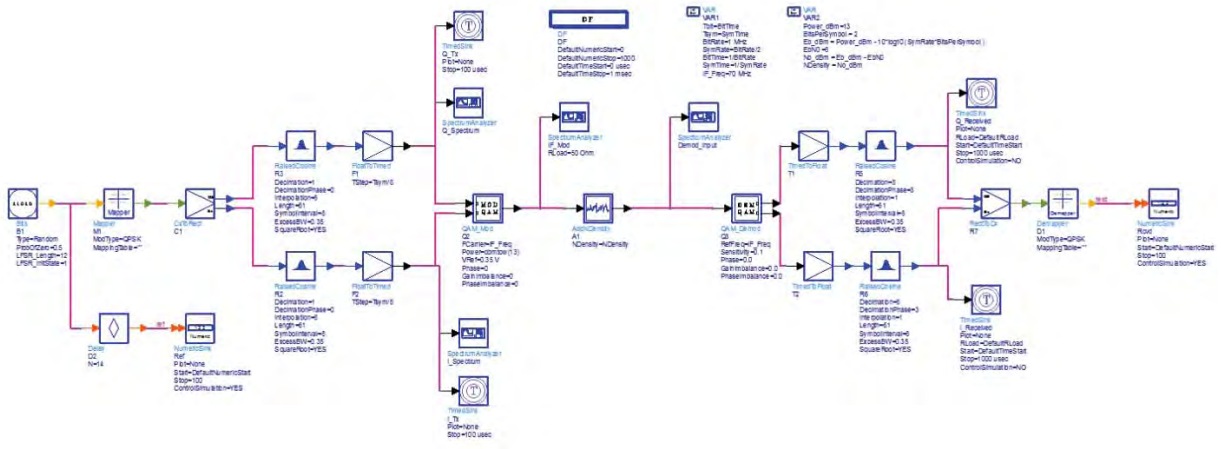
EbN0 = 6 ***(Comment: Eb/No variable which will be swept for BER vs. Eb/No curve)***

No_dBm = Eb_dBm - EbN0 ***(Comment: Noise power in dBm to be added to the signal)***

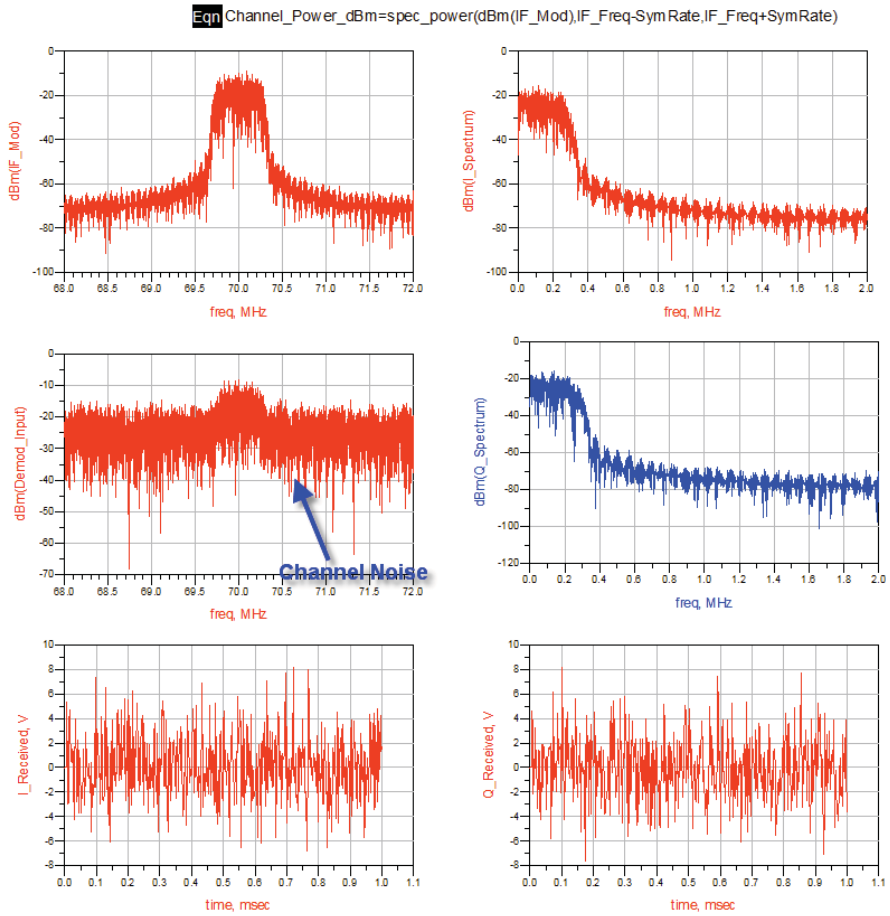
NDensity = No_dBm ***(Comment: Optional variable to read the Noise Power)***

3. Insert following components on the design:
    a. **AddNDensity** (AWGN channel) and define the NDensity as No_dBm or NDesnsity as per the equation variable written earlier)
    b. **QAM_Demod** and define the frequency as IF_Freq
    c. Insert **TimedToFloat** to I & Q channels at the output of QAM Demodulator
    d. Copy/Paste the RRC filter which were used in Modulator part and change the parameters as following
        i. Decimation = 8 (same as Interpolation used earlier)
        ii. Decimation Phase = 3 (we need to choose this parameter carefully to make sure we have the decent constellation at the output of RRC filters, range of this parameter is [0-(Decimation – 1)])
        iii. Interpolation = 1
        iv. SymbolInterval = 8 (same as Interpolation which 1)
        v. ExcessBW = 0.35
        vi. Length = 61
    e. Connect **TimedSink** at the output of each RRC Filters and name it I_Receive & Q_Receive as applicable.
    f. Connect **SpectrumAnalyzer** sink at the output of Noise Channel and name it as Demod_Input
4. Double click on the DF controller and go to Output Tab where you should see SymRate & IF_Freq already added. Select NDensity or No_dBm, EbNo from the list and click on Add button so that these values are available in the data display.

Overall QPSK system schematic should now appear as below



Run Simulation and plot a new graph for Demod_Input (which should show signal plus the noise as per our EbNo value) and Time Domain graph for received I & Q data. Data display should look something as below



Step4: BER simulations

From the steps above system seems to be behaving properly and remaining thing is to perform the BER simulations. Before we perform BER we need to synchronize the Tx reference signal (output of Bit source at the input) and Received Bits (output of the Demapper).

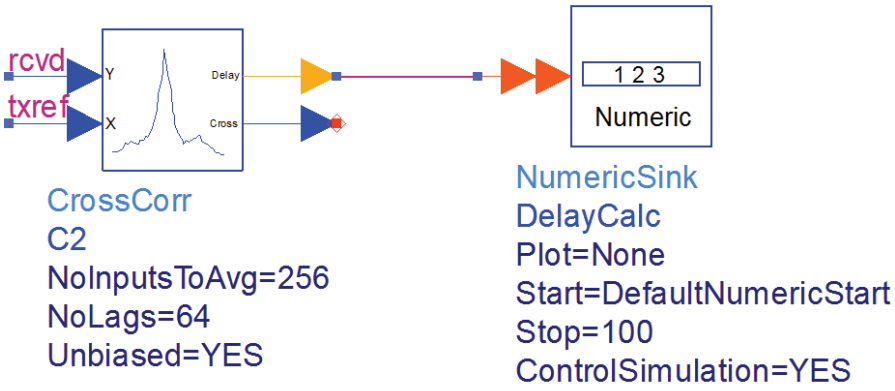
Copy the QPSK_System cell as QPSK_System_BER.

To find the delay easiest way is to use Cross Correlation block in Numeric-Signal Processing library as shown below.

1. Instead of drawing long wires, we can use Wire Label 

to name the nodes to be connected, name X pin of the CrossCorr block as txref and label the same name at the output of Bit source at the Input. Name pin Y as rcvd and provide the same name label to the output of the Demapper.

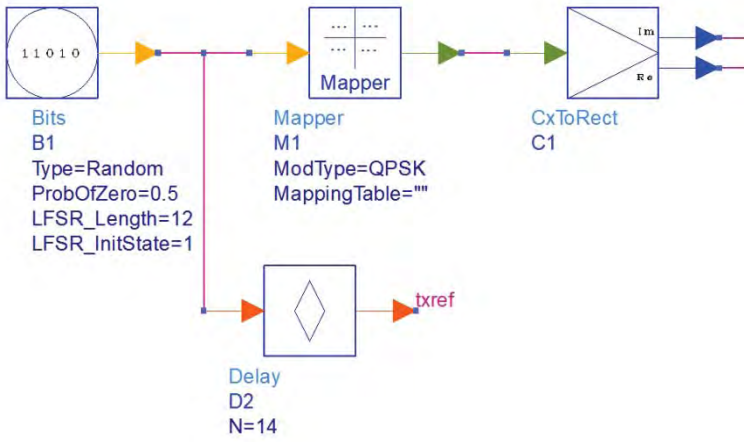
2. Connect a Numeric Sink (name it as DelayCalc) at the Delay output of the CrossCorr block as shown below to note the delay between the 2 signals (delay might be shown as negative and that would mean that signal at Pin X is delayed with respect to Pin Y of the CrossCorr block, usually we should connect ref signal to Pin X of the CrossCorr block)



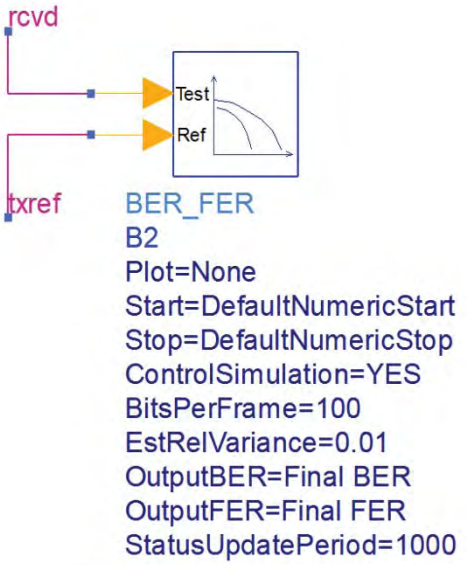
3. Run simulation and plot the result of the DelayCalc in a table as shown below:

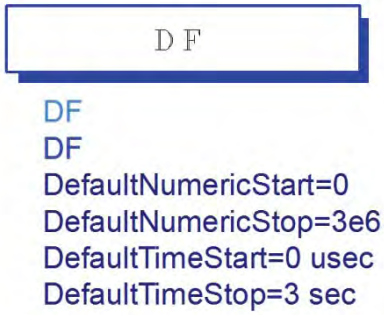
Index	DelayCalc
0	14.000
1	14.000
2	14.000
3	14.000
4	14.000

4. This simulation results indicate that received signal is delayed by 14 samples as compared to the reference signal and we need to insert 14 sample delay in the reference signal before we perform BER simulations.
5. Insert a Delay block after the Bit source and modify the Delay value to 14 as we calculated. Label the output of the Delay block as **txref**…

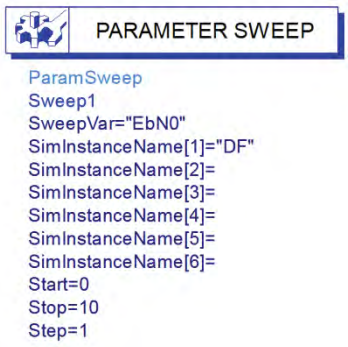


6. Insert BER_FER sink from Sinks library and set its parameters as shown here
    a. Start=DefaultNumericStart (it reads start value from PTolemy DF controller)
    b. Stop=DefaultNumericStop (it reads stop value from PTolemy DF controller)
    c. EstRelVariance=0.01 (Confidence factor for BER calculations)
7. Modify the DF controller to set the values as shown below. Here we are using 3e6 and we may require more for lower BER values as this sink is based on Monte Carlo technique.

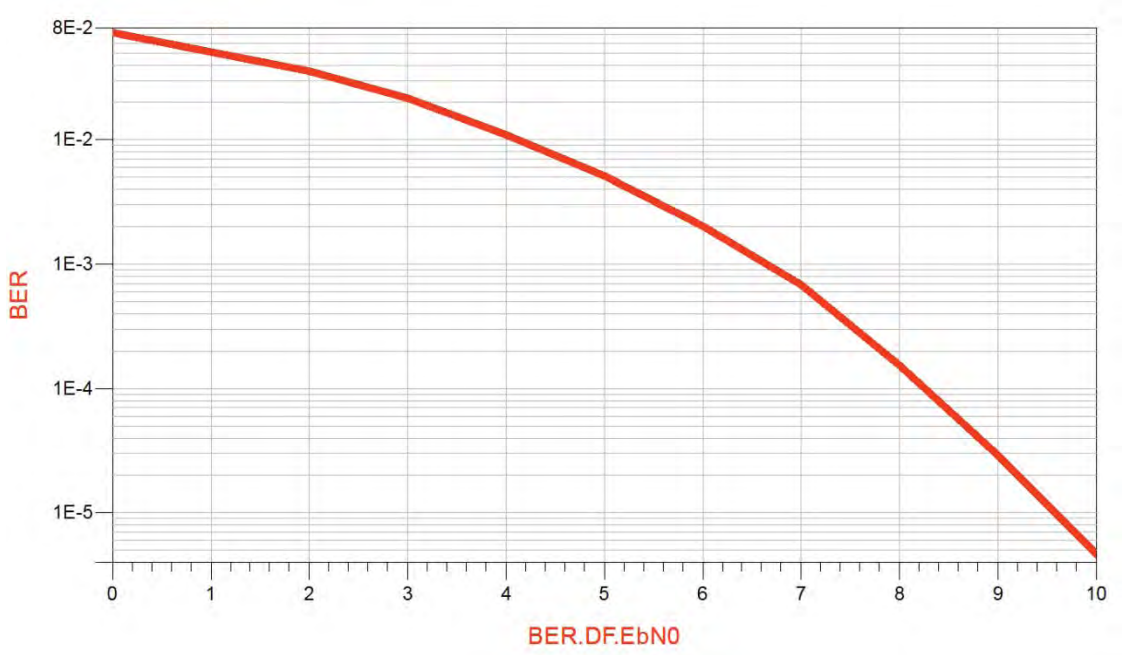




8. Insert a Parameter Sweep controller from Controllers library and set its parameters as shown here. This is to provide the sweep to EbN0 from 0 to 10 in a step of 1 which inturn will change the Noise to offer known EbN0 for specific modulation (QPSK as in our case) for BER calculations.



9. **Disable all other Sinks on the schematic design else we will get Out of Memory error due to huge dataset size because of large number of samples.**
10. Perform simulation and please note it might take good amount of time on higher EbN0 values as we need more number of bits for errors to happen.
11. Once simulation is finished, insert a rectangular plot in the data display and **select BER from the list of measurements and click on >>Add Vs…>> and select BER.DF.EbN0** (because we want to plot BER vs. EbN0). **Change the Y-axis to be log type** to see proper Waterfall curve characteristics as shown below.



Chapter 19: DSP / RF Co-simulation using ADS 2011

ADS Licenses Used:

- **ADS PTolemy Simulator**
- **Circuit Envelope Simulator**

Chapter 19: DSP - RF Cosimulation using ADS 2011

Objective:

If often needed to integrate DSP and RF subsystems to characterize the complete system performance for various system level specifications. ADS PTolemy which is essentially a mixed signal simulator offers a nice way to combine DSP and RF systems together as discussed in this chapter.

DSP RF Co-Simulation Basics:

To get started with the Mixed Signal system simulation, we assume that users have DSP system (as illustrated in Chapter 17) and RF systems (as illustrated in Chapter 5) which are tested independently and found to be working as desired.

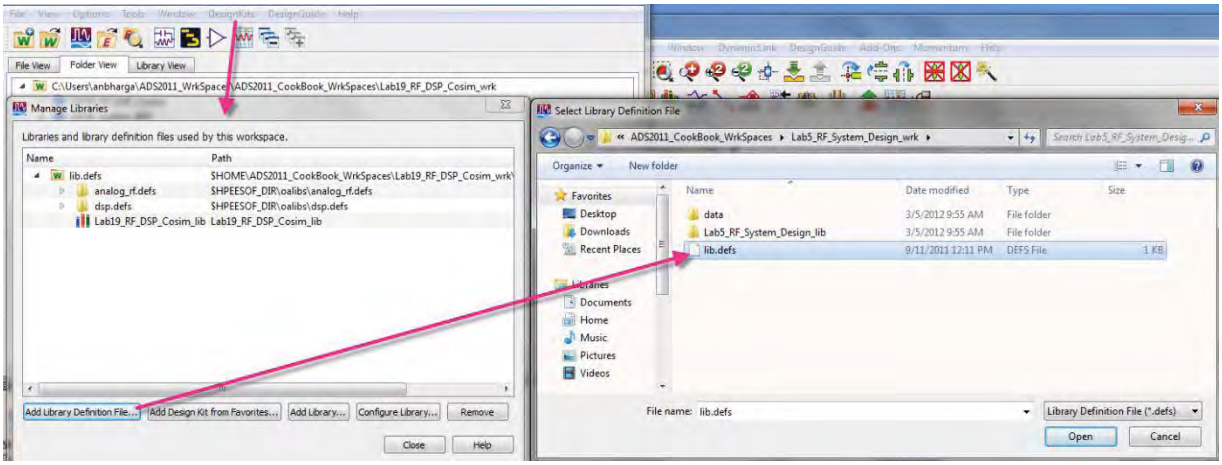
For performing integrated simulation, following things are to be understood:

a. RF system will always be called as sub-circuit on the main DSP design schematic i.e. Ptolemy will be end-2-end simulator and RF section will form part of the overall system design schematic.
b. RF sub-circuit can use either Envelope or Transient as a simulator because only these 2 simulators have time samples which will essentially allow PTolemy fed input samples to get processed by RF system/circuit and then pass the samples back to PTolemy.
c. The Source and Sink has to reside in Ptolemy i.e. data should start and end in Ptolemy environment.
d. If RF subcircuit is using Envelope controller then the RF subcircuit block in Ptolemy should be followed by EnvOutSelector block in Ptolemy to select the band which needs to be passed into Ptolemy as RF will generate Main band + Harmonic bands as per the setup done in Envelope controller and with Ptolemy operating on bandlimited signal we need to filter out the band by specifying the Carrier (centre) frequency of that band. How much frequency span is picked up is defined by the Sampling Time Step set on Timed component in Ptolemy environment.

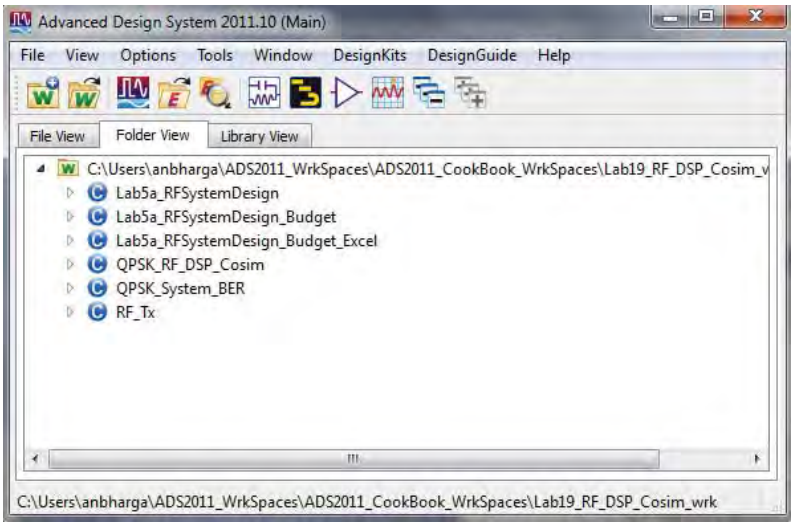
Example Case Study:

Let's take a simple example of QPSK system designed in Chapter 17 and RF Receiver designed in Chapter 5 to understand this concept of DSP RF cosimulation. Only difference is that we have designed additional RF Transmitter similar to RF receiver as illustrated in Chapter 5.

1. Create a new workspace with name Lab19_RF_DSP_Cosim_wrk
2. Go to DesignKit->Manage Libraries
3. Browse to Lab5_RF_SystemDesign_wrk and select lib.defs under the workspace folder as shown in next snapshot
4. Add lib.defs using the same method for Lab18_QPSK_SystemDesign_wrk

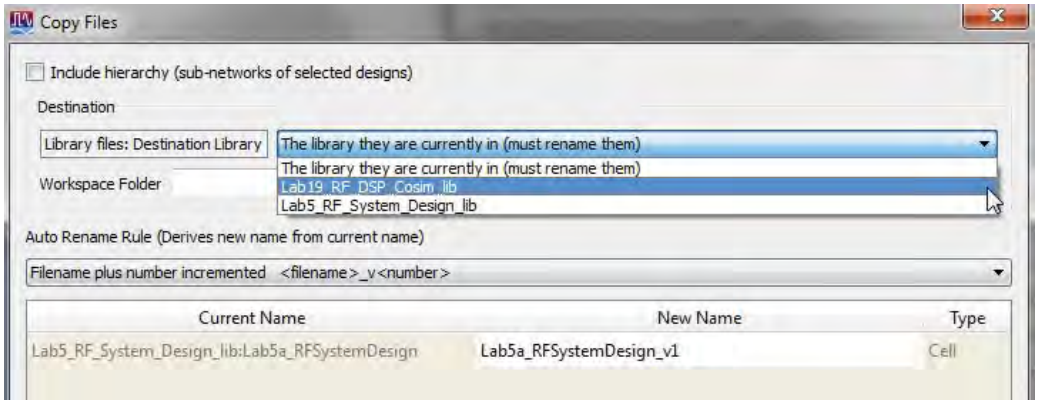


5. Now, once the previous workspaces are included we can see design cells of both of these workspaces in Lab19_RF_DSP_Cosim_wrk as shown below

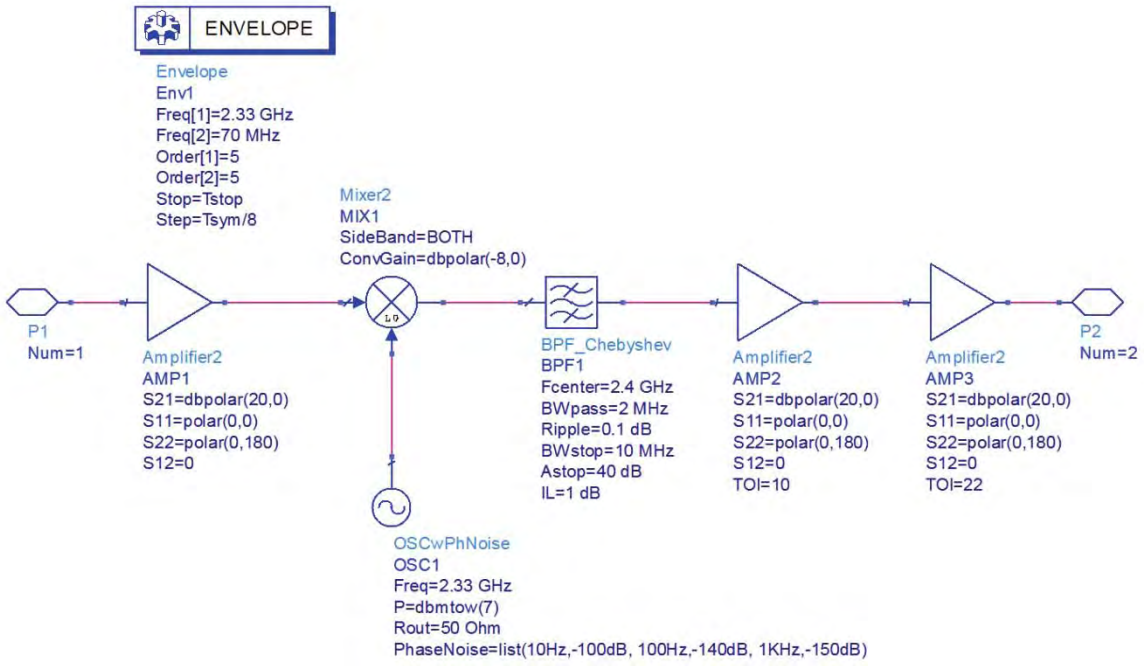


6. Once these designs are included in our present workspace, we have 2 options of using them for cosimulation:
    a. **Option 1:** Copy the required cells from these workspace locally in Lab19 workspace, this will make Lab19 independent of earlier 2 workspaces. However, if any changes are done to those designs then we will need to copy them again for cosimulation.
    b. **Option 2:** Let the original designs be there in their respective workspace and we can just create cosim schematic in Lab19. However, we need to make sure that path of earlier 2 workspaces don't change else we need to remove the 2 lib.defs files and include them with the new path again. Main benefit of this is that if any changes are done to RF subcircuits or DSP designs either in the original workspace or while using them in Lab19 it will reflect automatically.

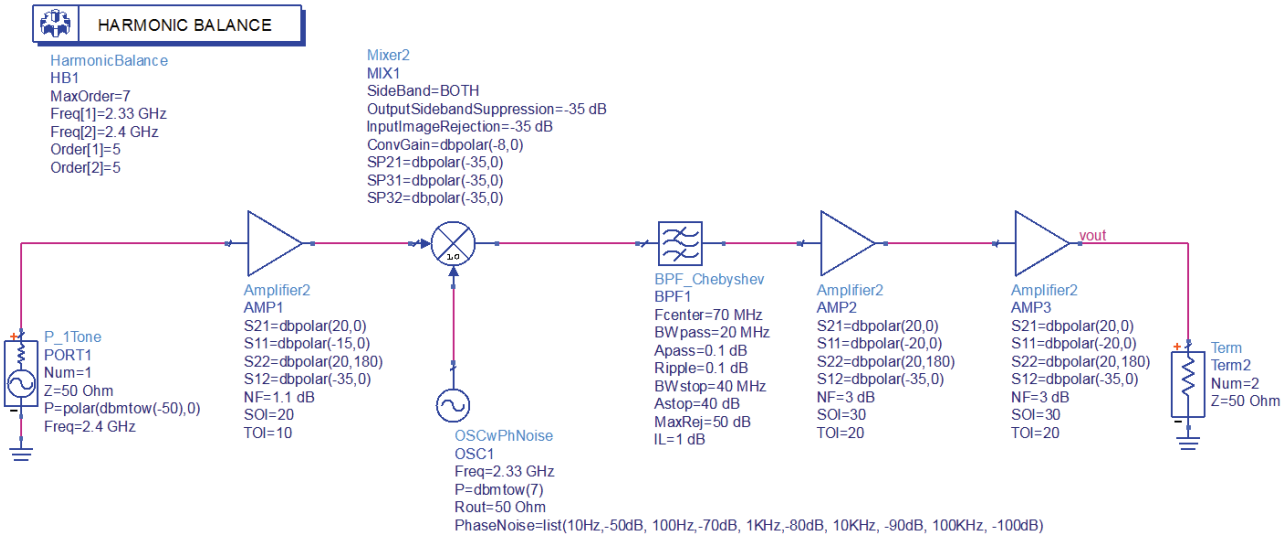
7. We shall use Option1 in present case and copy the required designs into Lab19 workspace. To do that right click on the desired cell and select Copy Cell and select the library in which these cells have to be copied and provide a new name to the copied cell if needed. By default ADS will add **_v1** in front of the cell name as shown below:



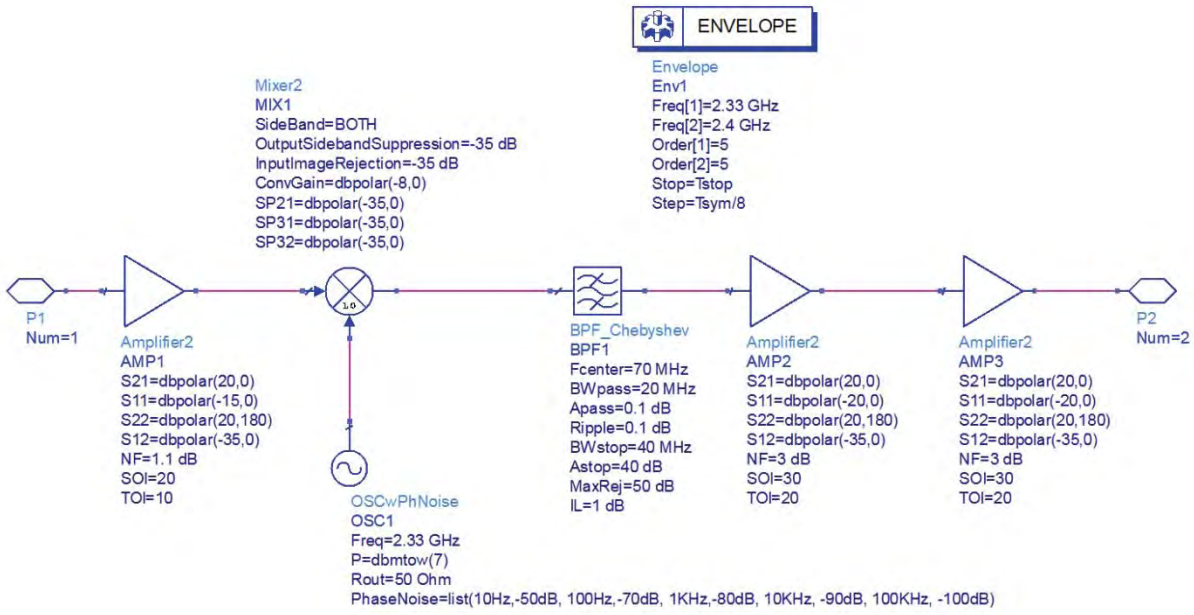
8. Once all the required designs have been copied to Lab19 workspace we can remove the 2 lib.defs file to avoid any confusion. To remove the lib.defs file, go to DesignKit->Manage Libraries and select the name of required lib.defs file and click on Remove. Repeat the process for other lib.def file.
9. Now we will be left with 2 design cells (if user is following the same nomenclature as mentioned in these chapters):
    a. QPSK_System_BER
    b. Lab5a_RFSystemDesign_v1
10. Create a new Schematic cell with name RF_Tx and create a RF Tx as shown below ***(pay special attention to the component specs such as TOI etc)***



11. Right on Lab5a_RFSystemDesign and select Rename and rename the cell as RF_Rx. Open the same to see design as shown below (recall that this is the design which was completed during Lab5):

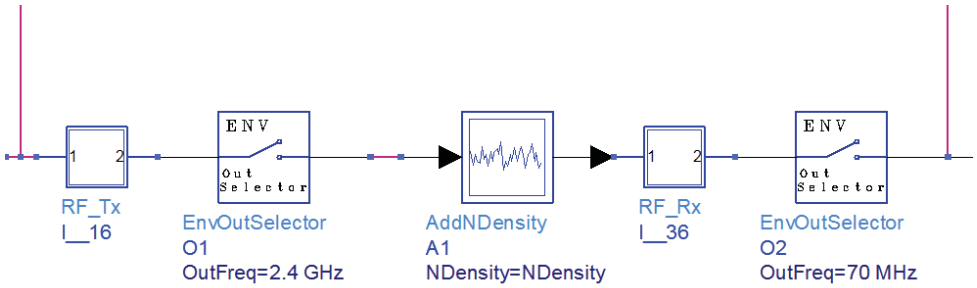


12. Delete P_1Tone, Term2 and HB controller from the schematic. Insert a Circuit Envelope controller from Simulation-Envelope library and set its parameter as shown below. Add Port 1 and Port 2 at input and output respectively. Once complete it should look like below:



Note: Please note Tsym is already defined in Ptolemy and we shall define Tstop later

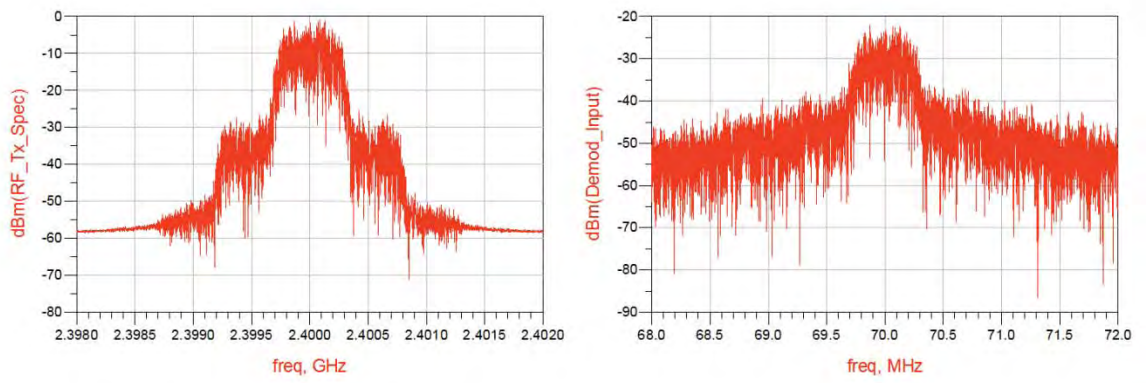
13. **Open the QPSK_System_BER schematic** and perform following actions:
    a. Disable BER sink, Delay block (connected to Ref Bit source) and Parameter Sweep controller.
    b. Enable all Spectrum Analyzer and Timed sinks
    c. Change the DefaultNumericStop and DefaultTimeStop to 1000 and 1 msec respectively
    d. Drag and Drop RF_Tx and RF_Rx designs from the main ADS window to this schematic (if you get Symbol generation method select Yes and then click OK to auto generate 2 port symbols)
    e. Place 2 EnvOutSelector components from **Circuit Cosimulation** library.
    f. Connect the RF_Tx etc as shown below. Make sure OutFreq in EnvOut selector is defined as per the expected frequency in our system design i.e. for output of Tx we defined as 2.4GHz and Output of Rx we have IF coming at 70 MHz.
    g. Modify the QAM modulator parameters: Power = -30 dBm, Vref=0.7V (this is to feed -30dBm at IF port else it will severe non-linear distortion)



h. Change the Spectrum Analyzer connected at Modulator output to be placed at Output of EnvOutSelect of RF_Tx so that we can observe the spectrum which got modified by RF Transmitter. Modify the name of this sink as RF_Tx_Spec

i. Add a variable Tstop = 1 msec (syntax and case should be same as used in Envelope controller)

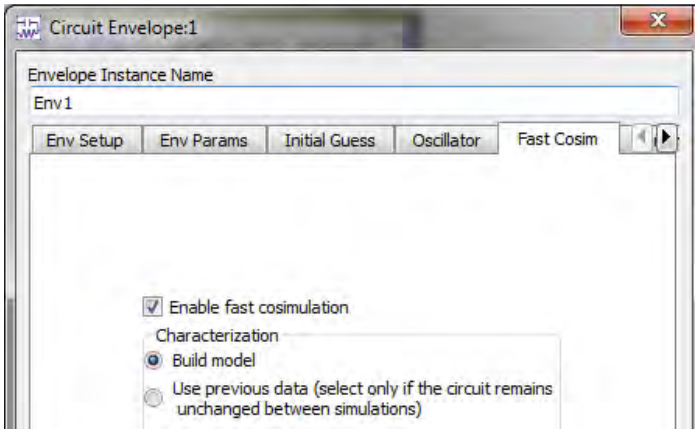
14. Perform simulation and plot 2 graphs: Tx_RF_spec and Demod_Input as shown below



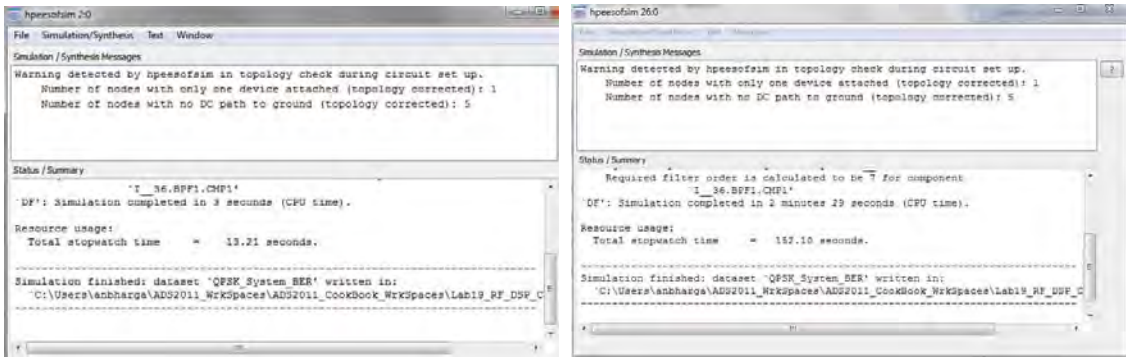
Notice the shoulders generated at Tx output due to Amplifier compression etc and also the simulation time taken for this complete system analysis. On a Dual Core Win7 machine the simulation time reported is @2mins and this will make it impractical when we perform BER kind of simulations

15. We can use Fast Cosim option provided in Envelope controller as long as the RF system/circuits are not changing or getting optimized. Refer to Fast Cosim documentation to get more details on the same. Go to RF_Tx subcircuit and double click on the DF controller->Fast Cosim tab and Select Enable Fast cosimulation as shown here.

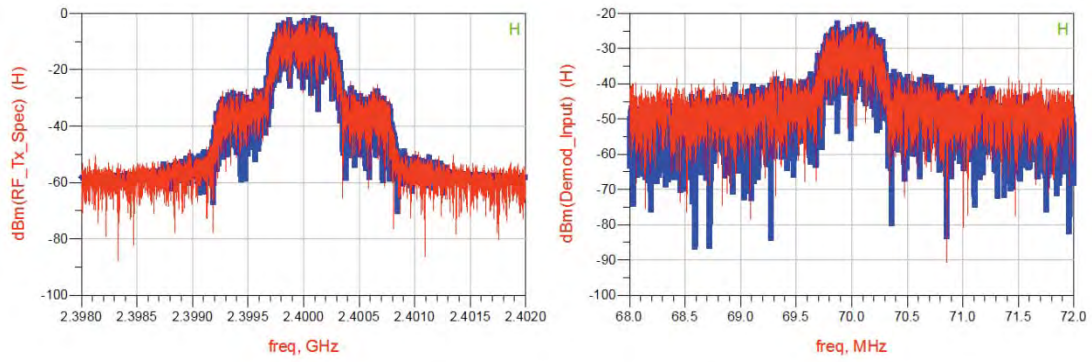
16. Go inside RF_Rx and enable the Fast Cosim option, additionally click on **Set Characterization Parameters** and enter Max Input Power = 50 dBm



17. Come back to main QPSK system design and run simulation, note the simulation time taken with Fast Cosim as shown below….we can speed improvement of >10x which results in huge time savings. Performance comparison snapshot shows that the performance is identical while using Fast Cosim method hence it can be used for lengthy simulations such as BER later.



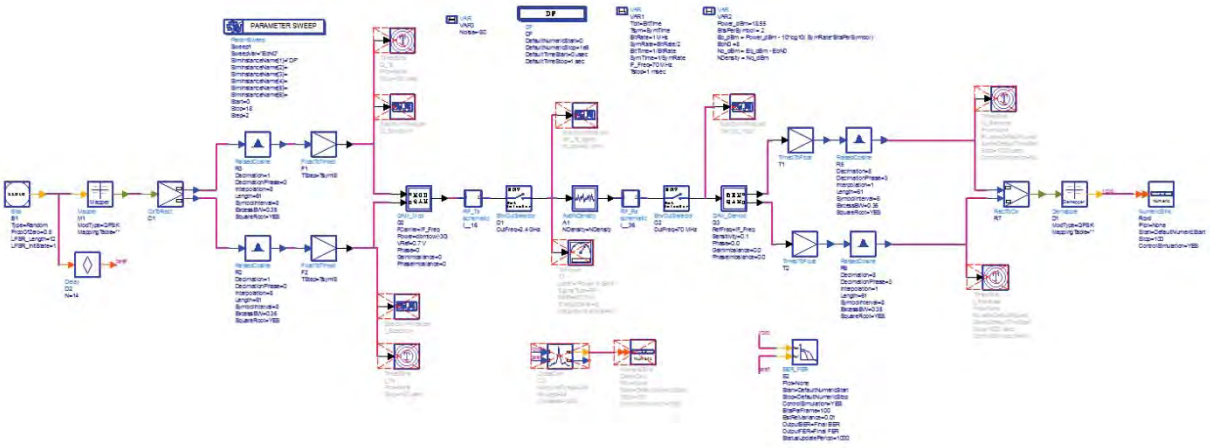
Performance Comparison of System Performance with and without Fast Cosim



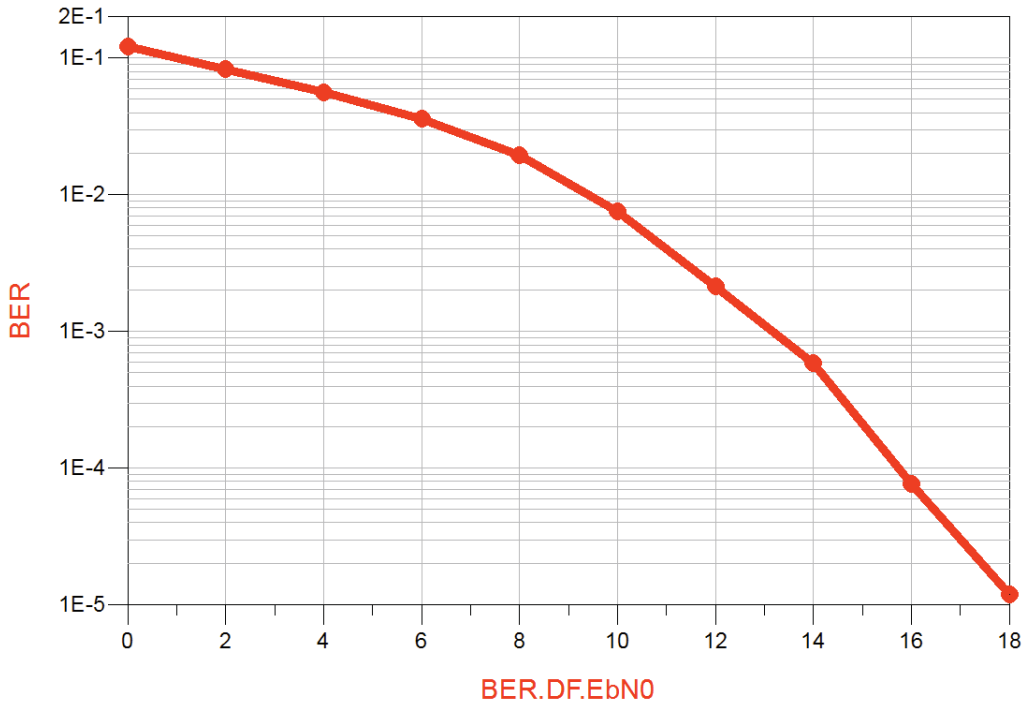
BER Simulations for RF – DSP Cosimulation:

Till now we are able to cosimulate RF and DSP design together and understood various key aspects of the co-simulation. We can extend this idea and now perform BER simulations on overall system. Do following:

a. Enable Delay, BER sinks and Parameter Sweep Controller.
b. Modify the Parameter Sweep to set EbN0 sweep from 0 to 18 in a step of 2
c. Disable all other sinks as we are going to run BER simulation which will involve large no. of samples
d. Modify the DF controller DefaultNumericStop and DefaultTimeStop to 1e6 and 1 sec respectively (we can use 3e6 and 3 sec also but in present case 1E6 and 1 sec would work just fine)
e. Modified schematic would look like snapshot below



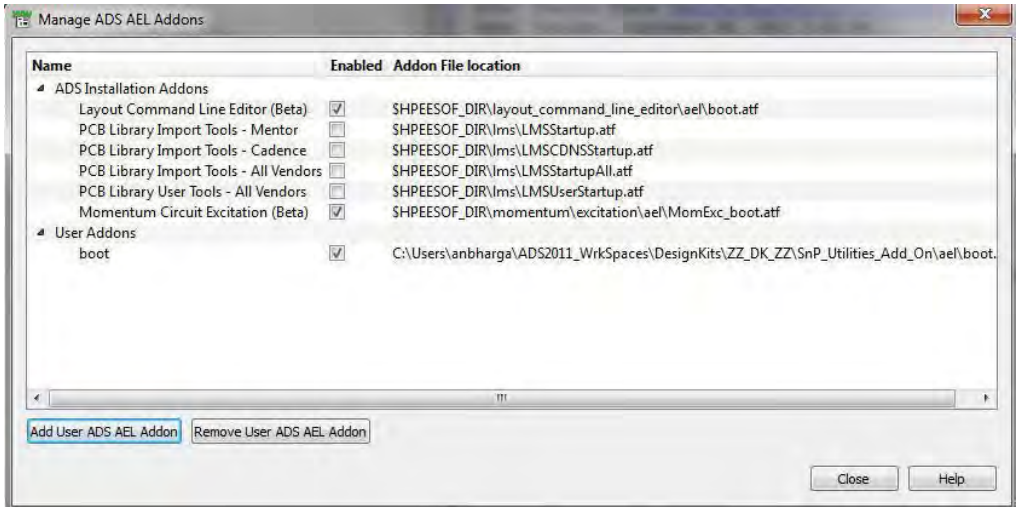
f. Run simulation and plot BER vs BER.DF.EbN0 as shown below ***(Don't forget to change the Y-axis to log type)***



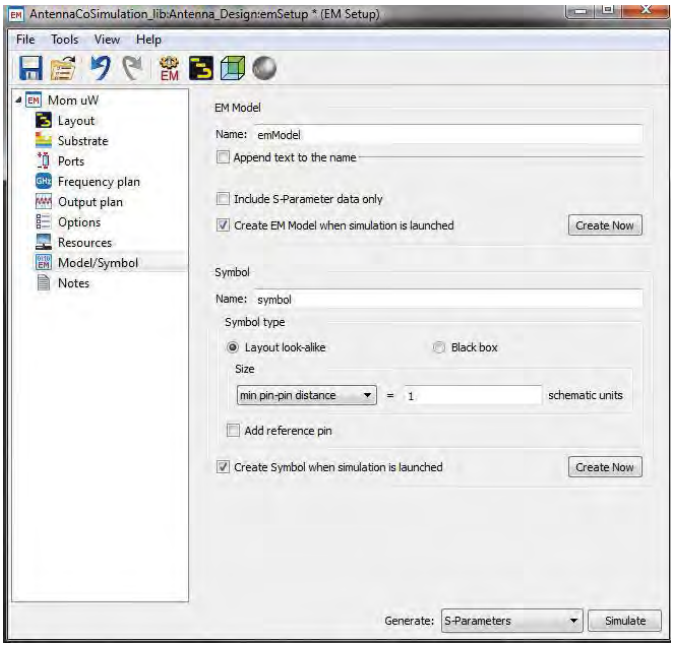
Appendix

Appendix-A: Antenna Pattern with Circuit Components in ADS2011

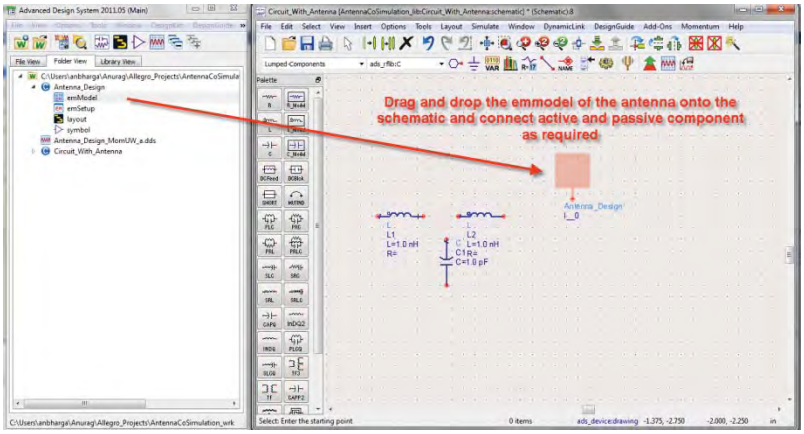
1. From the ADS Main Window, select **Tools->Manage ADS AEL Addons** and select Momentum Circuit Excitation(Beta) and shown below.



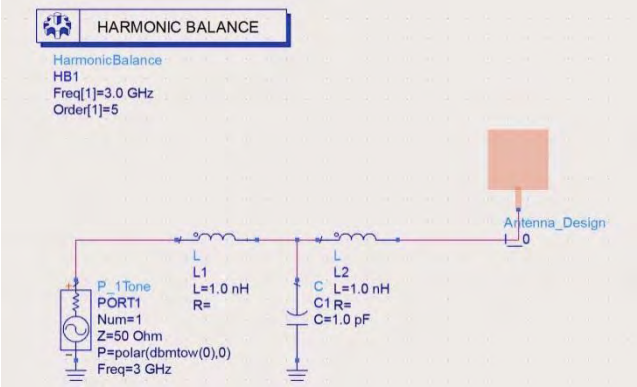
2. Create a new workspace and create the Antenna design in the layout and set the EM simulation as you normally do by setting up the substrate, simulation frequencies…please take care of adding specific frequency of interest because it may happen than frequency of interest may not appear in the list because of adaptive sweep.
3. In the model/symbol tab of the EM setup…….do following:
    a. Unselect Include S-Parameter data only
    b. Select Create EM Model when simulation is launched
    c. Select Create Symbol when simulation is launched



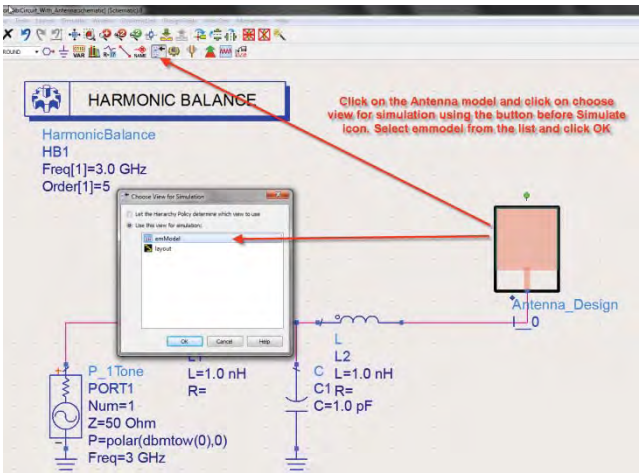
4. Click on Simulate to run Momentum simulation and check the S-Parameter results.
5. Once the simulation is finished “emmodel” will be created in the cell as shown. Drag and drop the same on to a new schematic cell and place the desired active or passive components.



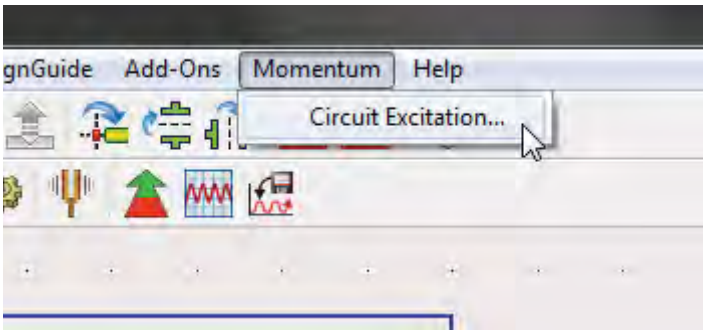
6. Connect the components and setup the AC or HB simulation as desired (shown below)



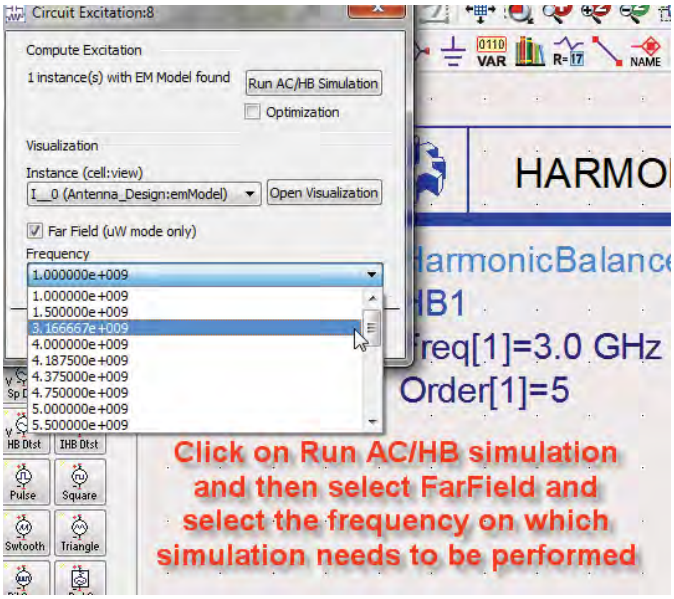
7. Click on the EM model and click on Choose View for Simulation and select “emmodel” from the list as shown below.



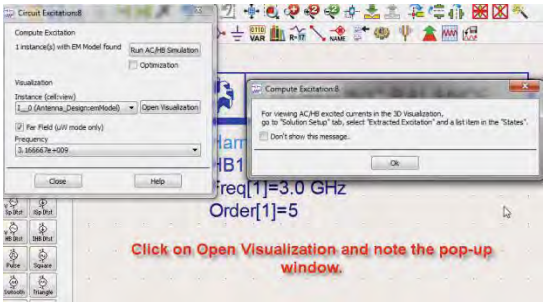
8. Because we selected Momentum AEL Addon, you should be able to see Momentum menu on the Schematic. Click on Momentum->Circuit Excitation



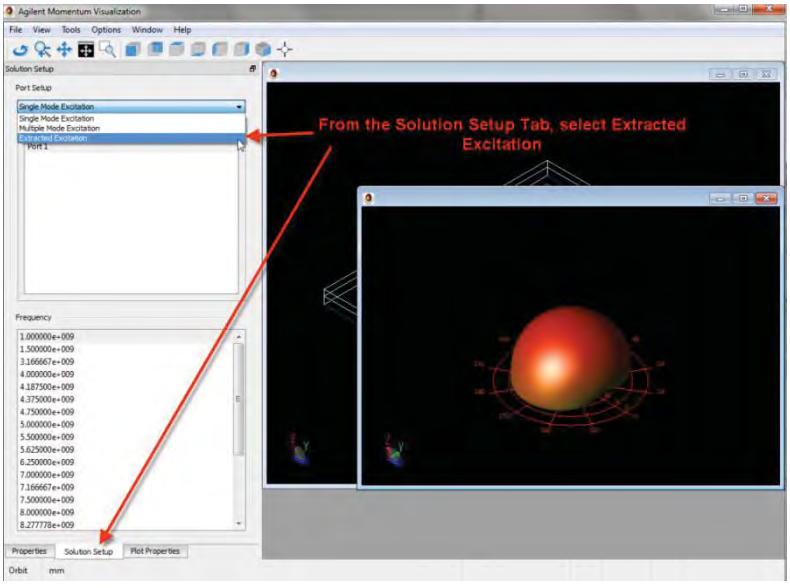
9. In the pop-up window, click on Run AC/HB Simulation and once it finished Visualization fields will be active. Click on Far Field and select the desired frequency from the list and click on Open Visualization



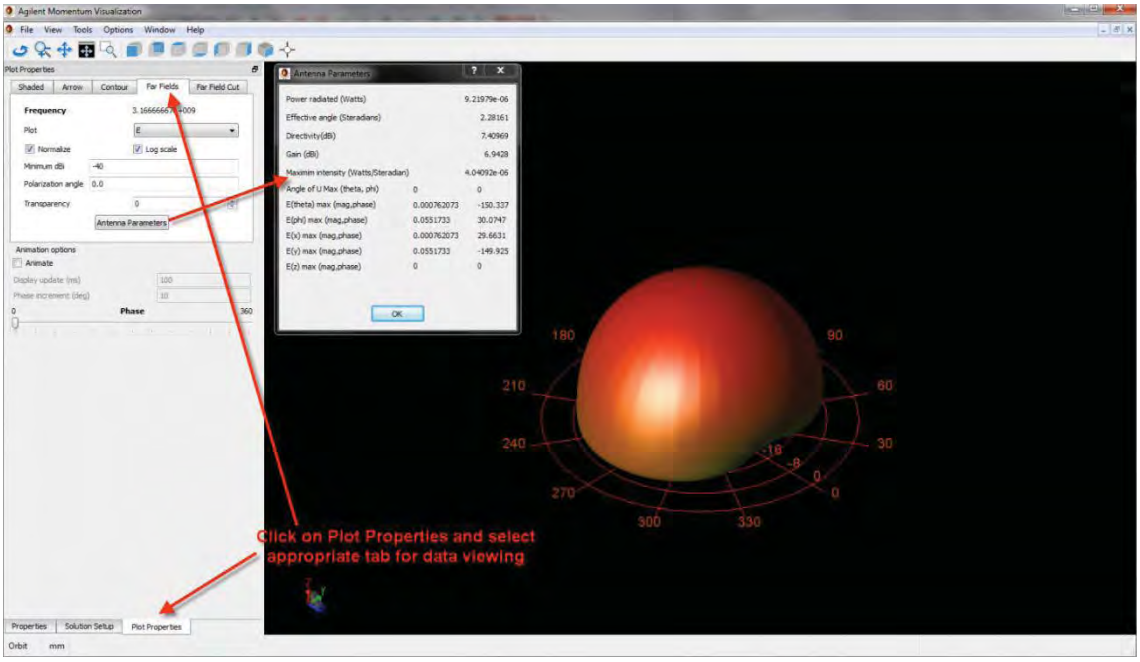
10. Make note of the message in the pop up window.



11. Far field window will open up…select Extracted Excitation from the Port Setup under the Solution Setup tab as shown below



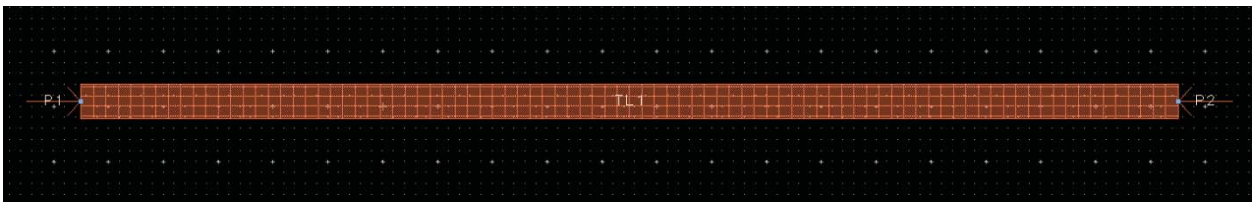
12. Go to Plot Properties to see various plotting options and getting Antenna Parameter (button) to see various Antenna parameters like Gain, Directivity etc….



Appendix-B: How to perform De-embedding in ADS

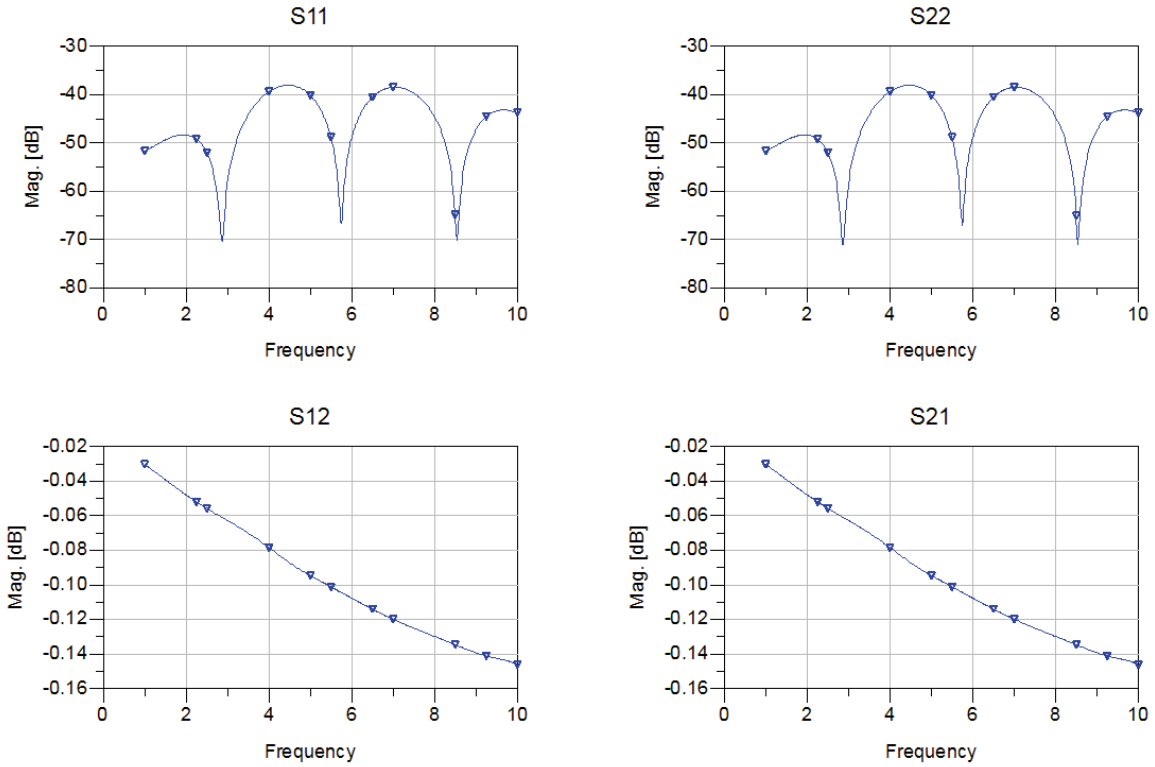
Step1:

Prepare the layout 1 e.g. 20mm line as shown below. Setup the substrate and setup the simulation condition such as Edge Mesh, S-parameter start & stop etc



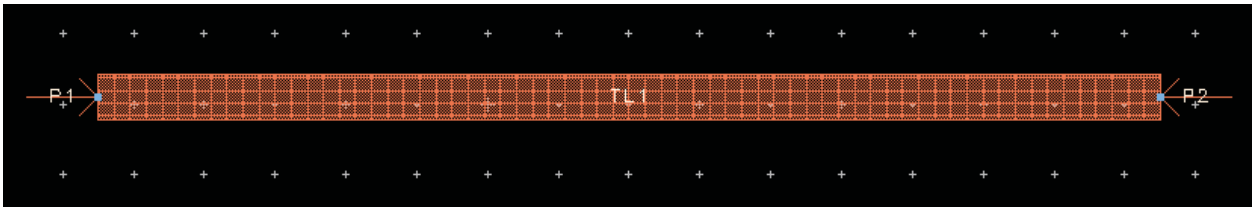
Step2:

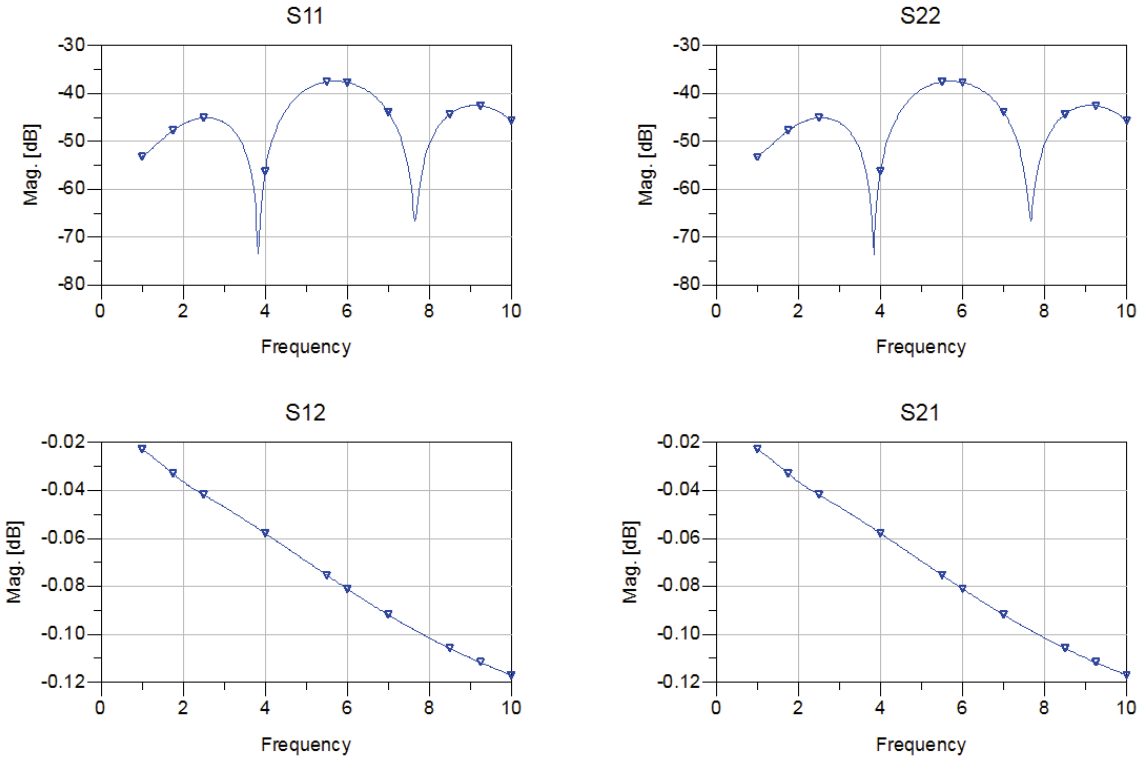
Run Momentum simulation and observe the data display as shown below.



Step3:

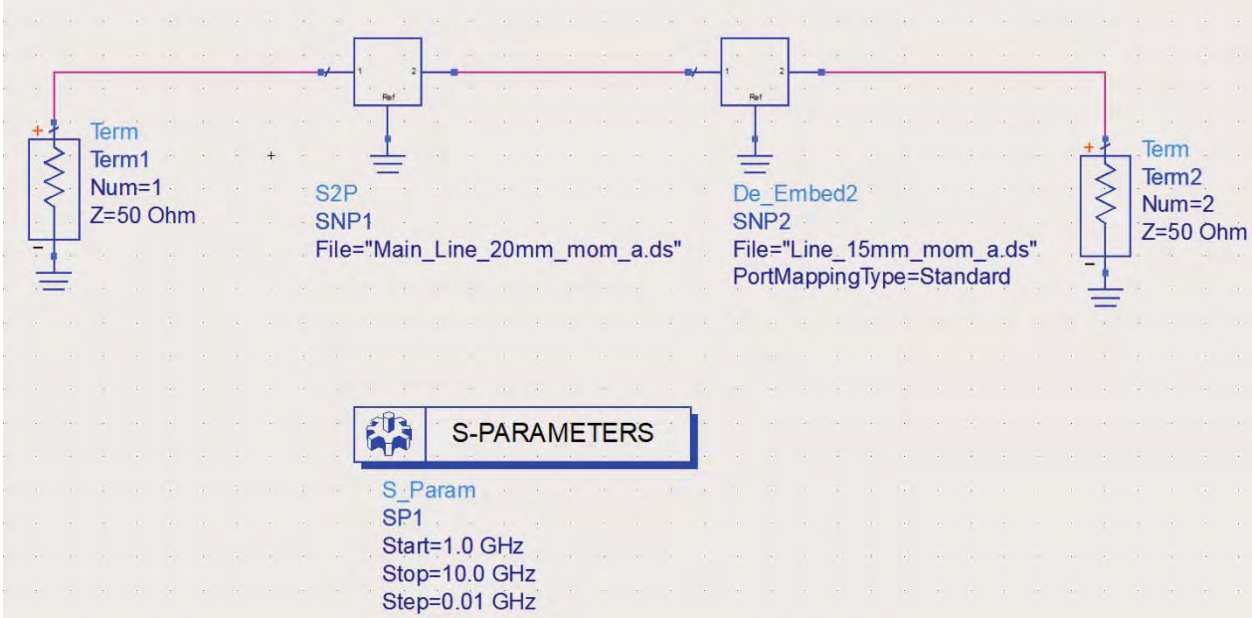
Similarly prepare 15mm line layout and use the same substrate and other simulation settings. Run simulation and observe the data display.



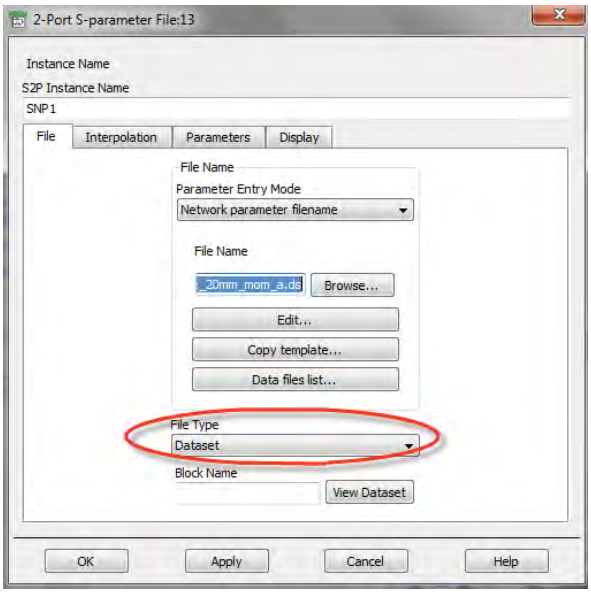


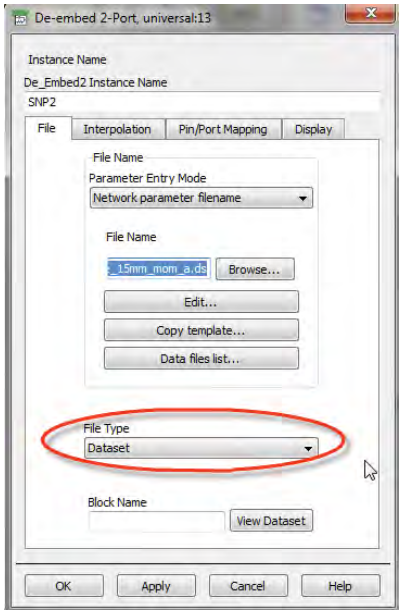
Step 4:

Prepare schematic for De-embedding as per the designs. In our case the original line (20mm) and the line to de-embed (15mm) both are of 2 ports hence we need to place following components from Data Items library as shown in next graphics.

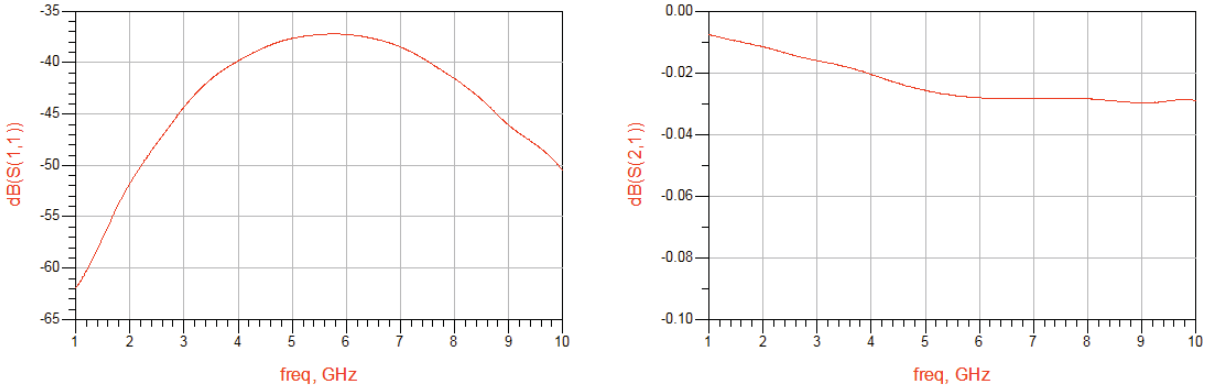


Double click on S2P component and change the File Type = Dataset, browse to the 20mm momentum simulation dataset. Similarly for 2-port Deembed component and change the File Type=Dataset and browse to the file which needs to be de-embedded (15mm in our case).



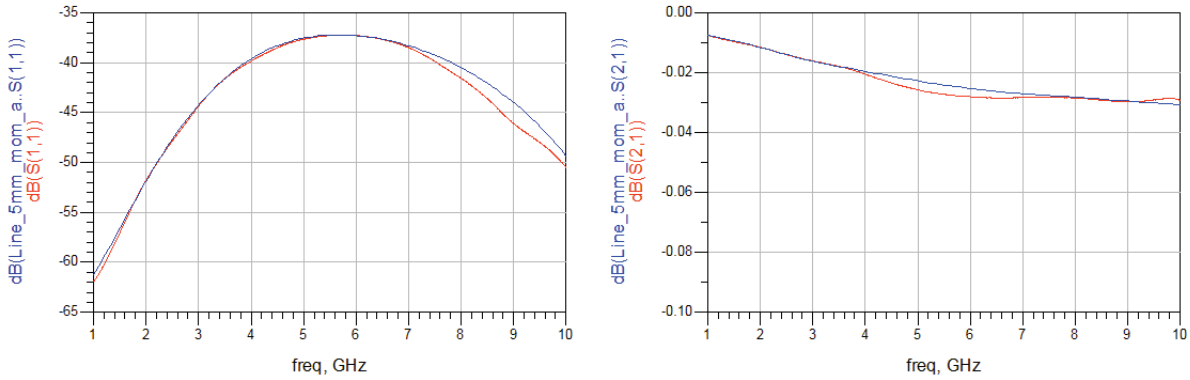


Setup the S-parameter simulation to see de-embedded results.



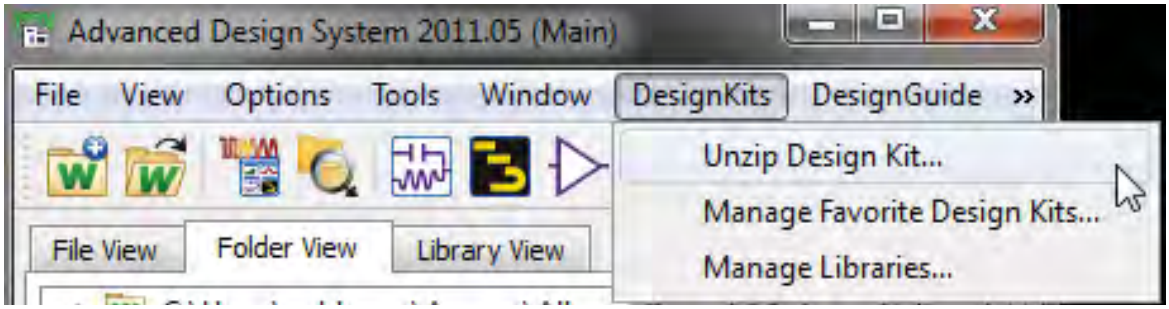
Verification of the De-embedded Results:

In order to check the results, create a 5 mm line in layout and perform simulation and compare the momentum simulation results of 5mm with de-embedded results as shown below

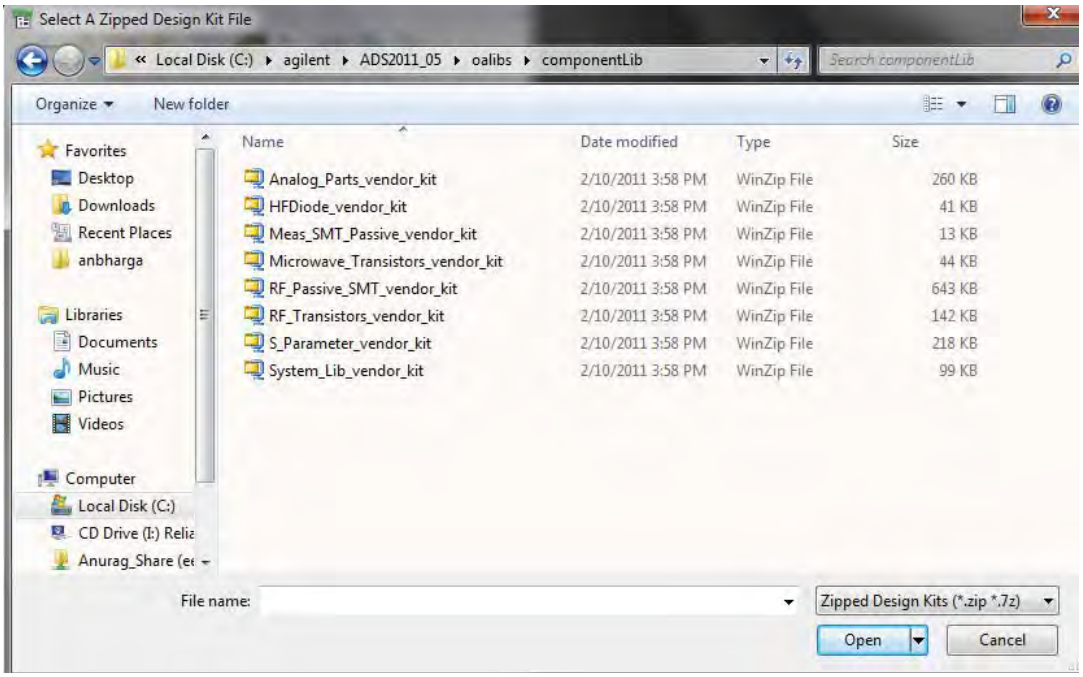


Appendix-C: How to use Vendor Component Libraries in ADS2011

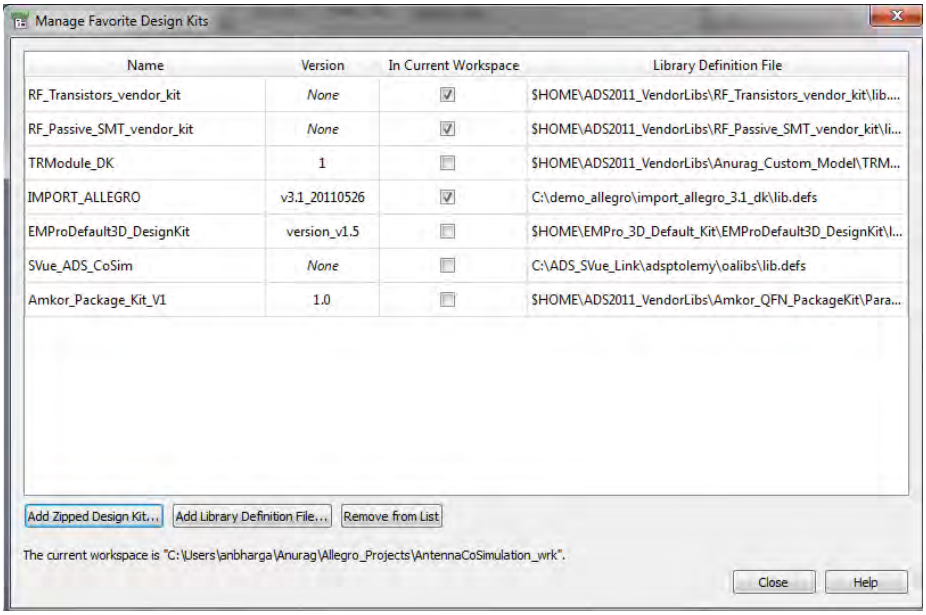
1. ADS2011 uses different methodology for Vendor component libraries which sometimes causes confusion to the existing users of ADS who have used earlier ADS releases.
2. All vendors libraries which were present by default in earlier ADS releases are now provided in a zipped format and it is recommend for designers to unarchive them at a central location (specific folder)
3. All zipped libraries are located at <ADS install dir>/oalibs/componentLib folder (e.g, C:\Agilent\ADS2011.05\oalibs\componentLib…please note that ADS2011.05 will be as per the version you may be using), in order to unarchive them, go to ADS Main Window and select DesignKit->Unzip Design Kit…



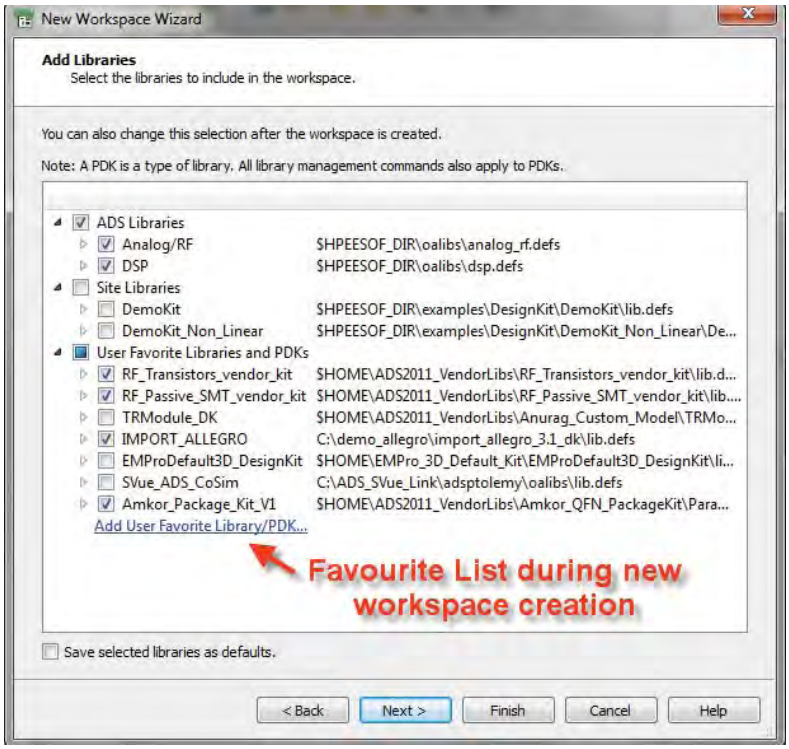
4. Browse to the location as mentioned as mentioned above, select the library to unarchive and click on Open, provide the location/directory where you need to unarchive the library. Repeat the steps for all needed libraries.



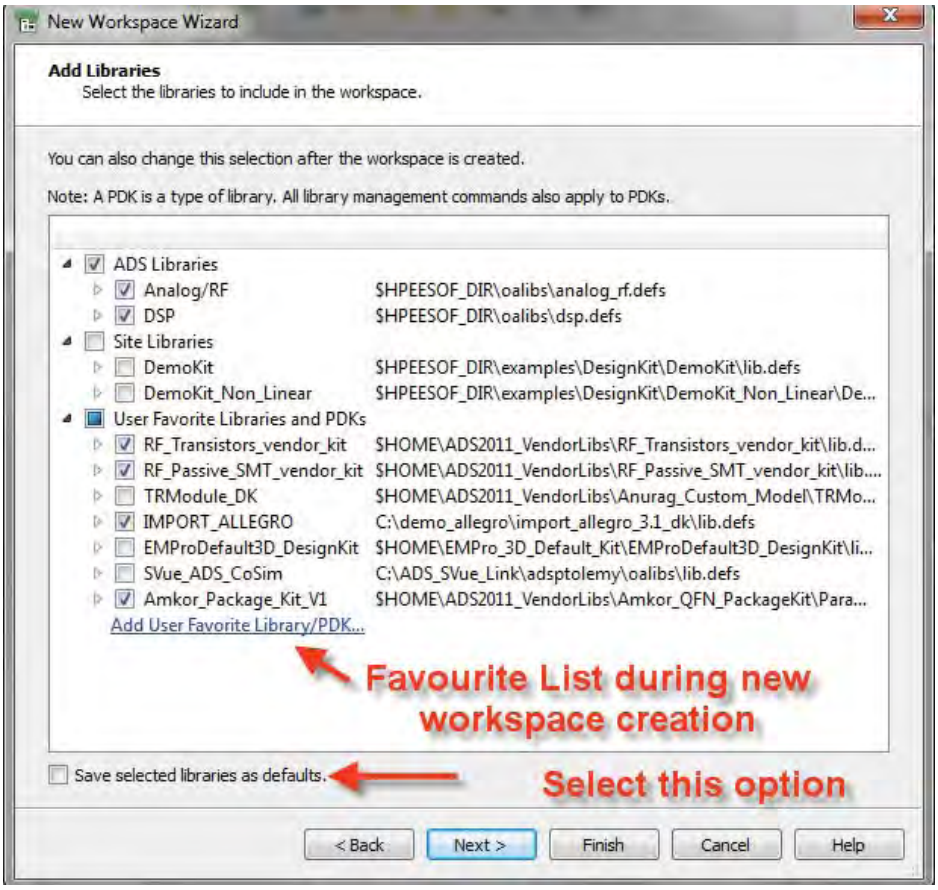
5. Once done, we can add all these libraries in our favourite list by going to DesignKit->Manage Favourite Design Kits as shown below



6. If your desired library is not appearing in the list, we can click on Add Library Definition File and then go to the folder where we have unarchived the library. Each unarchived library folder will have lib.defs file which is the file we need to point to. We can do this for all needed library so that they will appear in the favourite list while we create new workspace for easy selection as shown below:



7. If these libraries are needed on regular basis then it will be good idea to select the option “Save Selected libraries as defaults”, this option will add the currently selected libraries in all the workspaces which we create from next time onwards.



8. All 3rd party libraries which are available from various vendor websites like Freescale, Murata etc can be added to the favourite list similarly to the process defined above and please note that each of those libraries will have lib.defs file after unzip process.

www.agilent.com
Product specifications and descriptions in this document subject to change without notice.

Published in USA, November 8, 2012
5991-1516EN