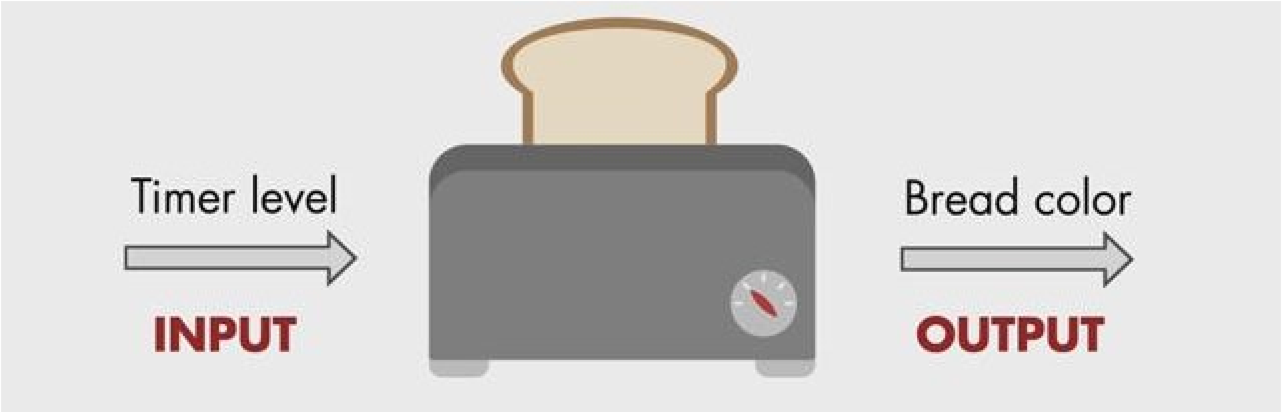
Robust Mechatronics

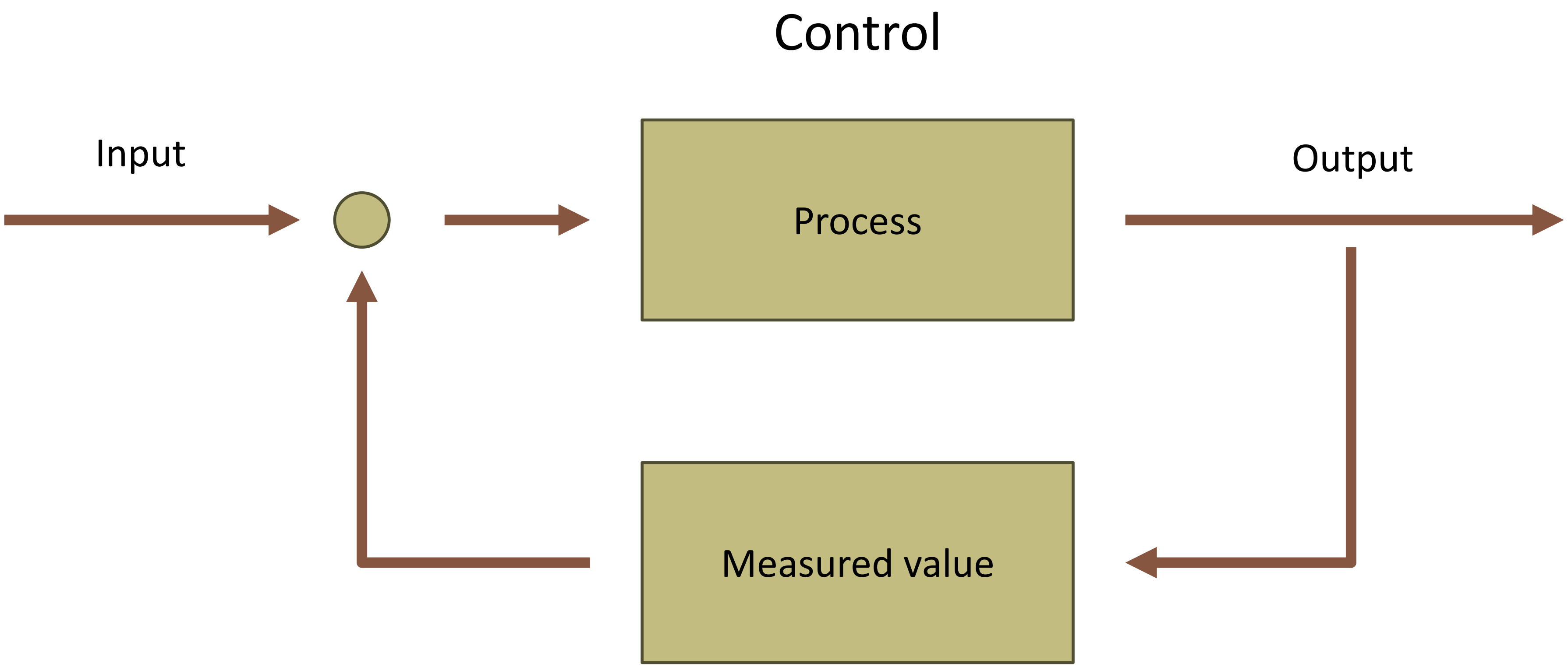
Mechatronics Automation



Dr Loukas Bampis, Assistant Professor
Mechatronics & Systems Automation Lab

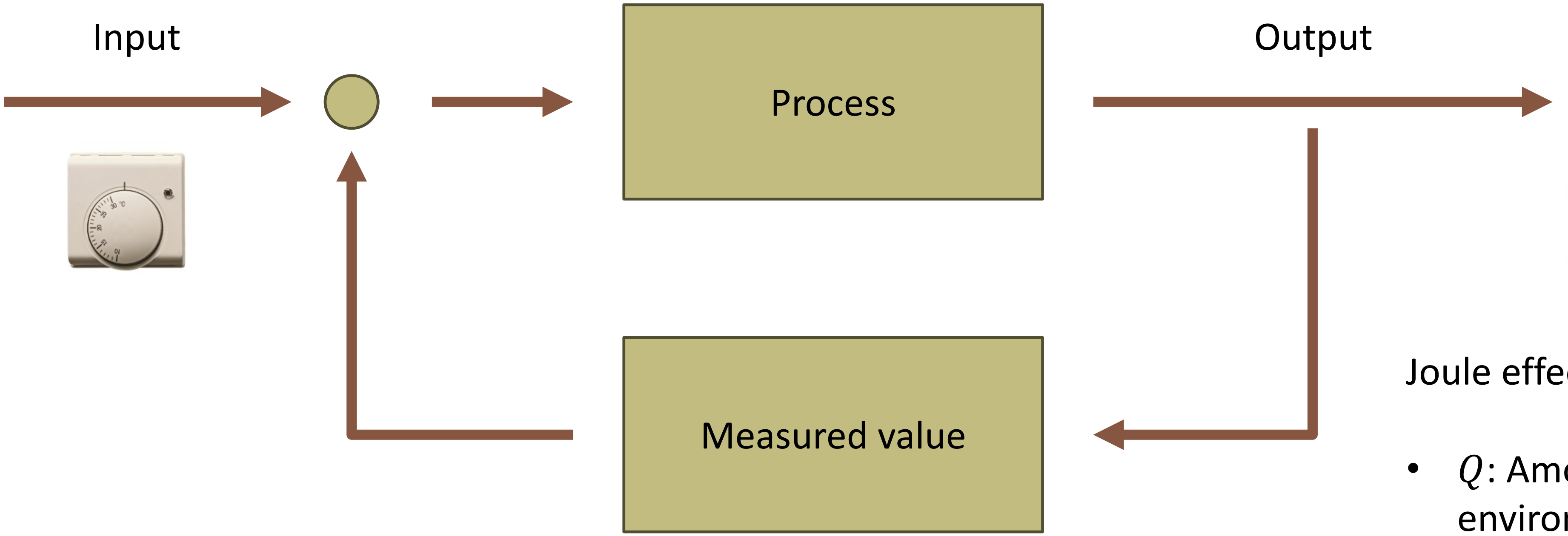
Mechatronics Automation

Automation system



Automation system

Space heating to desired temperature

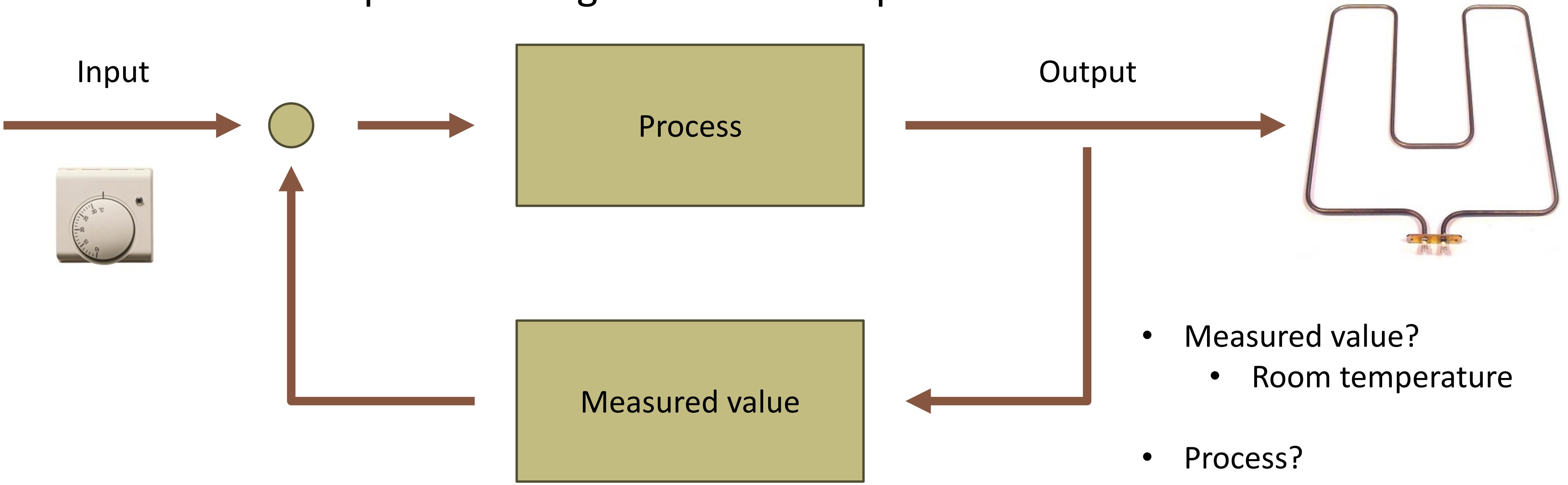


Joule effect: $Q = I^2 \times R \times t$

- Q: Amount of heat transferred to the environment
- I: Current
- R: Resistance
- t: Current transit time

Automation system

Space heating to desired temperature



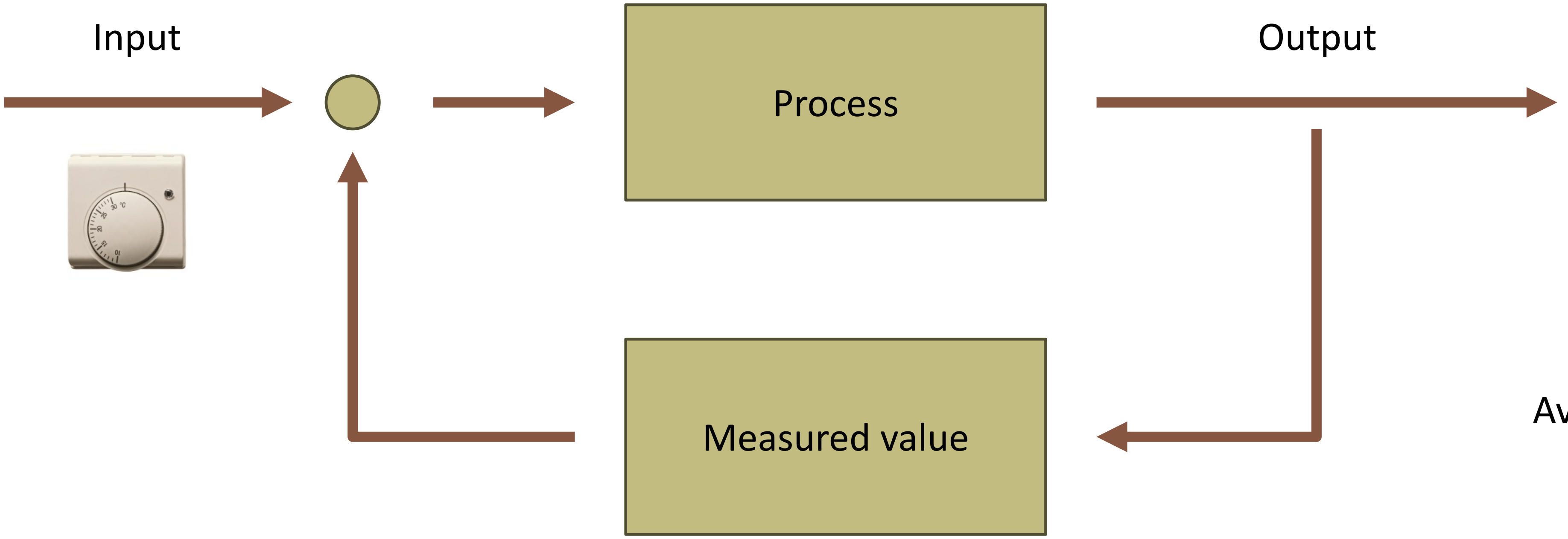
- Measured value?
  - Room temperature

- Process?
  - Comparison of desired temperature with room temperature
  - Enable or disable resistor

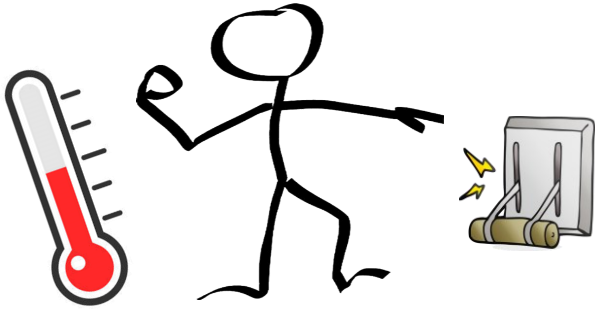
Mechatronics Automation

Automation system

Space heating to desired temperature

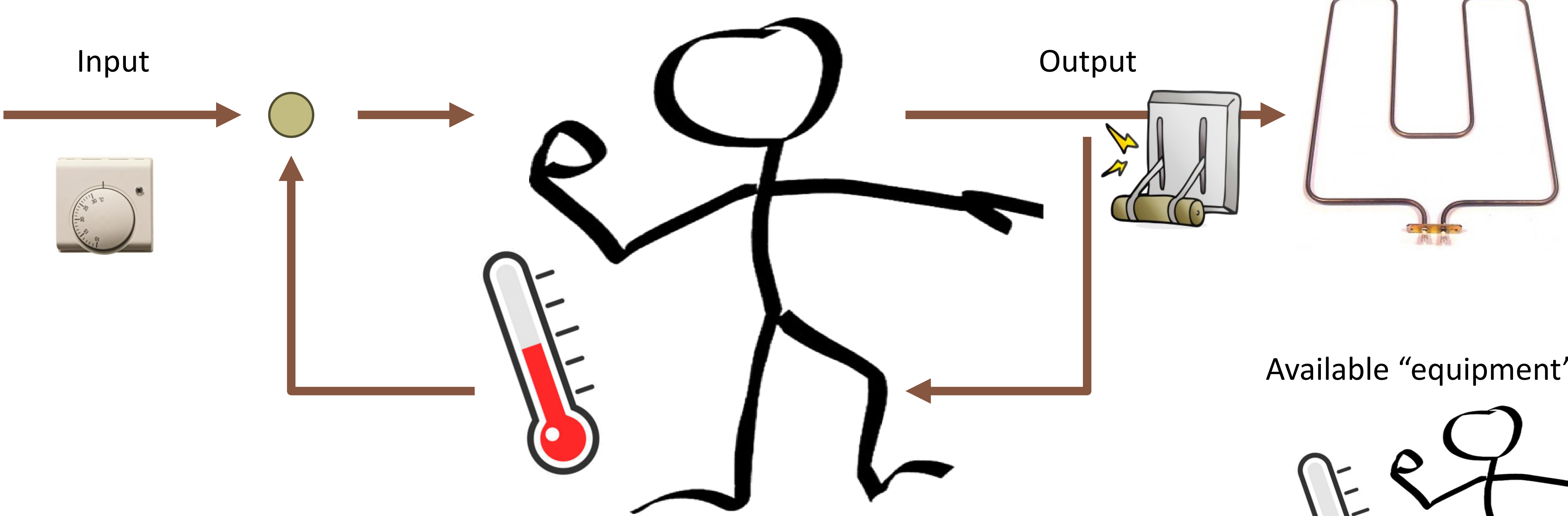


Available “equipment”:

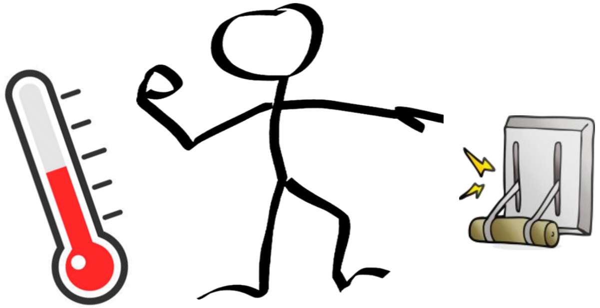


Automation system

Space heating to desired temperature



Available “equipment”:



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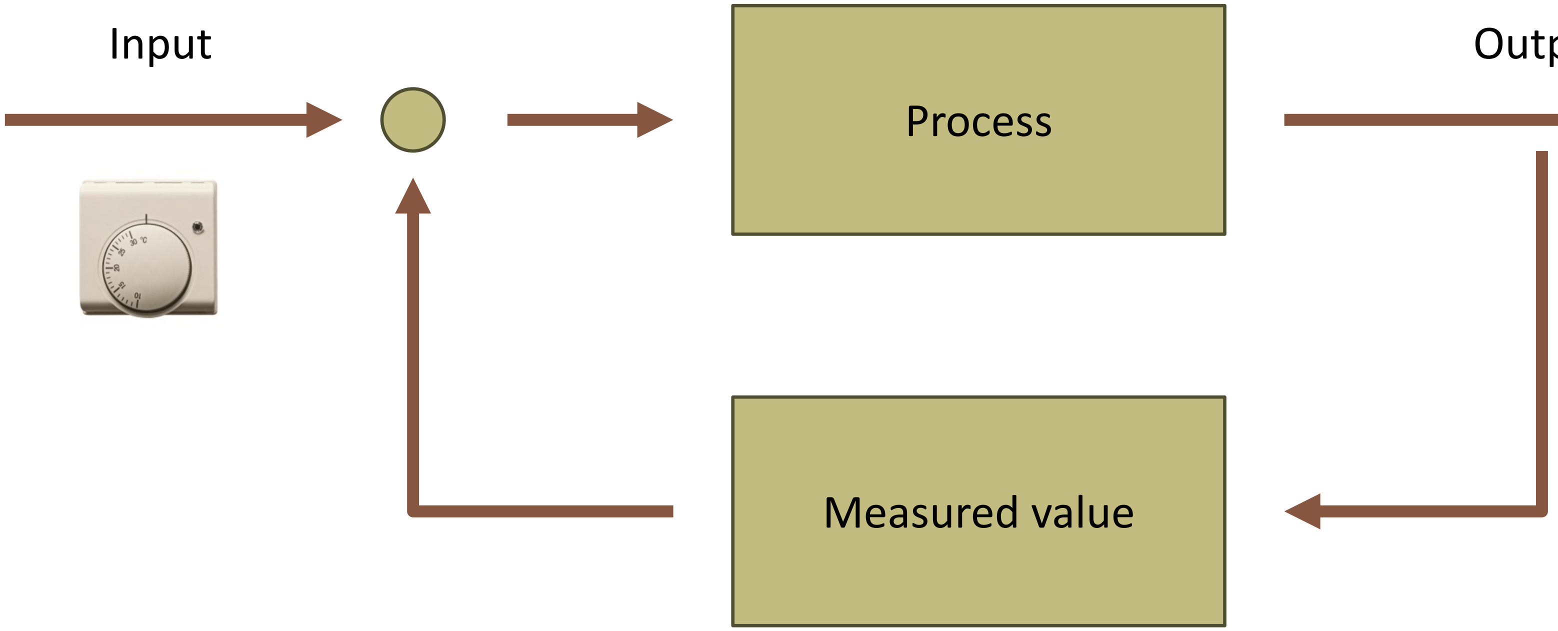
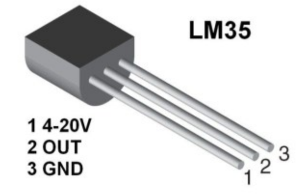
Automation system

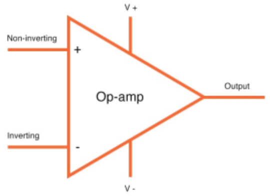
Space heating to desired temperature

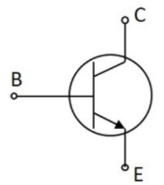


Available “equipment”:

- Sensors
- Electronic components
- Power electronics components



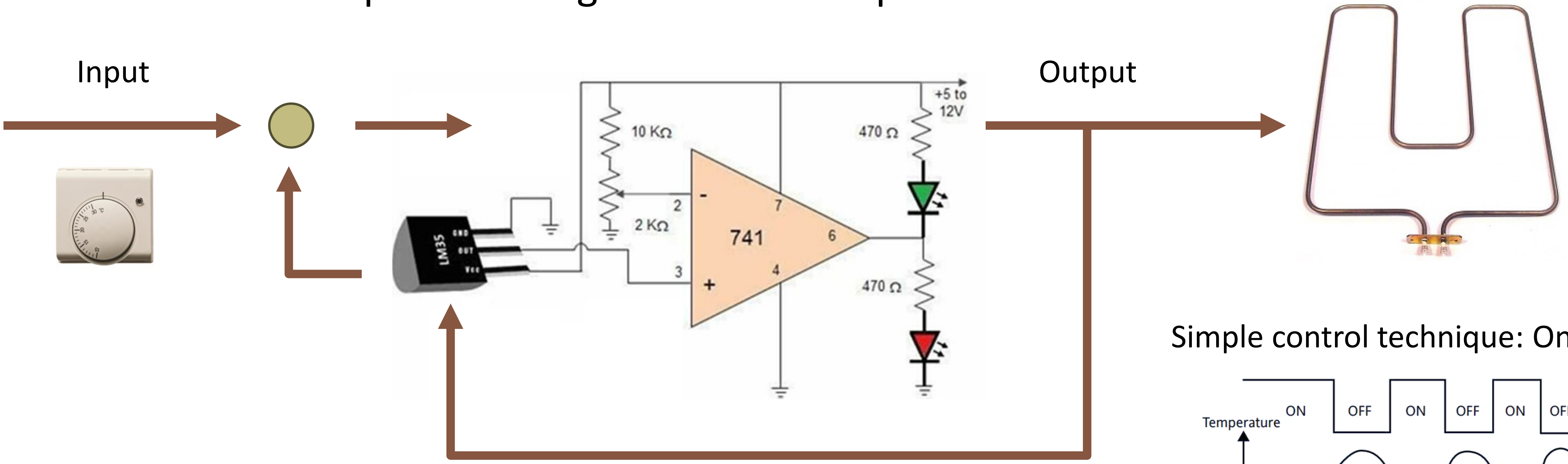




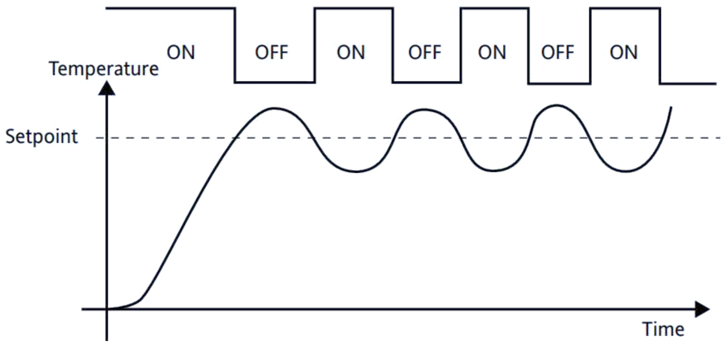
Mechatronics Automation

Automation system

Space heating to desired temperature

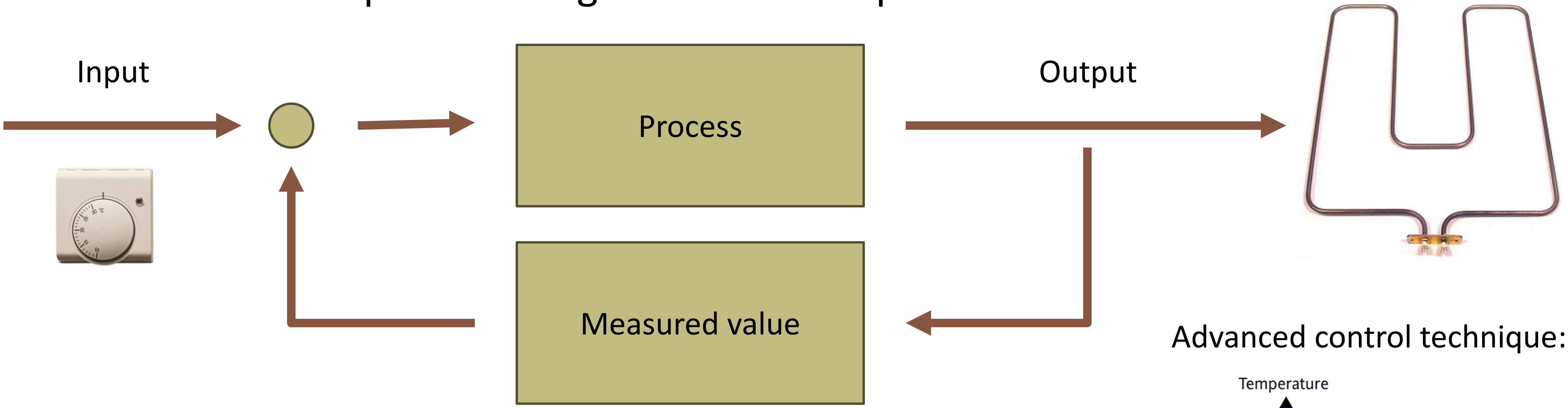


Simple control technique: On/Off Control



Automation system

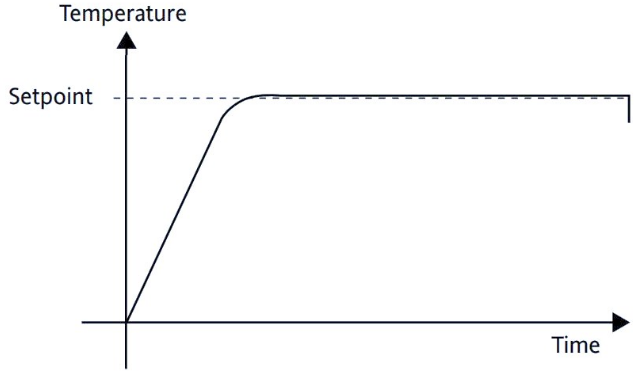
Space heating to desired temperature



How would we achieve more advanced control techniques?

- PID Control
- Operation only when the space is not empty
- Change the desired temperature under specific cases
- Memory/history retention

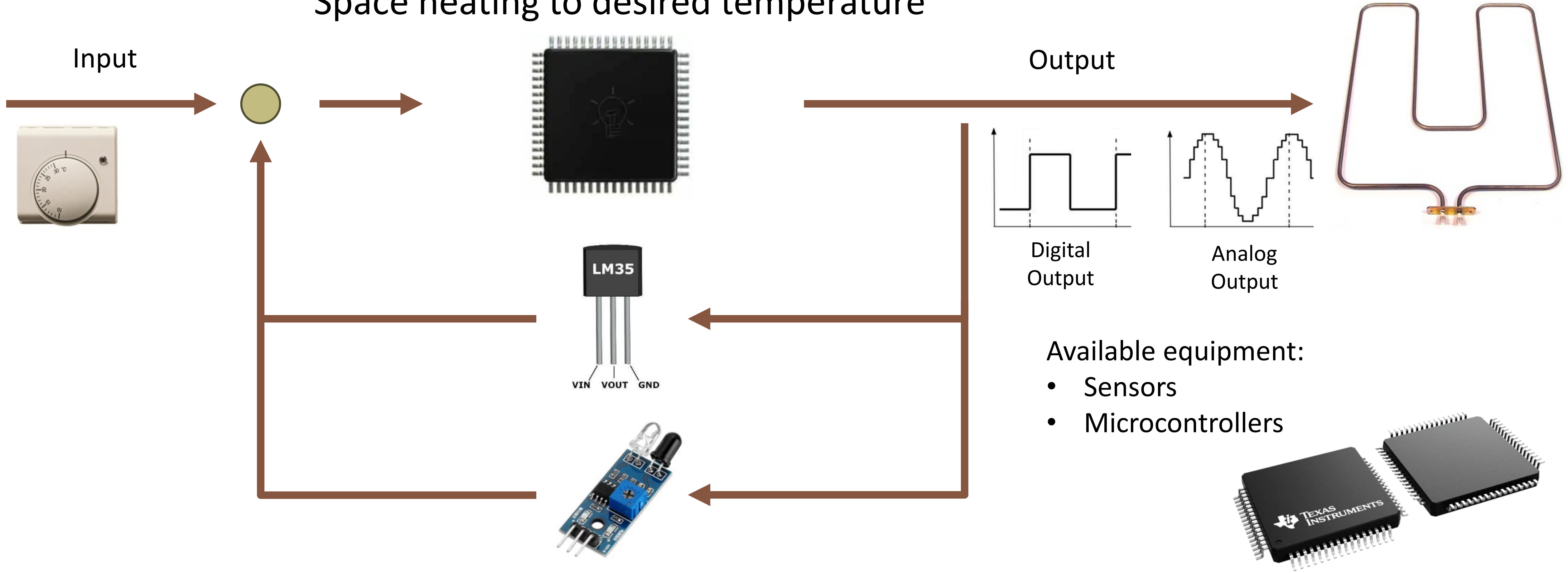
Advanced control technique: PID



Mechatronics Automation

Automation system

Space heating to desired temperature



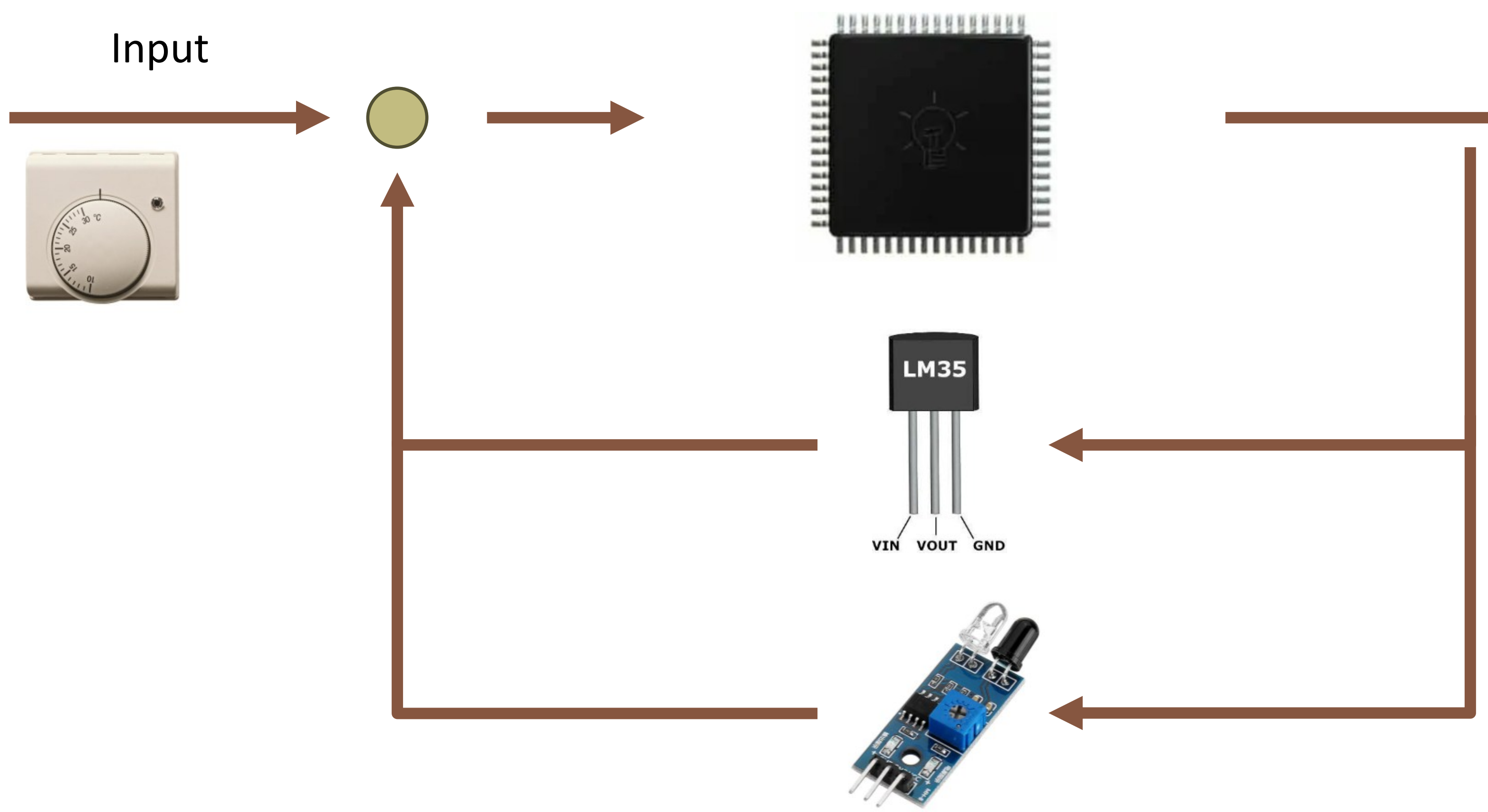
Available equipment:

- Sensors
- Microcontrollers

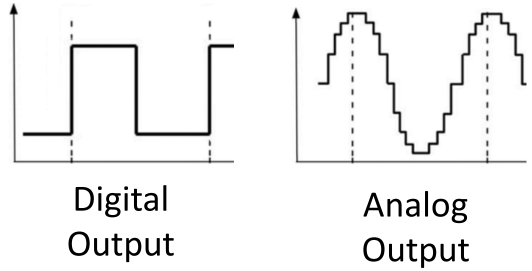
Mechatronics Automation

Automation system

Space heating to desired temperature

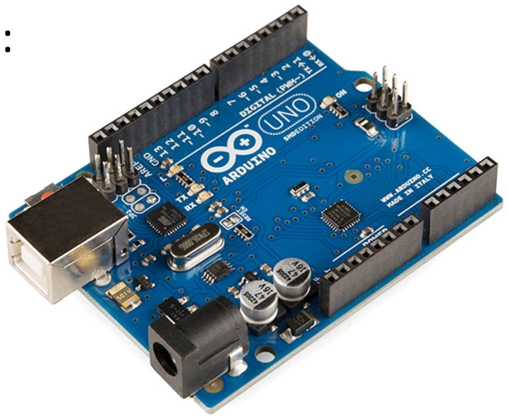


Output



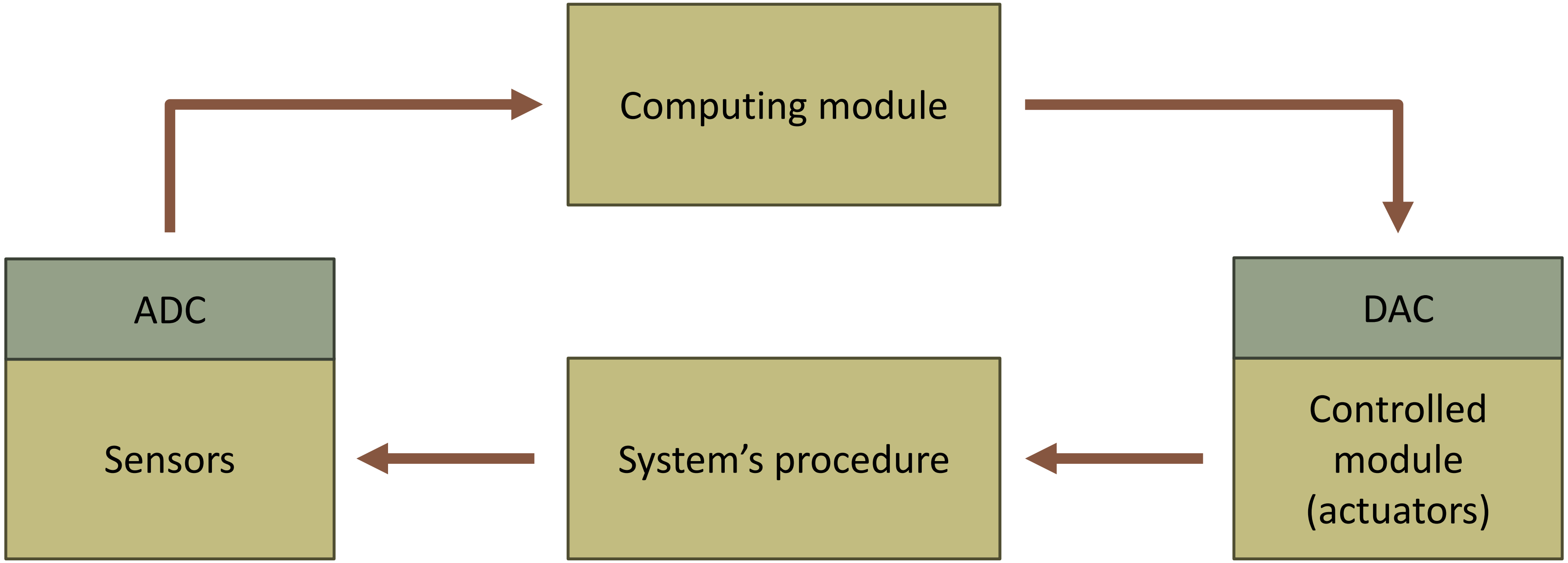
Available equipment:

- Sensors
- Microcontrollers



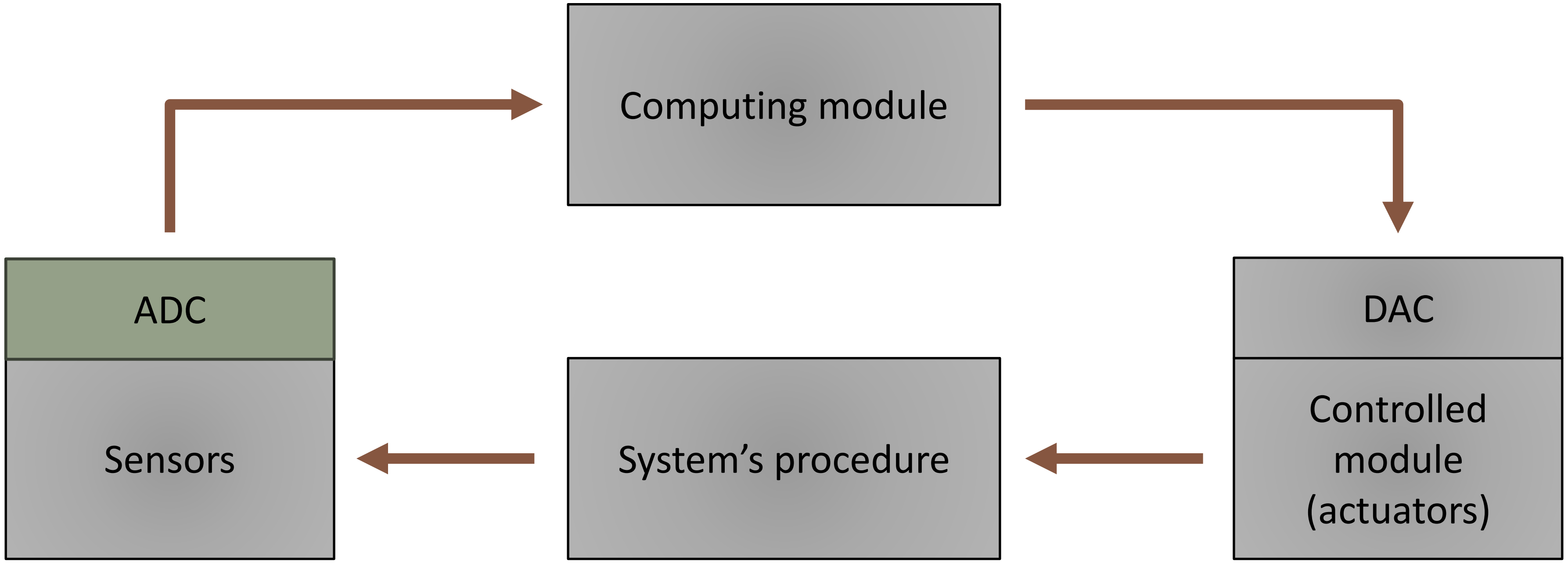
Mechatronics Automation

Control loop

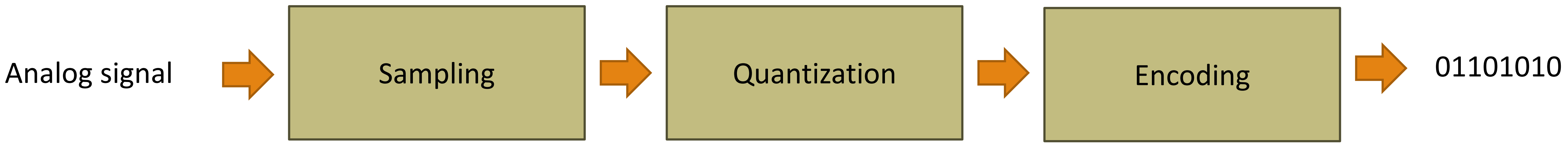


Mechatronics Automation

Control loop

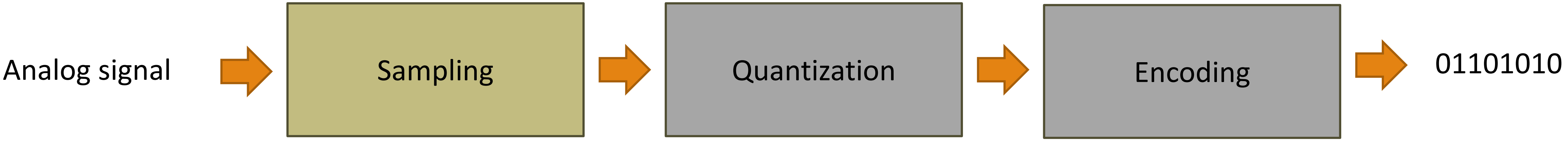


Analog to Digital Converter (ADC)



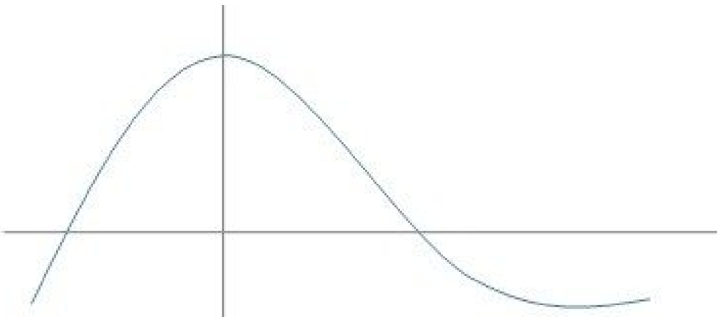
- Goal:
  - For an analog input signal
  - Produce the respective digital encoding

Analog to Digital Converter (ADC)

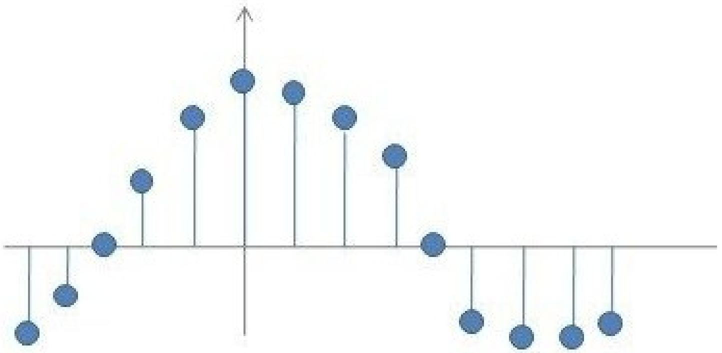


- Goal :
  - Convert a continuous input signal
  - In a discrete output signal

Continuous Signal?



Discrete Signal?



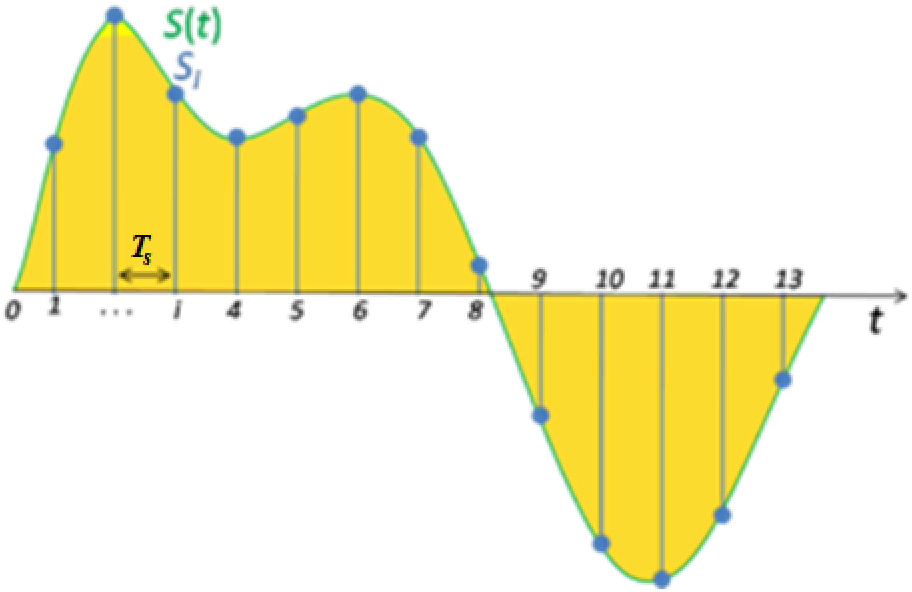
Analog to Digital Converter (ADC)

Analog signal → Sampling → Quantization → Encoding → 01101010

- Taking samples from an analog signal at specified time intervals
  - Sampling period T_s
  - Sampling frequency f_s
- Shannon's theorem: $f_s \geq 2 * f_{max}$
  - Nyquist Frequency:
    The highest frequency that can be sampled

$$f_n = f_s/2$$

- Result
  - Continuous in time analog signal →
    Discrete signal (discrete in time but continuous in amplitude)



Analog to Digital Converter (ADC)

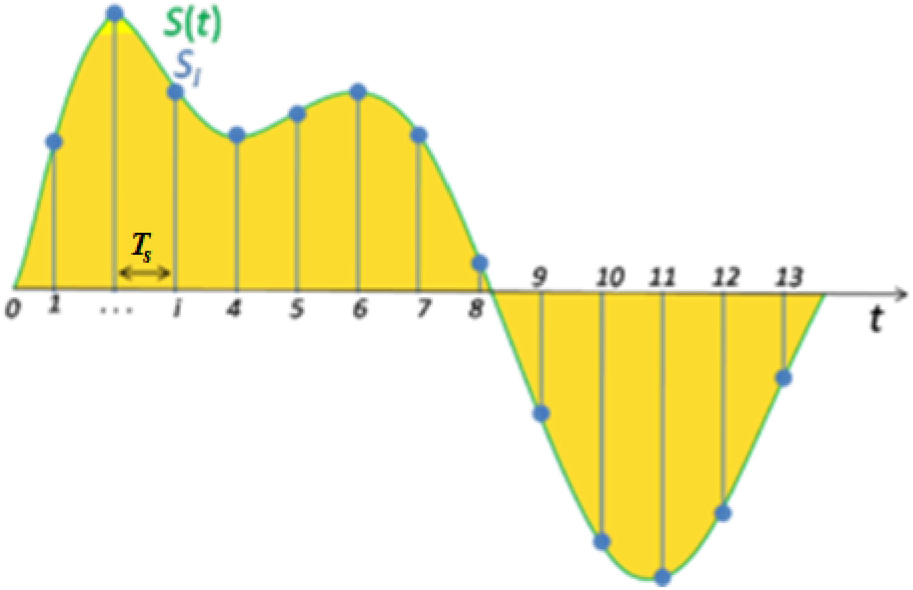
Analog signal → Sampling → Quantization → Encoding → 01101010

Is a discrete signal also digital?

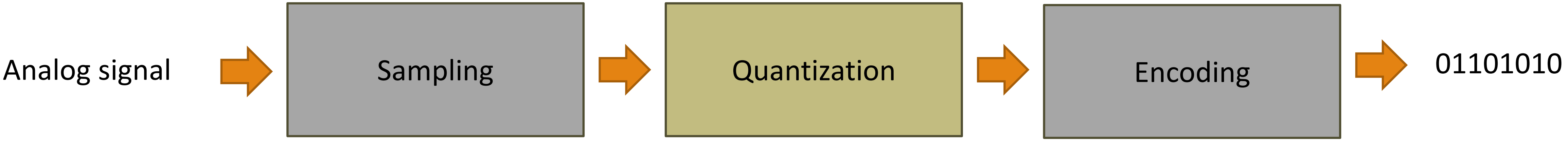
- Discrete time signal

  VS

- Discrete value signal

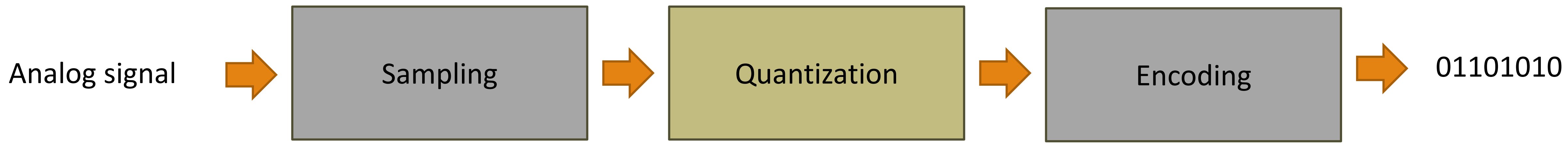


Analog to Digital Converter (ADC)



- Goal:
  - Categorization of input signal values
  - at different output levels

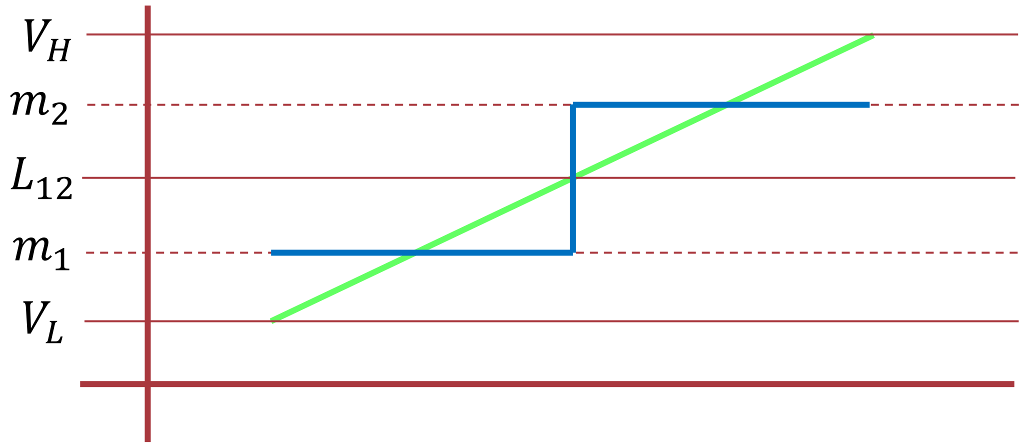
Analog to Digital Converter (ADC)



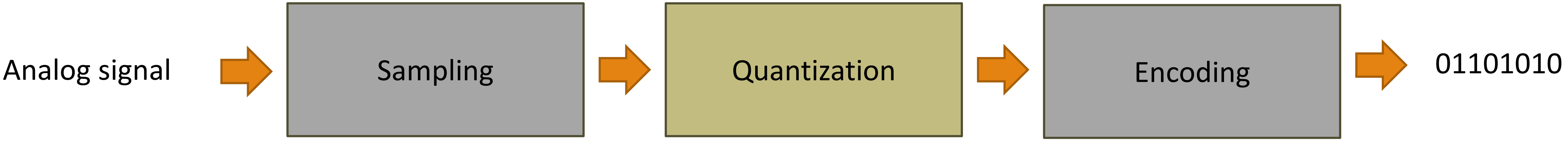
- Suppose I want to divide an input signal into two categories
  - Low Level and
  - High Level

- Steps:
  - What is the range of the signal? → V_L and V_H
  - How many are the categories (levels)? → Let 2: m_1 και m_2
  - How do I want to distribute them? → Let uniformly
  - How many threshold values should I compare with?

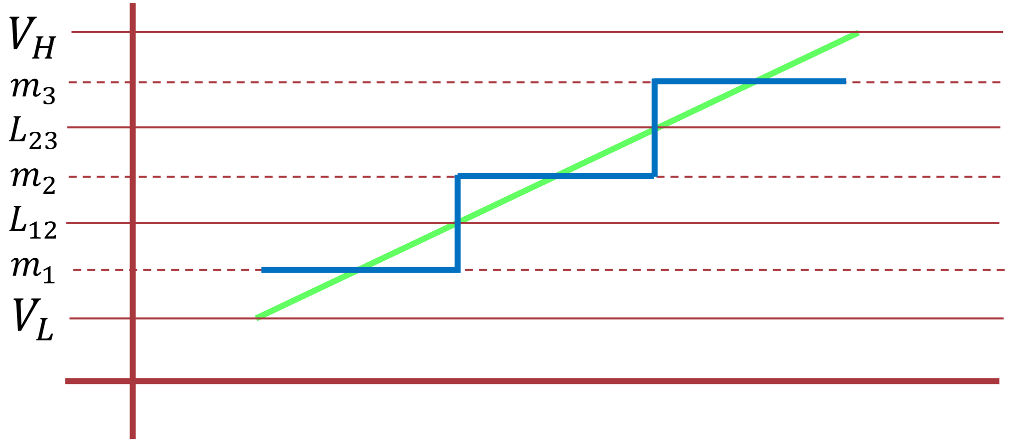
    → For 2 levels: 1 (L_{12})



Analog to Digital Converter (ADC)

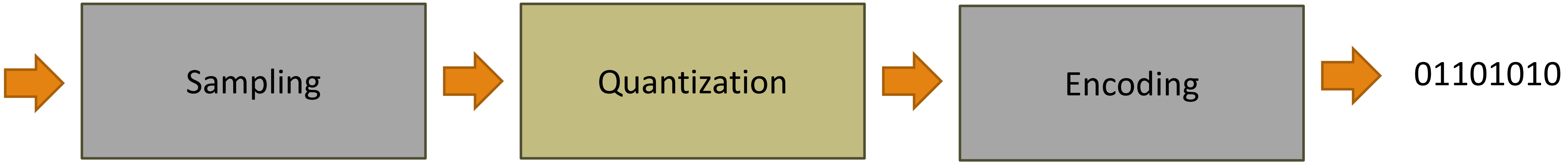


- Suppose I want to divide an input signal into three categories

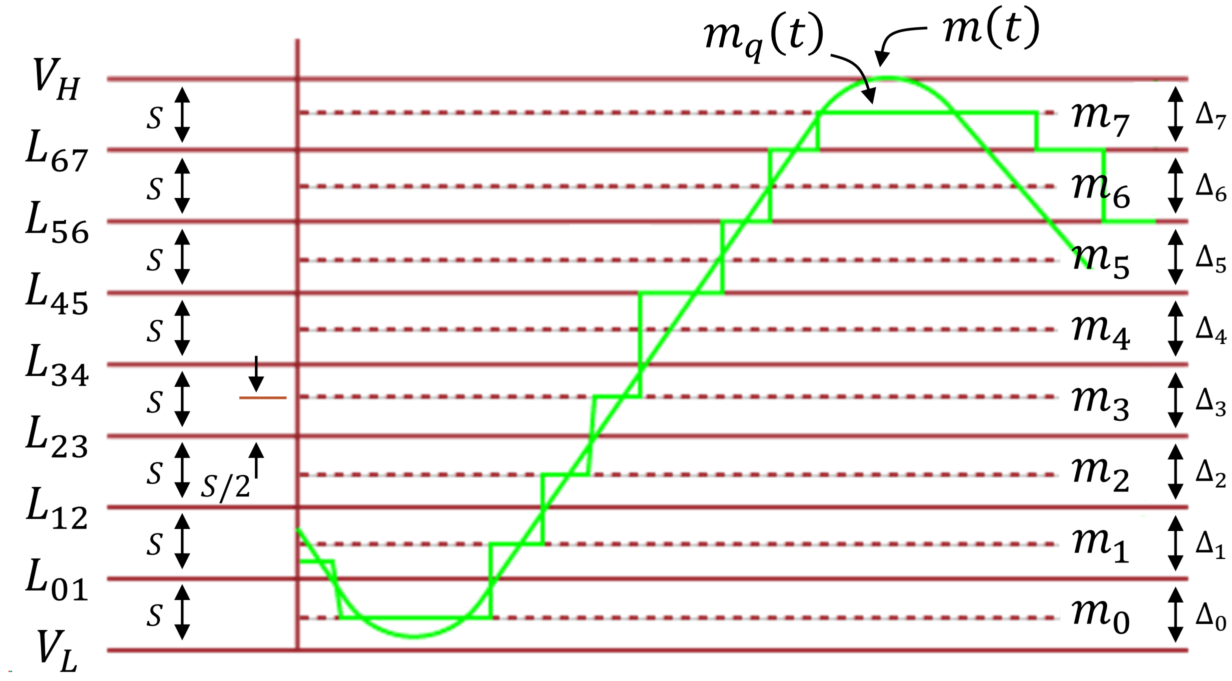


- Steps:
  - What is the range of the signal?
  - How many are the categories (levels)?
  - How do I want to distribute them?
  - How many threshold values should I compare with?

Analog to Digital Converter (ADC)



- Intervals and levels:
  - M = Intervals $(\Delta_0, \Delta_1, \ldots, \Delta_{M-1})$
  - M = Quantization levels $(m_0, m_1, \ldots, m_{M-1})$ in the middle of the intervals
- Quantization interval distribution: Equal intervals → Uniformly quantized signal
  - Interval size: $S = \frac{V_H - V_L}{M}$
- $m_q(t)$ = closest level to $m(t)$
- Quantization Error:
  - $e = m(t) - m_q(t), \ |e| \leq S/2$



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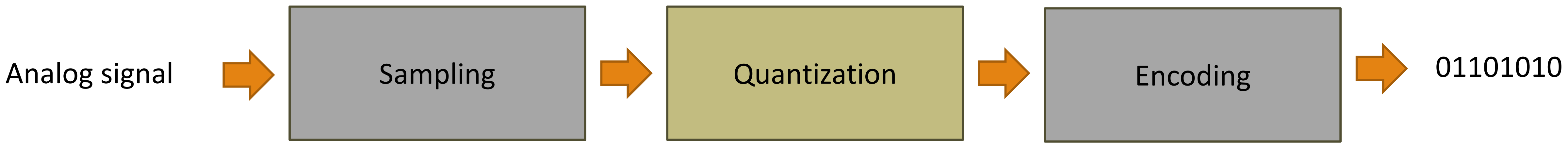
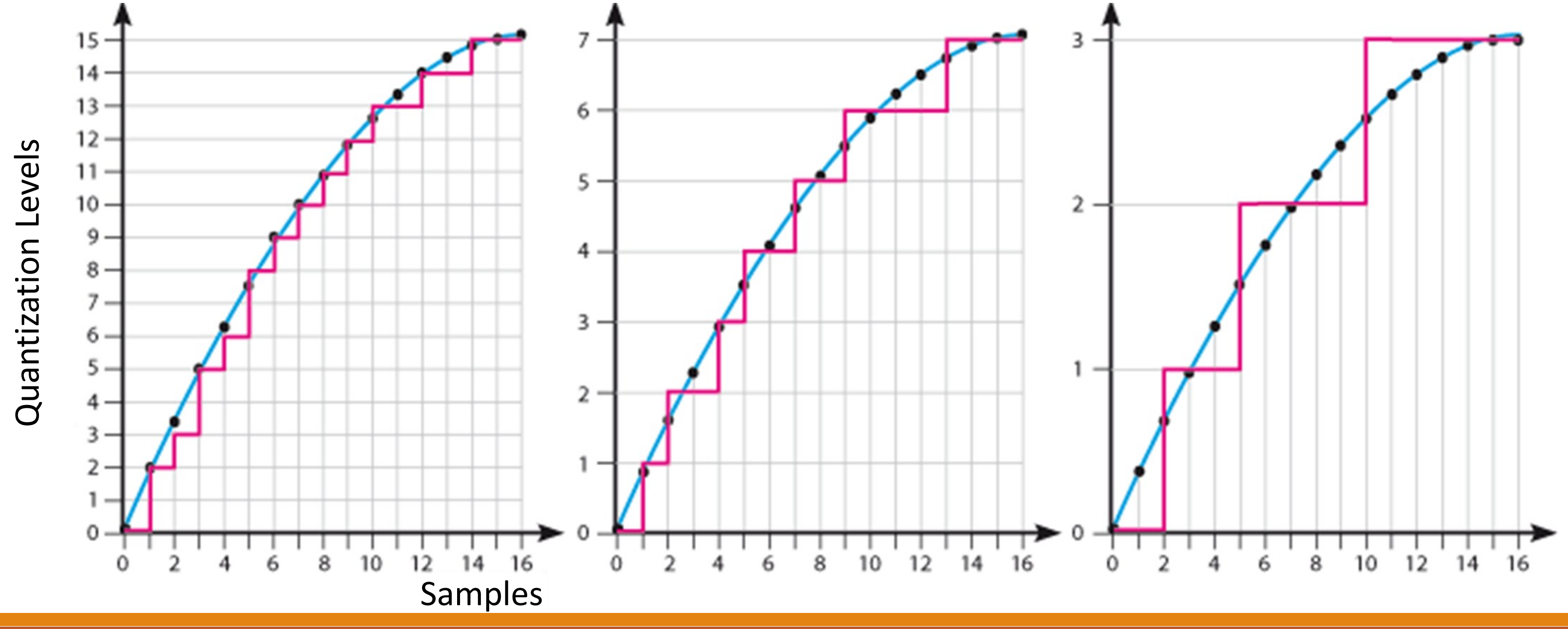
Analog to Digital Converter (ADC)



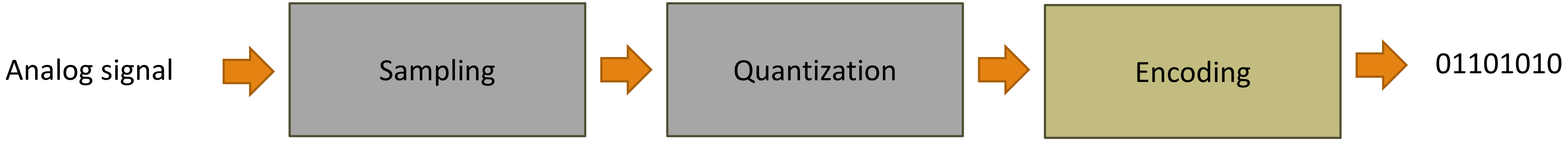
16 Quantization Levels | 8 Quantization Levels | 4 Quantization Levels



For the same signal range, the following holds:

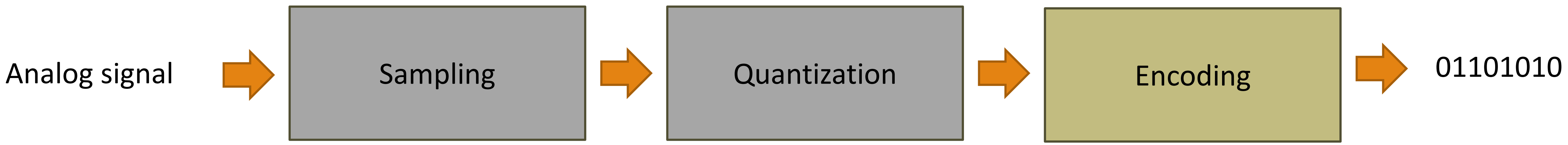
- $S_{16} < S_8 < S_4$
- $e_{16} < e_8 < e_4$

Analog to Digital Converter (ADC)

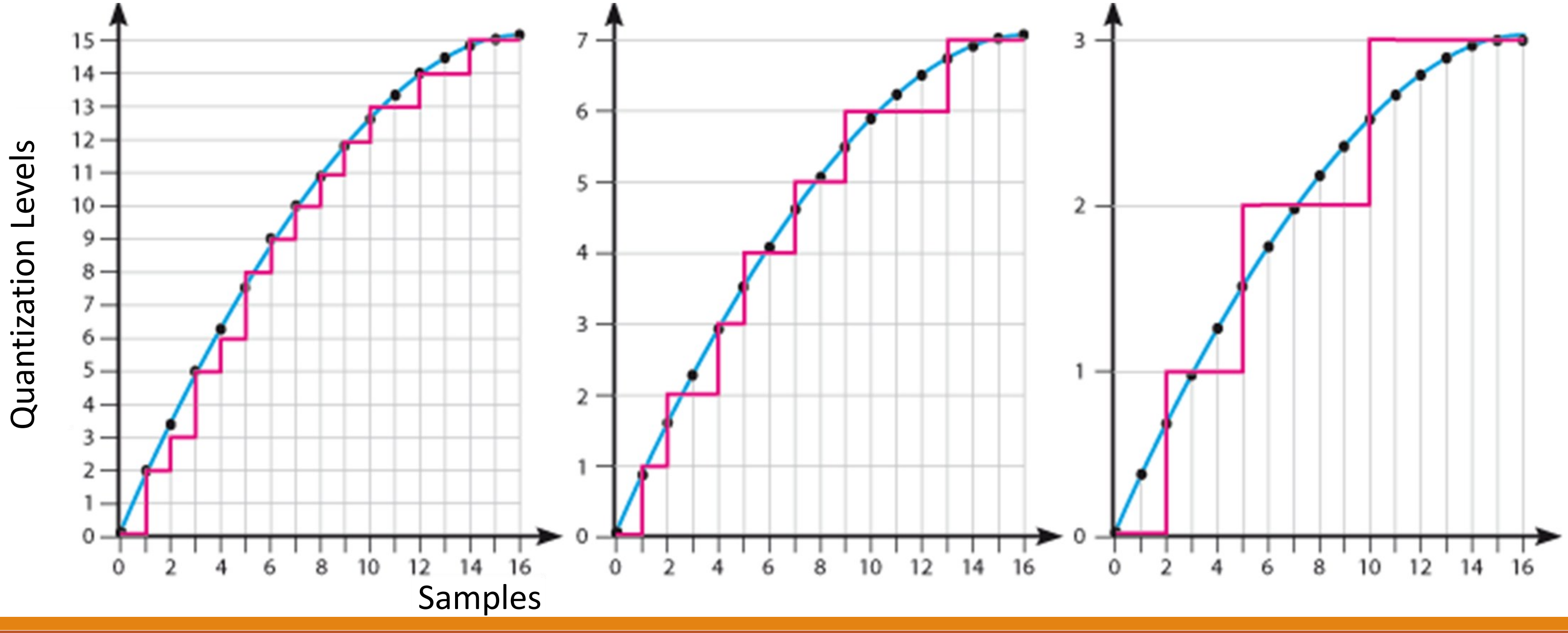


- Goal:
    - Assign each output level
    - To a unique binary code

Analog to Digital Converter (ADC)

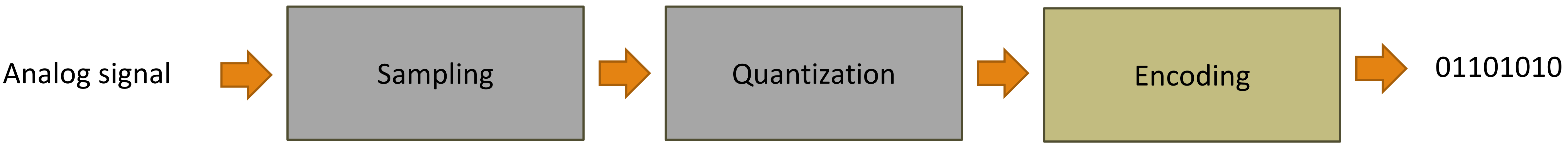


16 Quantization Levels | 8 Quantization Levels | 4 Quantization Levels

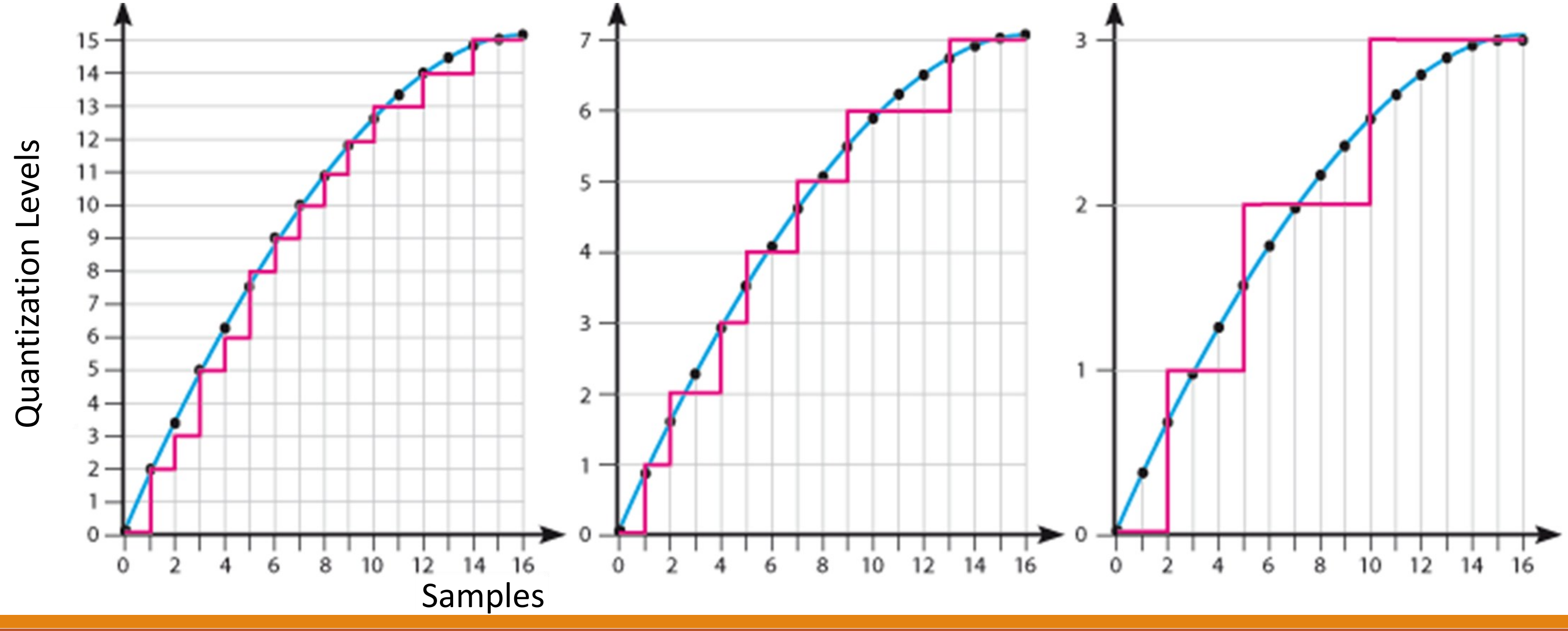


- How many bits do we need to represent 4 levels?
- How many bits do we need to represent 8 levels?
- How many bits do we need to represent 16 levels?

Analog to Digital Converter (ADC)

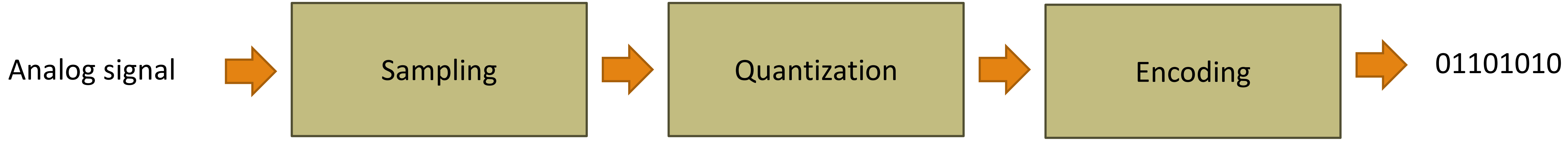


4 bits 3 bits 2 bits

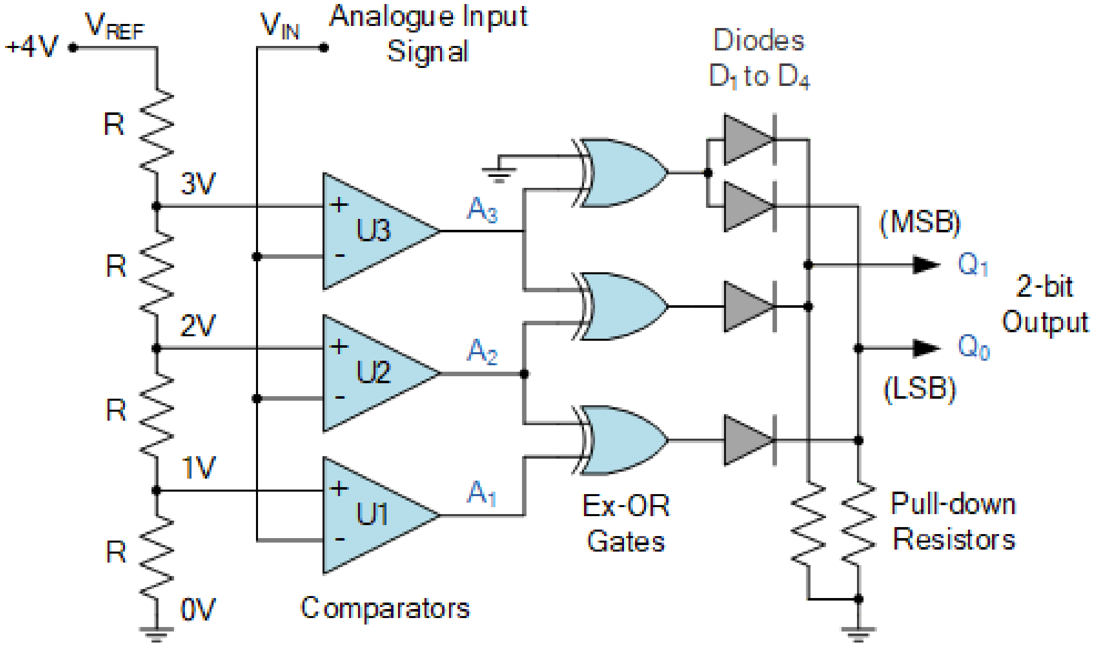


- How many bits do we need to represent 4 levels?
- How many bits do we need to represent 8 levels?
- How many bits do we need to represent 16 levels?

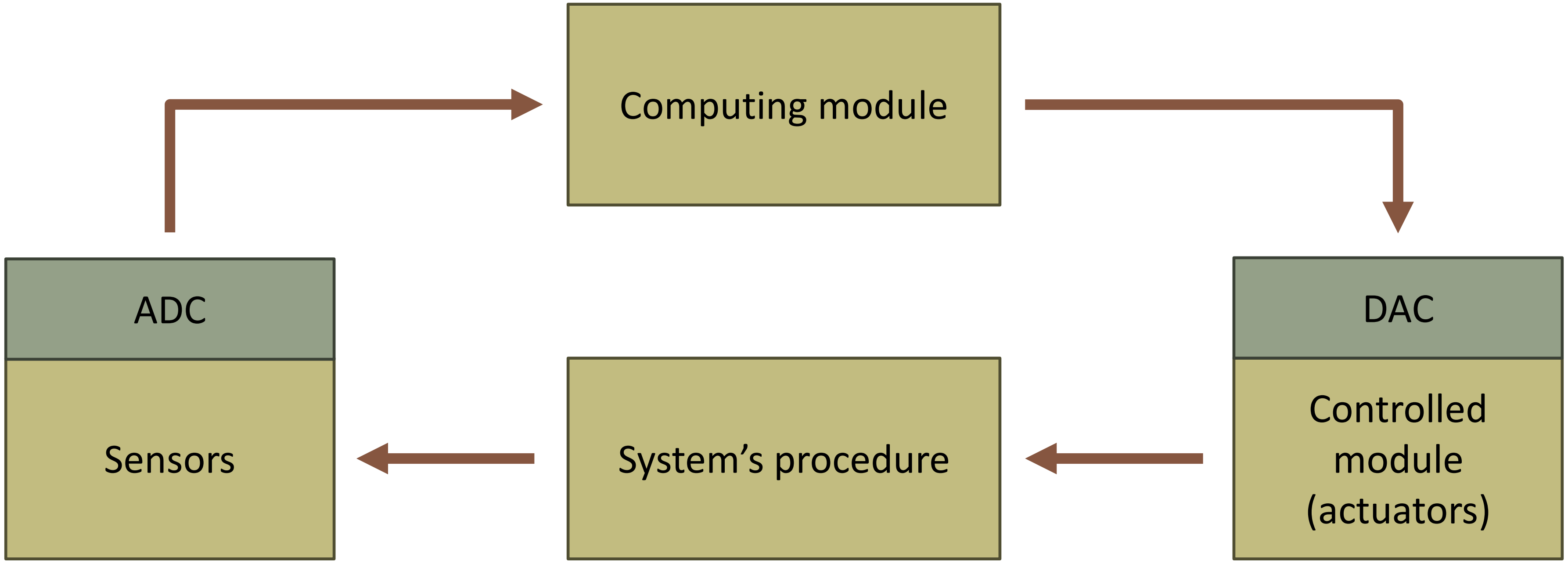
Analog to Digital Converter (ADC)



Simple ADC circuit example



Control loop



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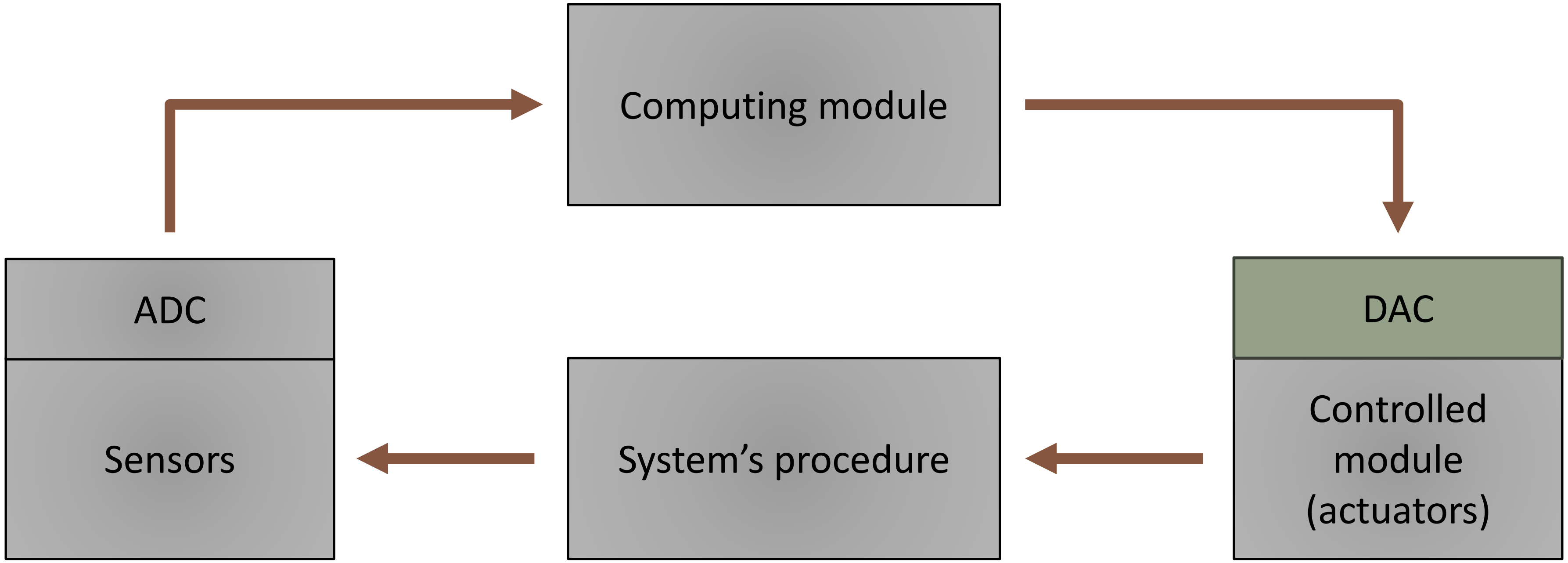
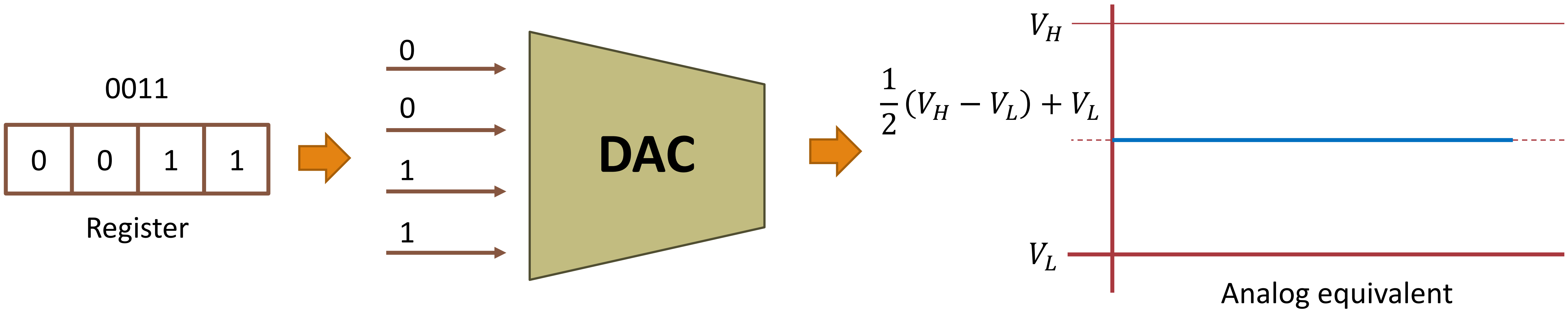
Control loop



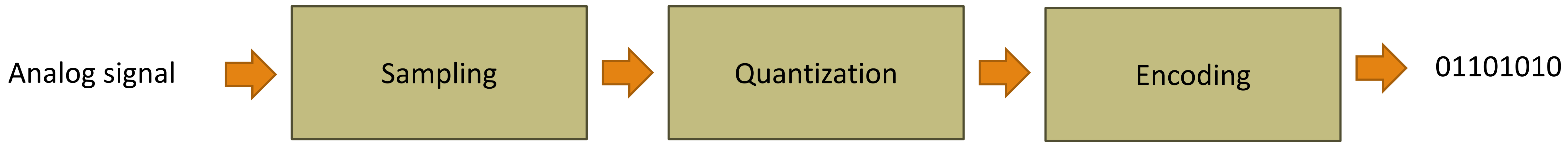
Digital to Analog Converters (DAC)::

Each digital input value is converted into a corresponding output voltage value between the V_L and V_H.



Mechatronics Automation

How do we achieve the reverse ADC process?

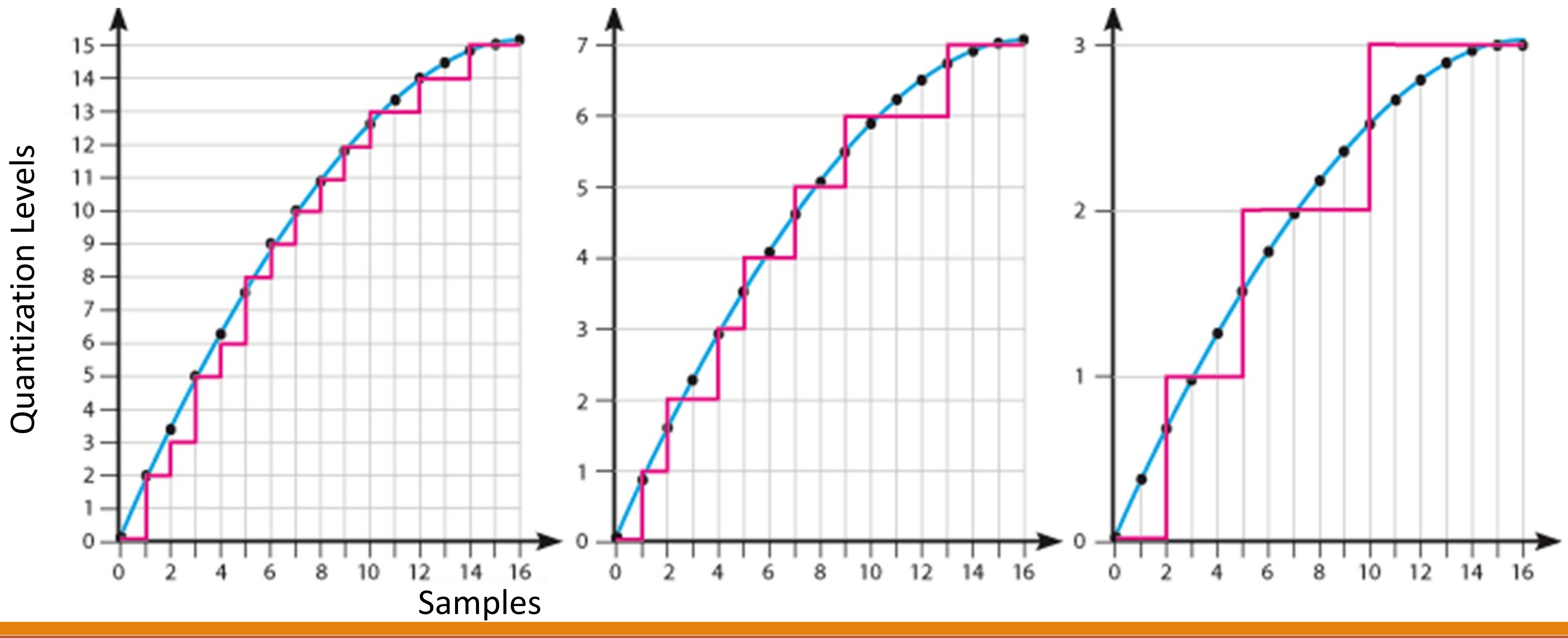


How do we achieve the reverse ADC process?

Digitalization:

Analog signal → Sampling → Quantization → Encoding → 01101010

4 bits | 3 bits | 2 bits



- Number of bits: n
- Available quantization levels: 2^n
- Range of digital representation: $0,\ldots,\ 2^n - 1$
- Digital equivalent of input signal:
  $b = (\ (m_q(t) - V_L)\ /\ (V_H - V_L)\ ) * (2^n - 1)$
- If $V_L = 0$:
  $b = (\ m_q(t)\ /\ V_H\ ) * (2^n - 1)$
  $b = (\ m_q(t)\ /\ V_{ref}\ ) * (2^n - 1)$

How do we achieve the reverse ADC process?

Decoding: Calculation of corresponding analogue voltage

- Analogue voltage value V_{out} with respect to the digital entry value b:

$$b = \frac{V_{out} - V_L}{V_H - V_L} * (2^n - 1) \quad \Rightarrow$$

$$b * (V_H - V_L) = (V_{out} - V_L) * (2^n - 1) \Rightarrow$$

$$b * (V_H - V_L) = V_{out} * (2^n - 1) - V_L * (2^n - 1) \Rightarrow$$

$$V_{out} * (2^n - 1) = b * (V_H - V_L) + V_L * (2^n - 1) \Rightarrow$$

$$V_{out} = \frac{b}{2^n - 1} * (V_H - V_L) + V_L$$

- Για $V_L = 0$:

$$V_{out} = \frac{b}{2^n - 1} * V_H$$

$$V_{out} = \frac{b}{2^n - 1} * V_{ref}$$

- Για μεγάλες τιμές του n :

$$V_{out} \approx \frac{b}{2^n} * V_{ref}$$

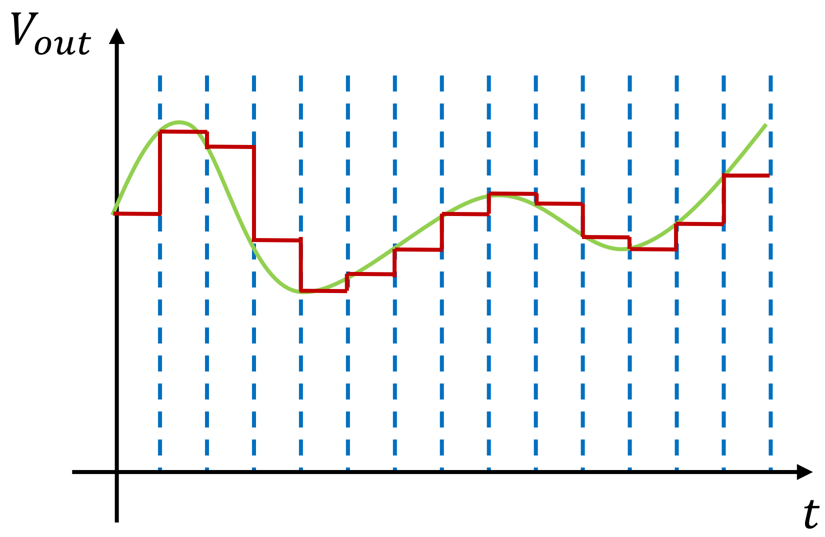
How do we achieve the reverse ADC process?

Quantization:

The output voltage (V_{out}) remains quantized at the available quantization levels depending on the number of digits

$$V_{out} = \frac{b}{2^n} * V_{ref}$$

- Number of bits: n
- Available quantization levels: 2^n
- Analogue voltage range: $0,\ldots,V_{ref}$
- Resolution (step): $\frac{1}{2^n} * V_{ref}$



DAC:: Circuit diagram

We need a circuit that succeeds: $V_{out} = \frac{b}{2^n} * V_{ref}$

Voltage Divider

However, since: $b = 2^{(n-1)} b_{n-1} + \cdots + 2^3 b_3 + 2^2 b_2 + 2^1 b_1 + 2^0 b_0 \Rightarrow$

$$V_{out} = V_{ref} \left(\frac{2^{(n-1)}}{2^n} b_{n-1} + \cdots + \frac{2^3}{2^n} b_3 + \frac{2^2}{2^n} b_2 + \frac{2^1}{2^n} b_1 + \frac{2^0}{2^n} b_0 \right)$$

$$V_{out} = V_{ref} \left(\frac{b_{n-1}}{2^1} + \cdots + \frac{b_3}{2^{n-3}} b_3 + \frac{b_2}{2^{n-2}} + \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n} \right)$$

Operational Amplifier: Summing Amplifier

Two basic circuits:

- Binary weighted resistor DAC
- R-2R ladder DAC

Binary weighted resistor DAC

Operational Amplifier:

$$\frac{V_{out}}{R_f}+\frac{-V_{ref}b_0}{2^3R}+\frac{-V_{ref}b_1}{2^2R}+\frac{-V_{ref}b_2}{2^1R}+\frac{-V_{ref}b_3}{2^0R}=0\Rightarrow$$

$$\frac{V_{out}}{R_f}=\frac{V_{ref}b_0}{2^3R}+\frac{V_{ref}b_1}{2^2R}+\frac{V_{ref}b_2}{2^1R}+\frac{V_{ref}b_3}{2^0R}\Rightarrow$$

$$V_{out}=V_{ref}\frac{R_f}{2^3R}b_0+V_{ref}\frac{R_f}{2^2R}b_1+V_{ref}\frac{R_f}{2^1R}b_2+V_{ref}\frac{R_f}{2^0R}b_3\Rightarrow$$

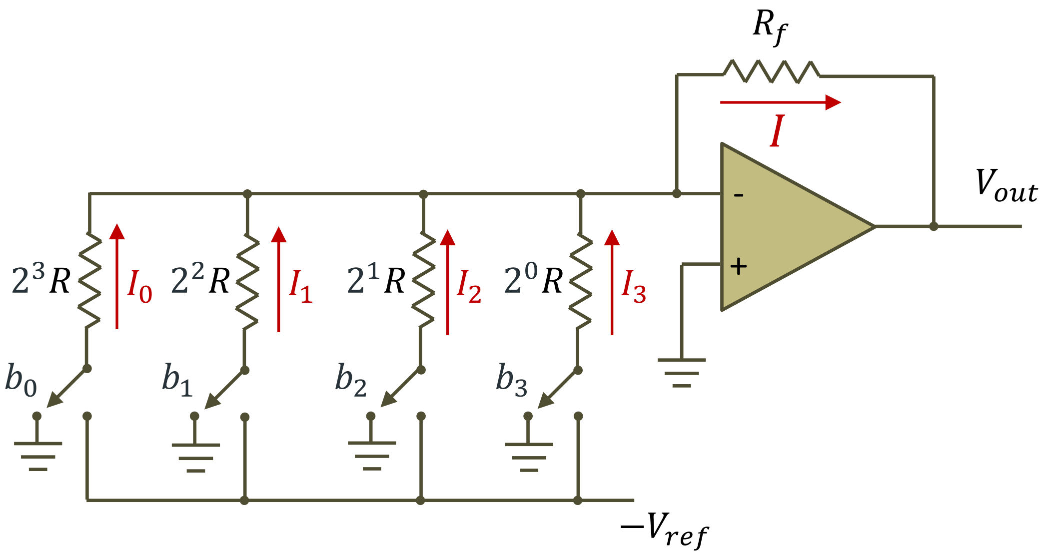
$$V_{out}=\frac{V_{ref}R_f}{R}\left(\frac{b_3}{2^0}+\frac{b_2}{2^1}+\frac{b_1}{2^2}+\frac{b_0}{2^3}\right)\xRightarrow{R=2R_f}$$

$$V_{out}=\frac{V_{ref}R_f}{2R_f}\left(\frac{b_3}{2^0}+\frac{b_2}{2^1}+\frac{b_1}{2^2}+\frac{b_0}{2^3}\right)\Rightarrow$$

$$V_{out}=\frac{V_{ref}}{2}\left(\frac{b_3}{2^0}+\frac{b_2}{2^1}+\frac{b_1}{2^2}+\frac{b_0}{2^3}\right)=V_{ref}\left(\frac{b_3}{2^1}+\frac{b_2}{2^2}+\frac{b_1}{2^3}+\frac{b_0}{2^4}\right)$$

$$V_{out}=V_{ref}\left(\frac{b_{n-1}}{2^1}+\cdots+\frac{b_3}{2^{n-3}}b_3+\frac{b_2}{2^{n-2}}+\frac{b_1}{2^{n-1}}+\frac{b_0}{2^n}\right)$$

$$n=4:\quad V_{out}=V_{ref}\left(\frac{b_3}{2^1}+\frac{b_2}{2^2}+\frac{b_1}{2^3}+\frac{b_0}{2^4}\right)$$

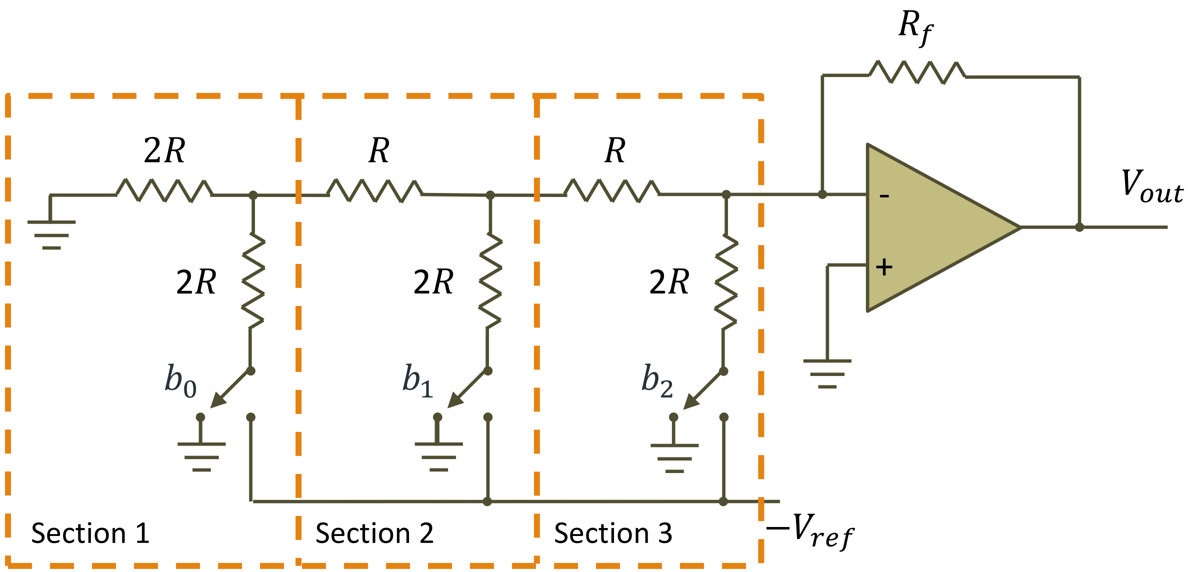


Recall that for an Operational Amplifier:

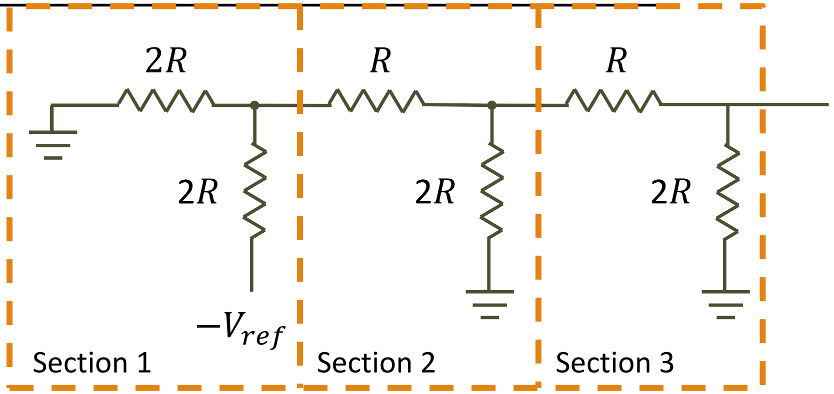
- The inverting input is virtually short-circuited to the ground without allowing the current to pass through

R-2R ladder DAC:: Circuit analysis for 3 bits

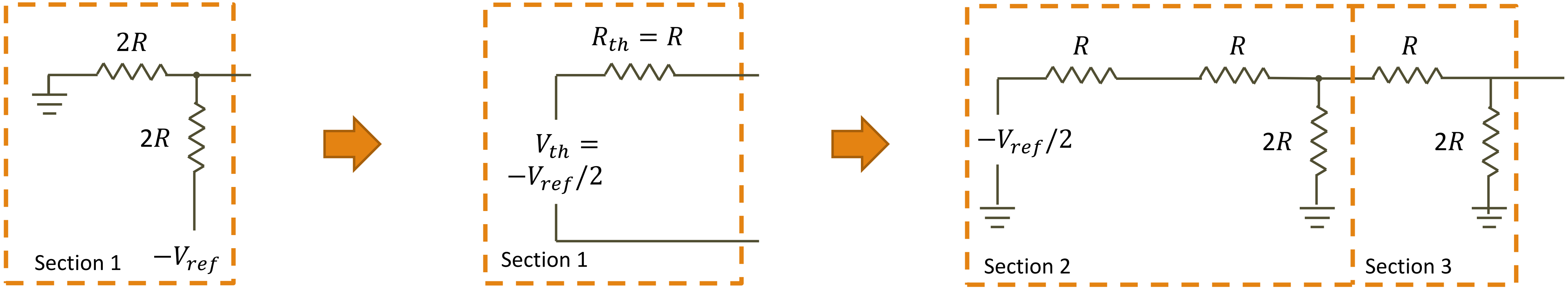
- Analysis by superposition principle and Thevenin's theorem:
  - Έστω:
    - $b_0 = 1, b_1 = 0, \ b_2 = 0$
    - $b_0 = 0, b_1 = 1, \ b_2 = 0$
    - $b_0 = 0, b_1 = 0, \ b_2 = 1$
  - Separate analysis for the 3 sections



R-2R ladder DAC:: Circuit analysis for 3 bits



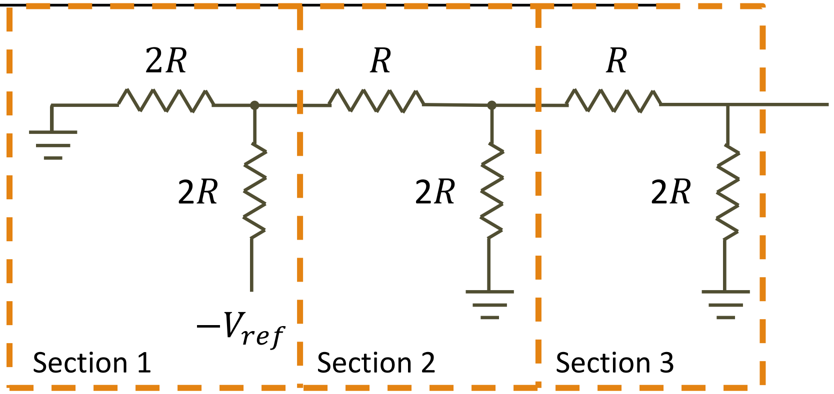
- Let: $b_0 = 1, b_1 = 0,\ b_2 = 0$
- Section 1:



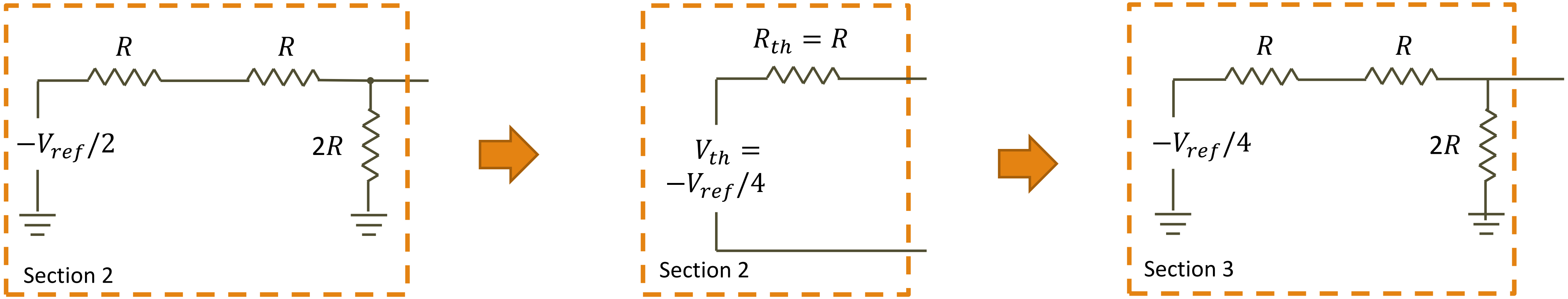
$$V_{th} = -V_{ref}/2$$
$$R_{th} = R$$

Mechatronics Automation

R-2R ladder DAC:: Circuit analysis for 3 bits



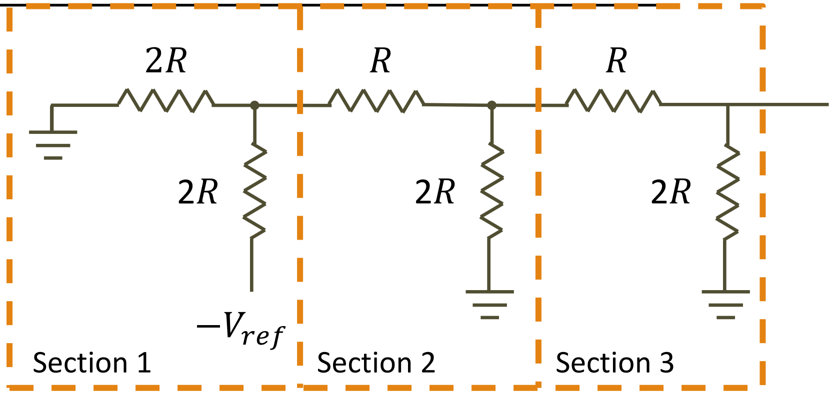
- Let: $b_0 = 1, b_1 = 0,\ b_2 = 0$
- Section 2:



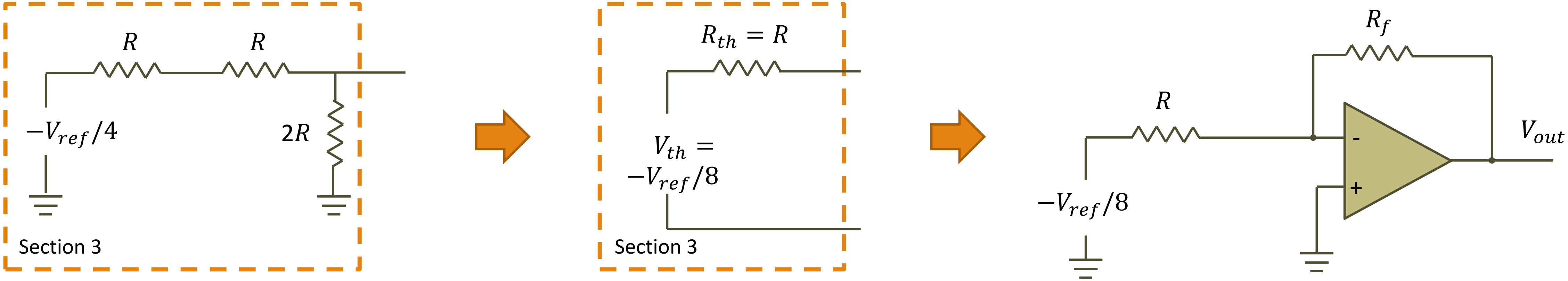
$$V_{th} = -V_{ref}/4$$
$$R_{th} = R$$

Mechatronics Automation

R-2R ladder DAC:: Circuit analysis for 3 bits



- Let: $b_0 = 1, b_1 = 0,\ b_2 = 0$
- Section 3:

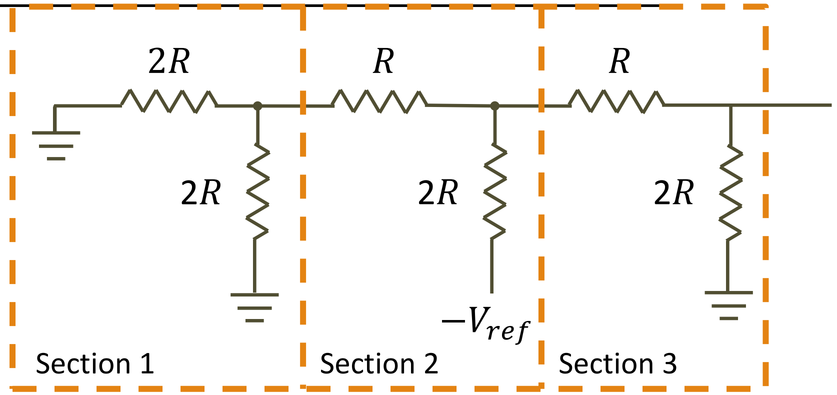


$$V_{th} = -V_{ref}/8$$
$$R_{th} = R$$

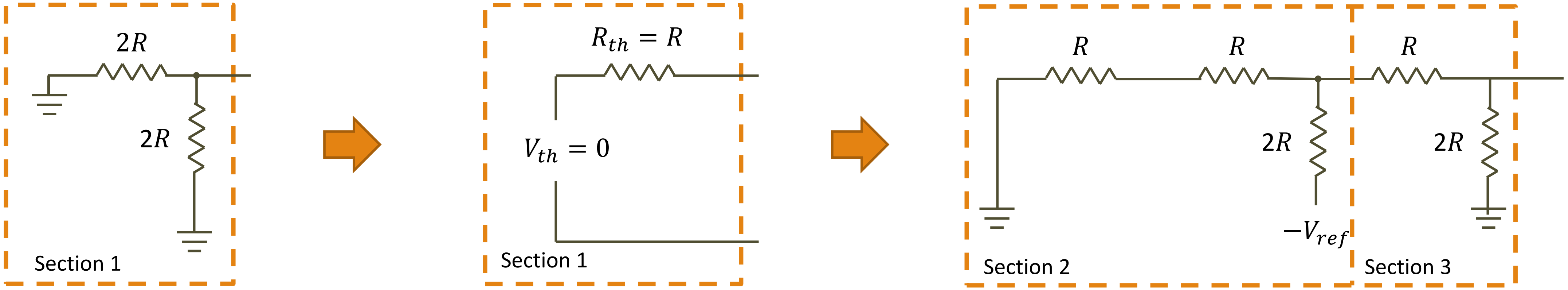
$$V_{out} = -\left(\frac{-V_{ref}}{8}\right)\frac{R_f}{R} \xRightarrow{R_f=R}$$

$$V_{out} = \frac{V_{ref}}{8}$$

R-2R ladder DAC:: Circuit analysis for 3 bits

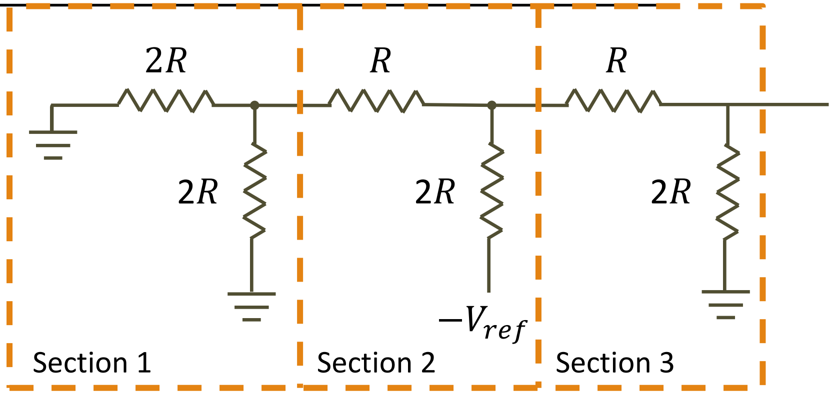


- Let: $b_0 = 0, b_1 = 1,\ b_2 = 0$
- Section 1:

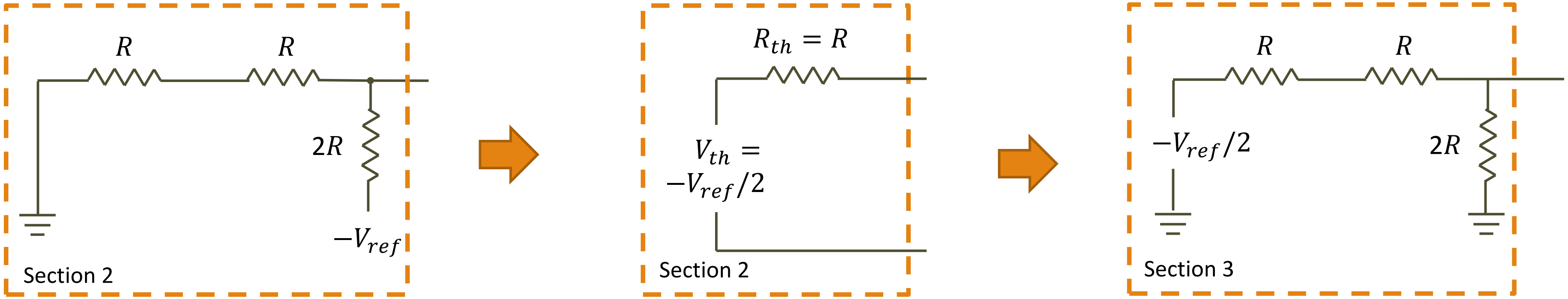


$$V_{th} = 0$$
$$R_{th} = R$$

R-2R ladder DAC:: Circuit analysis for 3 bits

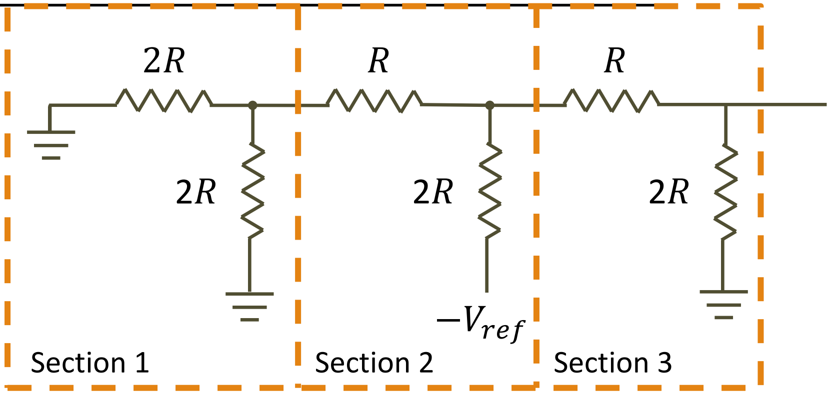


- Let: $b_0 = 0, b_1 = 1,\ b_2 = 0$
- Section 2:

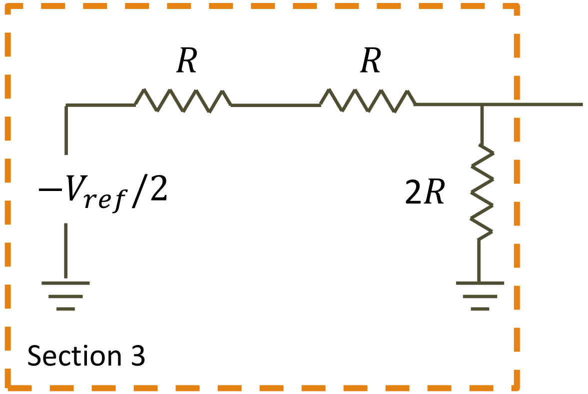


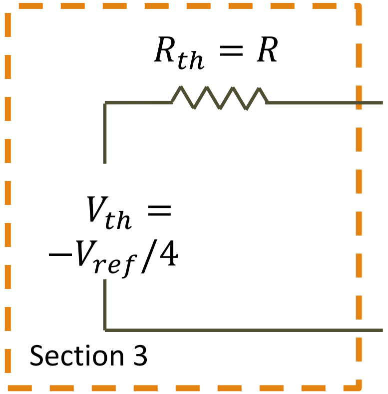
$$V_{th} = -V_{ref}/2$$
$$R_{th} = R$$

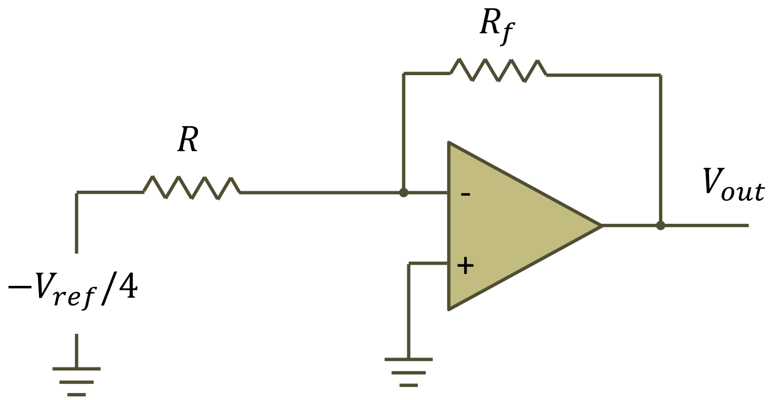
R-2R ladder DAC:: Circuit analysis for 3 bits



- Let: $b_0 = 0, b_1 = 1,\ b_2 = 0$
- Section 3:



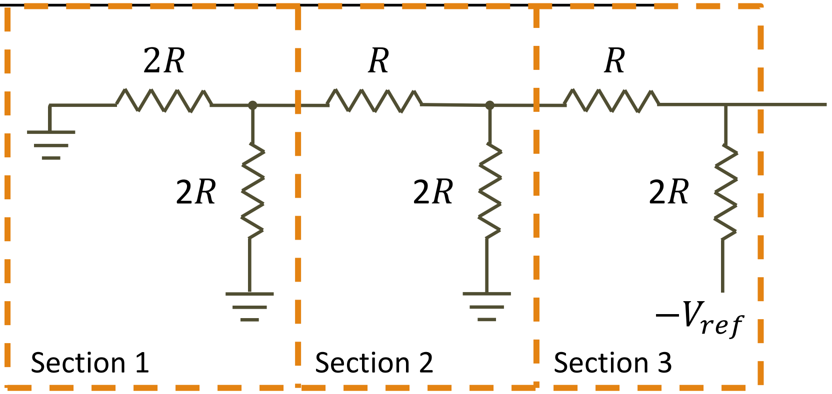




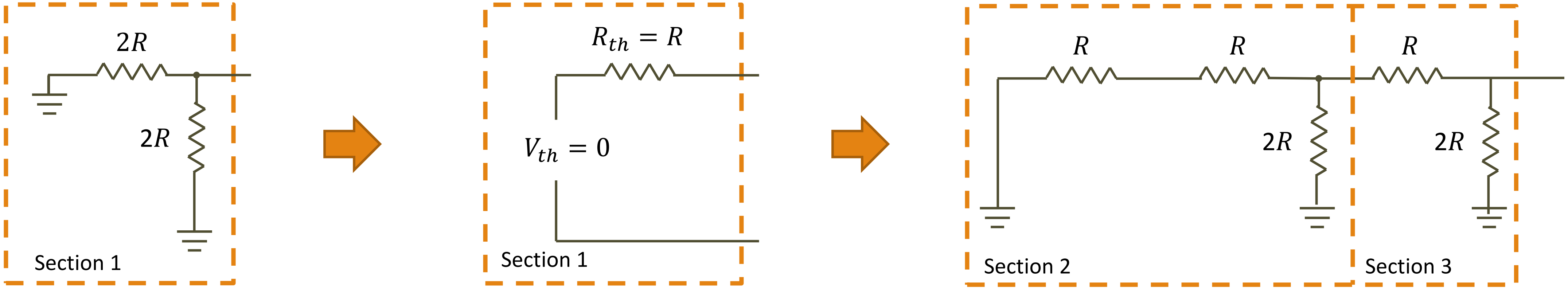
$$V_{th} = -V_{ref}/4$$
$$R_{th} = R$$

$$V_{out} = -\left(\frac{-V_{ref}}{4}\right)\frac{R_f}{R} \overset{R_f=R}{\Longrightarrow}$$
$$V_{out} = \frac{V_{ref}}{4}$$

R-2R ladder DAC:: Circuit analysis for 3 bits

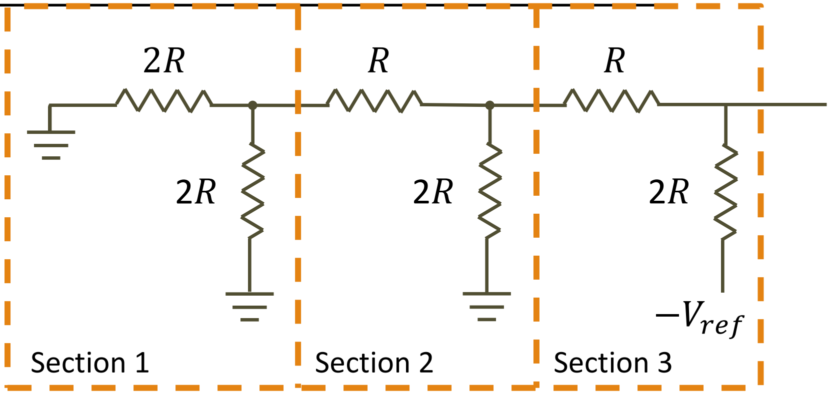


- Let: $b_0 = 0, b_1 = 0,\ b_2 = 1$
- Section 1:

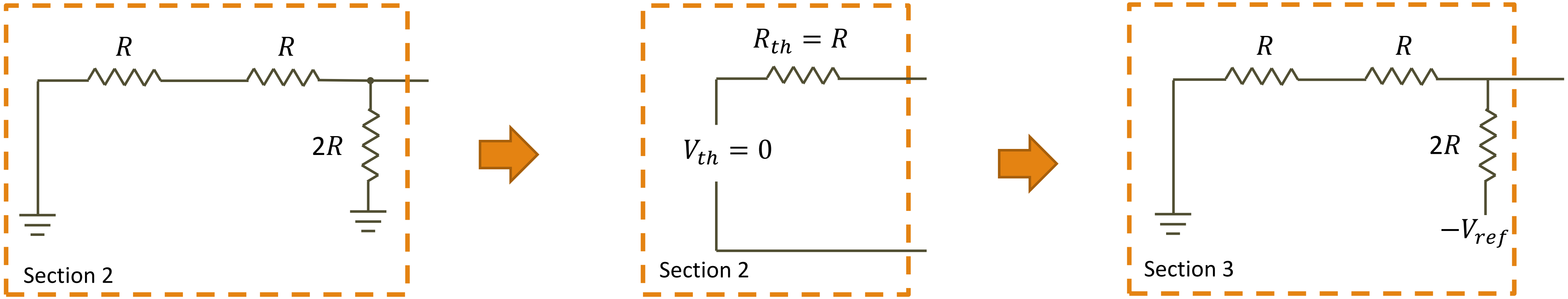


$$V_{th} = 0$$
$$R_{th} = R$$

R-2R ladder DAC:: Circuit analysis for 3 bits

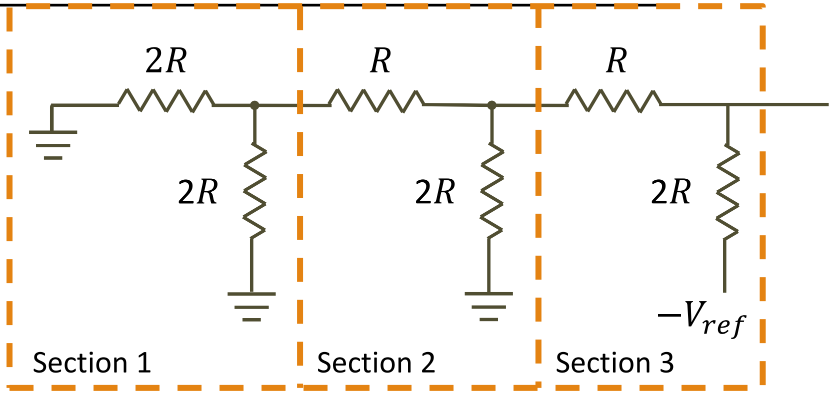


- Let: $b_0 = 0, b_1 = 0,\ b_2 = 1$
- Section 2:

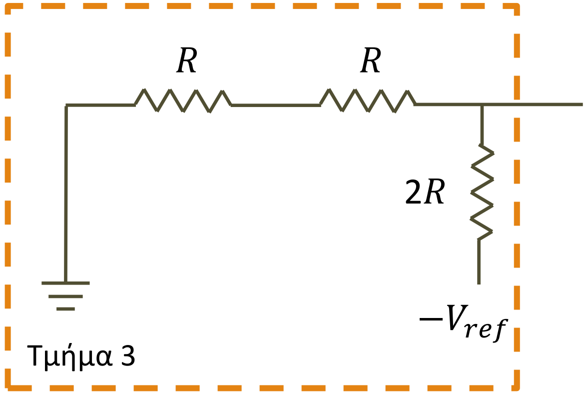


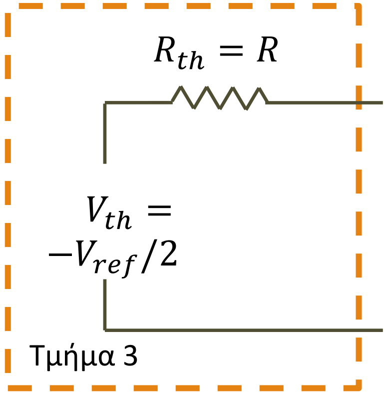
$$V_{th} = 0$$
$$R_{th} = R$$

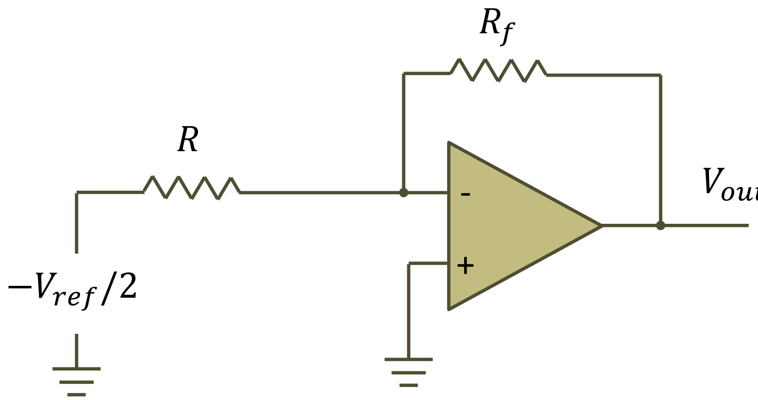
R-2R ladder DAC:: Circuit analysis for 3 bits



- Let: $b_0 = 0, b_1 = 0,\ b_2 = 1$
- Section 3:







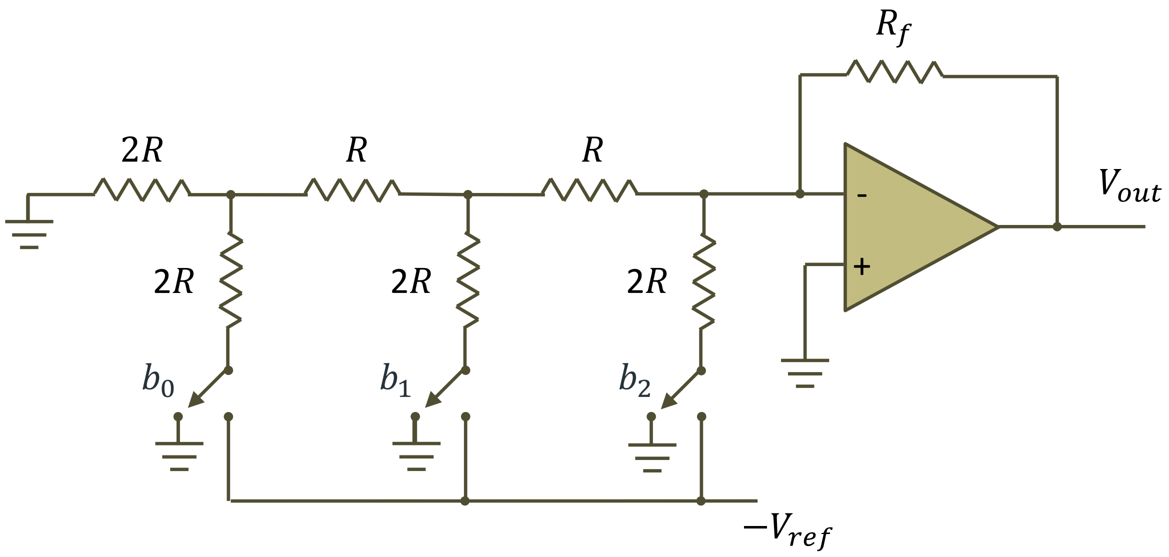
$$V_{th} = -V_{ref}/2$$
$$R_{th} = R$$

$$V_{out} = -\left(\frac{-V_{ref}}{2}\right)\frac{R_f}{R} \xRightarrow{R_f=R}$$
$$V_{out} = \frac{V_{ref}}{2}$$

R-2R ladder DAC:: Circuit analysis for 3 bits

Therefore:

- For: $b_0 = 1,\ b_1 = 0,\ b_2 = 0$
  - $V_{out} = \frac{V_{ref}}{8}$
- For: $b_0 = 0,\ b_1 = 1,\ b_2 = 0$
  - $V_{out} = \frac{V_{ref}}{4}$
- For: $b_0 = 0,\ b_1 = 0,\ b_2 = 1$
  - $V_{out} = \frac{V_{ref}}{2}$



From the superposition principle and due to the operational amplifier (summing amplifier):

$$V_{out} = b_2\frac{V_{ref}}{2} + b_1\frac{V_{ref}}{4} + b_0\frac{V_{ref}}{8} \Rightarrow \qquad V_{out} = V_{ref}\left(\frac{b_2}{2} + \frac{b_1}{4} + \frac{b_0}{8}\right)$$

$$\Rightarrow \qquad V_{out} = V_{ref}\left(\frac{b_2}{2^1} + \frac{b_1}{2^2} + \frac{b_0}{2^3}\right)$$